Russian Physics Journal, Vol. 49, No. 12, 2006

DEFECTS IN THE GaAs AND InGaAs LAYERS GROWN BY LOW-TEMPERATURE MOLECULAR-BEAM EPITAXY

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UDC 621.315.592:548.552.22

The problem of defect formation in the GaAs and InGaAs layers grown by low-temperature molecular-beam epitaxy is discussed. The effect of growth conditions (temperature and flux ratio between the elements of groups III and V) on the morphology of growth surface, internal structure, type, and concentration of electrically- and optically active defects is analyzed. A comparison is made between the defect formation processes occuring during the epitaxial growth and post-growth annealing of the layers.

INTRODUCTION

Low-temperature molecular-beam epitaxy (*LT*-MBE) of gallium arsenide and other compounds III-V has been increasingly studied in recent years. It was shown that a decrease in the growth temperature from conventional values of 500–600°C down to 150–200°C results in the incorporation of excess non-stoichiometric arsenic into the lattice mainly in the form of point defects [1–6]. *LT*-GaAs containing excess arsenic possesses unique physical properties such as high specific resistance (up to 10^8 Ω·cm) and a very low lifetime of minority charge carriers (<1 ps). This material is promising for fabricating high-speed photodetectors, unipolar transistors, integrated circuits, etc. In addition, *LT*-layers containing excess arsenic are of great scientific interest for investigation of intrinsic point defects in III-V compounds and their effect on the electrical and optical properties of the material.

At present, the structure and properties of *LT*-GaAs and related compounds are widely studied in a number of countries. In Russia, research along this line is performed in the A. F. Ioffe Physical Technical Institute (St. Petersburg), Institute of Semiconductor Physics of Siberian Branch of Russian Academy of Sciences (Novosibirsk), and Tomsk State University and V. D. Kuznetsov Siberian Physical Technical Institute (Tomsk). The effect of growth conditions on the growth-surface morphology, electrical and optical properties of *LT*-GaAs and InGaAs were examined in detail by our research team. In this paper, on the basis of these studies, the problem of defect formation in *LT*-GaAs and InGaAs is considered. The paper is written using the materials published in [6–15]. A total review of the current state of the art in the technology of low-temperature molecular beam epitaxy is given in [16].

GROWTH AND INVESTIGATION TECHNOLOGY

Epitaxial GaAs and InGaAs layers were grown in a Katun' MBE facility in the Institute of Semiconductor Physics of Siberian Branch of Russian Academy of Sciences (Novosibirsk). First, a 50 nm thick buffer layer was grown at 580°C on semi-insulating GaAs substrates of (001) orientation. Then, the temperature was reduced down to 150–250°C and a non-doped or a silicon-doped ($N_{Si} = 1 \cdot 10^{19}$ cm^{-3}) 1μm thick *LT*-GaAs layer was grown. The growth rate was controlled by a constant Ga flux of 1 μm/h. The Ga ratio (J_{As}/J_{Ga}) was varied in the range from 1 to 20 by the As flux variation. As a rule, a flux of As_4 molecules was used; however, a flux of As_2 molecules was applied in a number of experiments.

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 1064-8887/06/4912-1334

The InGaAs layers were grown using a similar technology on the semi-insulating (001) InP substrates. The ratio of the III-group elements (In and Ga) was chosen so that the lattice parameter of the InGaAs film matched that of the InP substrate, which corresponds to the following composition: $In_{0.53}Ga_{0.47}As$. The growth temperature was varied in the range from 150 to 480°C, the ratio between the As and III-group element fluxes (J_{As}/J_{III}) in the molecular beam was changed in the range from 0.02 to 20 at a growth rate of 1 μm/h, with a typical layer thickness being 1 μm.

After deposition, the GaAs and InGaAs samples were removed from the growth chamber and divided in two groups. The samples of the first group were studied immediately after epitaxial growth (*as grown*), whereas the others were studied upon 10-minute annealing in the growth chamber at 500 or 600°C in the As_4 flux.

The growth-surface relief was examined by electron microscopy (using the method of replicas). The internal layer structure was studied by transmission electron microscopy (TEM) including high-resolution electron microscopy (HREM) and x-ray diffractometry using CuK_α-radiation and the (004) reflex. To study the point defects, the optical absorption spectra in the near infrared range as well as photoluminescence spectra at $T = 77$ K were measured. The electrophysical parameters of the layers were determined by measuring the conductivity and Hall constant (Van-der-Pouw technique).

AN *LT*-GaAs LAYER STRUCTURE

Growth-surface structure

The electron-microscopic investigation of the samples using the method of replicas shows that a homogeneous micrograin relief is formed on the epitaxial layer surface at a growth temperature of 150°C. The grains have an average size of ~100 nm and are extended along one direction. As the growth temperature increases, the grain size dereases down to 3–5 nm at $T_g = 250$°C) [6].

An increase in the As flux (both in the As_4 and As_2 form) results in the change of the growth- surface relief [11]. A morphologically uniform surface without special features formed at $J_{As}/J_{Ga} \approx 1$ transforms to a nonuniform one with microdefects (round submicron growth pits). The pit density increases with the J_{As}/J_{Ga} ratio. A comparison of the surface microreliefs of the layers grown using the As_4 and As_2 fluxes shows that the increase in the As_2 flux results both in the formation of the submicron pits and general roughening of the surface.

The surface microrelief of the layers doped by silicon is more uniform. The surface of doped layers is microrough and contains a great number of nano-sized ridges in the entire range of the J_{As}/J_{Ga} ratios. The growth pits similar to those in the non-doped layers are formed in silicon-doped layers only at high As fluxes ($J_{As}/J_{Ga} \geq 10$).

LT-GaAs lattice deformation

Earlier studies of the x-ray spectra showed that the *LT*-GaAs layers contain excess non-stoichiometric arsenic As_{ex}, whose concentration depends on the growth conditions. As the growth temperature T_g decreases in the range $250 \geq T_g \geq 150$°C, the As_{ex} concentration increases up to the maximum value ~ 1.5 at. % at $T_g = 150$ °C [6].

The incorporation of excess arsenic is accompanied with a tetragonal distortion of the *LT*-GaAs lattice in the direction perpendicular to the substrate surface. An increase in the lattice parameter of the layer relative to that in the substrate is observed for all examined samples grown at $T_g \leq 250$°C, that is, $\Delta a/a = (a_l - a)/a > 0$ (here a_l and a correspond to the layer and the substrate, respectively). $\Delta a/a$ and $[As_{ex}]$ increase monotonically, as the growth temperature decreases. Analysis of the experimental results revealed a linear correlation between the change in the lattice parameter $\Delta a/a$ and the excess arsenic concentration $[As_{ex}]$ (atom/cm^3), which can be represented as $\Delta a/a \approx 5 \cdot 10^{-22} [As_{ex}]$. This dependence can be used for estimation of $[As_{ex}]$ using the measurements of $\Delta a/a$ by the x-ray diffraction method, since this method is more straightforward than x-ray spectrum microanalysis.

Along with the growth temperature, the ratio of As and Ga fluxes in a molecular beam significantly affects the excess arsenic concentration and *LT*-GaAs lattice parameter [10]. The lattice parameter of the layers grown at 150°C dramatically increases at a small deviation from the stoichiometric conditions ($1 < J_{As}/J_{Ga} < 3$), reaches the maximum, and then smoothly decreases (Fig. 1). Similar dependence of $\Delta a/a$ on J_{As}/J_{Ga} was also observed at $T_g = 200$°C [12, 17]. At

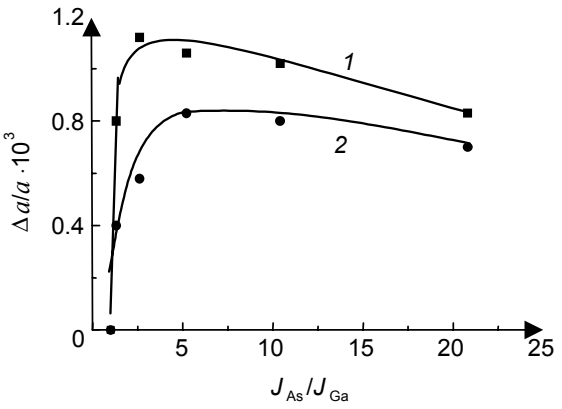

Fig. 1. The effect of the J_{As}/J_{Ga} ratio on the change in the lattice parameter in undoped (*1*) and Si doped (*2*) GaAs layers.

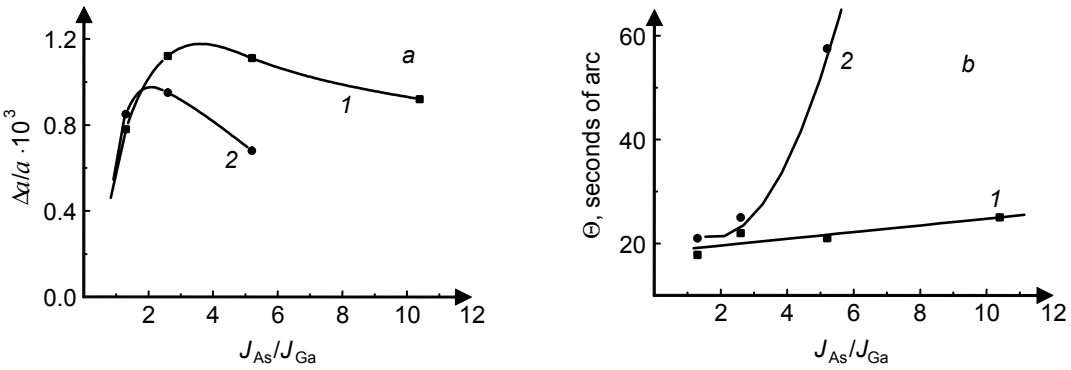

Fig. 2. A Lattice parameter (*a*) and a diffraction peak half-width (*b*) versus J_{As}/J_{Ga} ratio for the GaAs layers grown using As_4 (*1*) and As_2 (*2*) fluxes.

higher temperatures, $\Delta a/a$ increases with J_{As}/J_{Ga} and reaches its limit (saturates) corresponding to the arsenic excess concentration maximum possible at this temperature [17].

It is seen from Fig. 1 that the doping impurity has a pronounced effect on the lattice parameter of *LT*-GaAs. In the silicon doped layers ($N_{Si} = 1 \cdot 10^{19}$ cm^{-3}), $\Delta a/a$ decreases as compared to the undoped layers in the whole range of the J_{As}/J_{Ga} ratios. The observed change in $\Delta a/a$ is an order of magnitude higher than that expected for the case of substitution of Ga atoms for silicon ones. Hence, it follows that a decrease in the lattice parameter in the Si doped layers is due to a decrease in the excess arsenic concentration. A similar effect of displacement of excess arsenic was observed for *LT*-GaAs doped by silicon or beryllium [18–20].

The experiments on growth of layers using different arsenic molecular forms (As_2 or As_4) showed [11] that in the case of As_2 flux, the lattice parameter changes less, while the changes in the diffraction peak half-width Θ characterizing the structure disordering are more noticeable than those in the case of As_4 flux at similar growth conditions (Fig. 2). Crystalline perfection of the layers grown using the As_2 flux is drastically decreased with increase in J_{As}/J_{Ga}. At $J_{As}/J_{Ga} > 5$, the epitaxial growth is ceased.

Thus, it follows from these results that in *LT*-GaAs, a high concentration of excess arsenic (up to 1.5 at. %), a tetragonal lattice distortion, and an increase in the lattice parameter relative to that in the substrate are observed. Lattice deformation of *LT*-GaAs essentially depends on the growth conditions: growth temperature, flux ratio of As and Ga, presence of the doping impurity, and molecular form of arsenic. $\Delta a/a$ increases with decreasing the temperature and

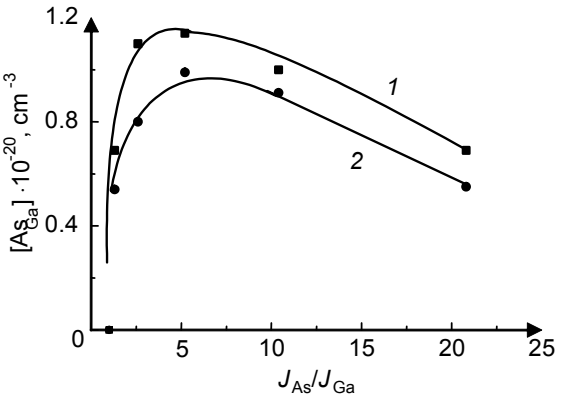

Fig. 3. Dependence of the As_{Ga} defect concentration on the flux ratio J_{As}/J_{Ga} for undoped (*1*) and Si-doped (*2*) GaAs layers.

increasing the flux ratio (for $J_{As}/J_{Ga} < 5$). Silicon doping and replacing As_4 by As_2 result in a decrease in the *LT*-GaAs lattice deformation.

Point defects in *LT*-GaAs

It is well known that within the homogeneity region of a GaAs single crystal, non-stoichiometric arsenic occupies the interstitial (As_i) and antisite positions (As_{Ga}). Simultaneously, vacancies (V_{Ga}) are generated in the gallium sublattice. The equilibrium concentration of these defects exponentially decreases with temperature down to 10^9 cm^{-3} at $T < 500$°C [21, 22].

The excess arsenic concentration in *LT*-GaAs reaches 1.5 at. % ($3.3 \cdot 10^{20}$ atom/cm^{-3}), which exceeds the equilibrium solubility limit of As at growth temperatures of 150–200°C by many orders of magnitude and is indicative of a highly nonequilibrium state of point defects in *LT*-layers. According to the litearature data [23–25], the ensemble of point defects in *LT*-GaAs includes the same three main defects: As_{Ga}, V_{Ga}, and As_i, the concentration of antisite arsenic being dominant [24].

The measurements of IR-absorption spectra show that the concentration of As_{Ga} antisite defects depends on the growth conditions [10]. As the growth temperature T_g decreases, the As_{Ga} concentration increases up to the maximum value ~ $1.2 \cdot 10^{20}$ cm^{-3} at $T_g = 150$°C, which is in qualitative agreement with the data on excess arsenic incorporation. Figure 3 demonstrates the effect of the flux ratio J_{As}/J_{Ga} on the As_{Ga} concentration for undoped and silicon-doped layers grown at $T_g = 150$°C. A comparison of Figs 1 and 3 shows that with increasing J_{As}/J_{Ga}, the As_{Ga} concentration and lattice deformation $\Delta a/a$ change symbasically. This fact supports the conclusion [24] that antisite arsenic is the dominating defect responsible for the increase in the *LT*-GaAs lattice parameter. It is also seen that the As_{Ga} defect concentration in the silicon-doped layers is lower than that in the undoped layers (Fig. 3). The displacement of excess As by the Si impurity is observed in all *LT*-layers, independently of the growth temperature, flux ratio J_{As}/J_{Ga}, and form of the molecular beam used (As_2 or As_4). This effect is assumed to be due to the competition between the As and Si atoms for the sites of incorporation into the Ga sublattice and to the increase in the energy of the As_{Ga} defect formation resulting from the shift of the Fermi level to the conduction band bottom in the Si-doped layers [12].

The measured photoluminescence (PL) spectra show that the *LT*-layers are characterized by a very low intensity of radiative recombination. This seems to be due to high concentrations of As_{Ga} antisite defects and gallium vacancies, since both types of defects are taken to be the centers of nonradiative recombination. The presence of high concentrations of As_{Ga} defects and V_{Ga} in *LT*-layers is supported by measurements of their electrophysical parameters. The undoped *LT*-layers have a specific resistance of $\rho \geq 10^2$ Ω·cm caused by hopping conductivity through the localized states belonging to the antisite As_{Ga} defects [6, 26]. In the silicon doped layers ($N_{Si} = 1 \cdot 10^{19}$ cm^{-3}), the conductivity is due to free-charge carriers, whose

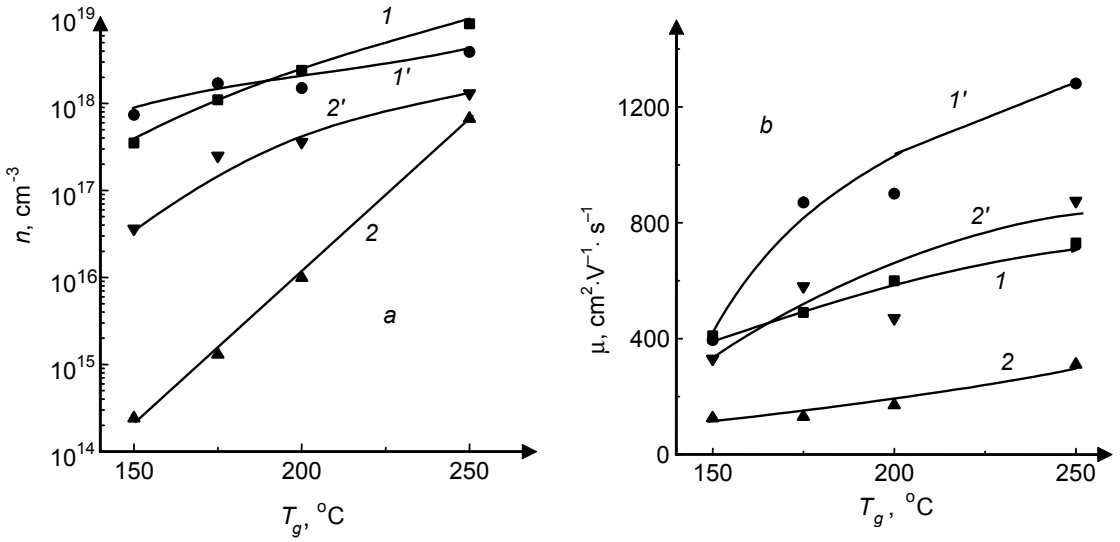

Fig. 4. Growth-temperature dependence of free charge-carrier concentration (*a*) and mobility (*b*) in GaAs layers grown at $J_{As}/J_{Ga} = 1.1$ (*1* and *1′*) and $J_{As}/J_{Ga} = 3$ (*2* and *2′*). *As-grown* (*1* and *2*) and upon annealing (*1′* and *2′*).

concentration and mobility strongly depend on the growth temperature and flux ratio J_{As}/J_{Ga} (Fig. 4). In the range of low J_{As}/J_{Ga}, where the layer composition is close to a stoichiometric one, the parameters of the *LT*-GaAs are close to those of the layers grown at high temperatures (500–600°C). An increase in the excess arsenic concentration caused both by a decrease in the growth temperature and an increase in the flux ratio J_{As}/J_{Ga} results in a drastic decrease in the free charge-carrier concentration and in an increase in the compensation factor [10].

The high compensation factor in *LT*-GaAs with excess As cannot be attributed to the amphoteric behaviour of silicon, because the probability of Si_{As} defect formation should decrease with increasing the As_{ex} concentration. The most probable compensating acceptor centers in the Si-doped layers are the gallium vacancies that can be singly-, doubly, and thriply ionized (V_{Ga}^{1-}, V_{Ga}^{2-}, and V_{Ga}^{3-}). If in accordance with [25], we assume V_{Ga}^{3-} to be a dominating acceptor defect in *LT*-GaAs, the V_{Ga} concentration should be no lower than $3\cdot10^{18}$ cm^{-3} to compensate the Si donors with a concentration of $1\cdot10^{19}$ cm^{-3} observed for a high concentration of excess arsenic. Much the same concentrations of gallium vacancies in *LT*-GaAs are found in [27, 28] by the method of positron annihilation.

Thus, the experimental data show that the electrophysical and optical properties of *LT*-GaAs containing excess arsenic are mainly determined by As_{Ga} and V_{Ga} defects. As to interstitial arsenic As_i, the following facts point out to the formation of this defect: *a*) a favorable ratio between the covalent As (0.18 nm) and tetrahedral interstice (0.104 nm) radii in the GaAs lattice, *b*) a linear correlation between $\Delta a/a$ and [As_{ex}], and *c*) a difference beween the excess arsenic concentration measured by the x-ray spectroscopic method and the As_{Ga} concentration determined using optical absorption spectra. These concentrations are $3.3\cdot10^{20}$ and $1.2\cdot10^{20}$ cm^{-3}, respectively, at $T_g = 150$°C.

Negative ions with the concentration ~$3\cdot10^{18}$ cm^{-3} identified by the authors as interstitial arsenic (As_i^{1-}) were found in [28] by the method of positron annihilation. It is believed that this defect along with V_{Ga} can be responsible for the compensation of Si_{Ga} donors. However, because of the lack of reliable experimental data, the problem on the concentration and electrical activity of interstitial arsenic is to be investigated.

The effect of annealing on the *LT*-GaAs structure

Experiments show that post-growth annealing of *LT*-GaAs at 600°C for 10 min significantly changes the structure and properties of the layers. Transmission electron microscopy reveals arsenic clusters with an average size of ~7 nm and concentration of ~$(6–8)\cdot10^{16}$ cm^{-3} in the annealed samples [6]. The moiré strips in the electron-microscopic pattern indicate

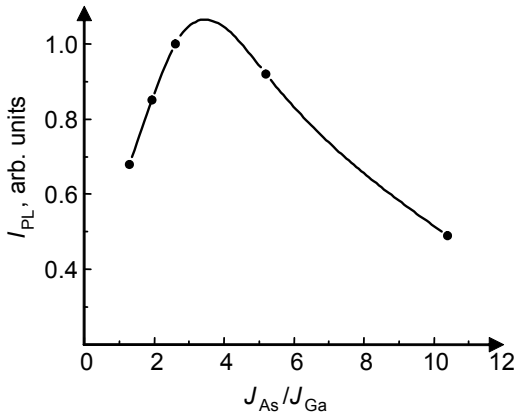

Fig. 5. Dependence of the 0.95 eV PL band intensity in the annealed GaAs samples on the flux ratio J_{As}/J_{Ga}.

that the clusters have an ordered crystalline structure (Fig. 5). The formation of As clusters is accompanied by a decrease in the *LT*-GaAs lattice deformation and its lattice parameter down to the value typical of stoichiometric GaAs ($\Delta a/a = 0$). In so doing, the antisite As_{Ga} defect concentration decreases by more than an order of magnitude. A significant increase in the free charge-carrier concentration after annealing is indicative of a decrease in the gallium vacancy concentration (Fig. 4). The electron concentration in the layers grown at high arsenic excess ($J_{As}/J_{Ga} \geq 3$) and low temperature (150–175°C) increases by 2–3 orders of magnitude after annealing. However, it remains much lower than the impurity concentration ($N_{Si} = 1 \cdot 10^{19}$ см$^{-3}$). Low values of the electron concentration and mobility ($n \leq 10^{17}$ cm^{-3}, $\mu \leq 500$ cm^2/(V·s)) are indicative of the fact that the annealed layers remain highly compensated, that is, the defects responsible for the compensation of Si_{Ga} donors are not completely annealed at 600°C. The high stability of non-equilibrium point defects can be due to the formation of stable complex defects consisting of the intrinsic point defects and impurity atoms, for example, the complexes Si_{Ga}–V_{Ga}.

The presence of these Si_{Ga}–V_{Ga} complexes is confirmed by measurements of photoluminescence spectra. The integral PL intensity is markedly increased after annealing, which can be due to the decrease in the concentration of defects being the centers of non-radiative recombination (As_{Ga}, V_{Ga}). The bands with maxima at 1.2 and 0.95–1.0 eV arise in the spectra of annealed samples. The 1.2 eV band is usually attributed to the complex Si_{Ga}–V_{Ga}. This band is the most pronounced in the PL spectra of layers grown at high temperatures ($T_g \geq \geq 200$°C) and low flux ratios ($J_{As}/J_{Ga} \leq 1{,}5$), i.e. at low arsenic excess. After annealing these layers, the electron concentration decreases (Fig. 4, curves *1* and *1′*), that is, the concentration of Si_{Ga}–V_{Ga} complexes increases. The nature of the emission band in the range of 0.95–1.0 eV has not been clearly identified. The intensity of this band in the annealed samples depends on the flux ratio J_{As}/J_{Ga} used while growing the layers (Fig. 5). This dependence is qualitatively similar to the dependence of the As_{Ga} defect concentration on J_{As}/J_{Ga} (Fig. 3). It can be assumed that the 0.95–1.0 eV band is related to the complexes including antisite arsenic, for example, As_{Ga}–V_{Ga}. Such complexes were earlier revealed in *LT*-GaAs by positron annihilation [27, 28].

Thus, annealing of *LT*-GaAs at $T = 600$°C results in the formation of excess arsenic clusters distributed over the layer volume. In so doing, the lattice deformation and the concentrations of the As_{Ga} and V_{Ga} point defects decrease, while the electrical activity of Si impurity increases. However, the annealing temperature 600°C is insufficient to completely activate the silicon impurity due to the formation of stable complexes consisting of the intrinsic point defects and impurity atoms (As_{Ga}–V_{Ga}, Si_{Ga}–V_{Ga}).

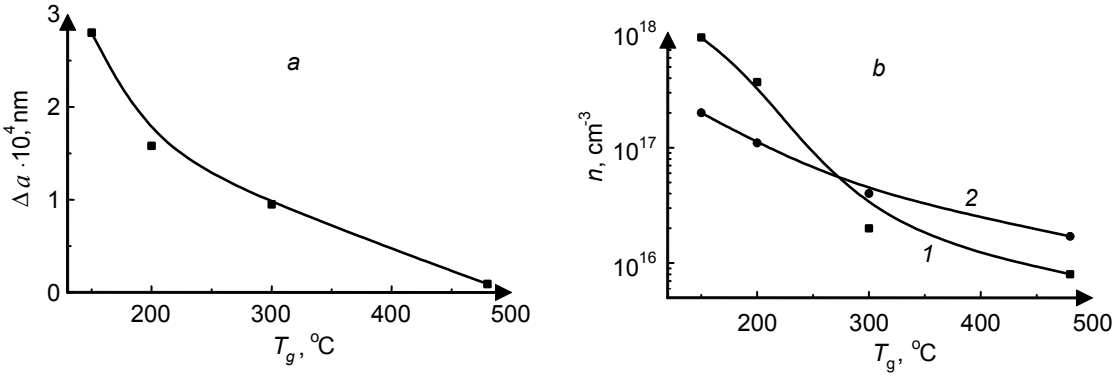

Fig. 6. The effect of growth temperature on the lattice parameter (*a*) and free charge-carrier concentration (*b*) in the InGaAs layers (*1 – as-grown*, *2* – after annealing).

THE STRUCTURE OF *LT*- InGaAs

Growth-surface structure

As in the case of GaAs, submicron growth pits are the typical growth-surface elements of InGaAs epitaxial films grown at low temperatures and flux ratios of $J_{As} / J_{III} > 1$ [9]. The pit density increases with decrease in temperature from 480 down to 150°C and increase in the arsenic flux ($1 < J_{As} / J_{Ga} < 20$) [7–9], that is, for both cases, with increase in the arsenic concentration in the adsorption layer. At low arsenic fluxes ($J_{As} / J_{III} \leq 0.1$), an excess concentration of the III-group elements (Ga, In) occurs on the *LT*-InGaAs surface, the Ga + In alloy drops of micron sizes are formed from the elements. As a result, two growth mechanisms are realized on different parts of the growth surface: vapour-crystal and vapour-liquid-crystal mechanisms. This causes formation of a morphologically non-uniform InGaAs film containing a lot of dislocations. As the arsenic flux increases in the range $0.1 < J_{As} / J_{III} < 1$, the liquid phase is broken to small drops, which is accompanied by a local decrease in the layer growth rate and appearance of typical pits on the surface [9]. The most uniform *LT*-InGaAs surface without defects is formed at the flux ratios $J_{As} / J_{III} = 1–3$.

Lattice deformation and point defects in *LT*-InGaAs

In epitaxial growth of the InGaAs solid solution, the ratio of the group III elements (In and Ga) was chosen so that the lattice parameters of the InGaAs film matched those of the InP substrate. The lattice mismatch ($\Delta a/a = (a_{InP} - a_{InGaAs})/a_{InP}$) measured for the samples grown at different conditions varies in the interval $(3–6)\cdot10^{-3}$ and increases with decreasing temperature and increasing the flux ratio J_{As} / J_{III} [8,9]. The diffraction peak half-width Θ is 24–30 seconds of arc for the samples grown at T_g = 480°C and increases up to the value 100 seconds of arc with decreasing temperature and increasing the flux ratio J_{As} / J_{III}. The maximum value Θ ≈ 400 seconds of arc is observed for the layers grown at the excess of group III elements ($J_{As} / J_{III} < 0.4$).

Figure 6 shows the change in the lattice parameter ($\Delta a = (a_{init} - a_{ann})$) after annealing of the InGaAs layers grown at different temperatures. It is seen that Δa increases with the decrease in T_g and is $3\cdot10^{-3}$ Å at T_g = 150°C. Assuming, by analogy with *LT*-GaAs, that the lattice parameter of *LT*-InGaAs changes after annealing due to certain redistribution of excess arsenic occupying mainly the antisite positions (As_{In}, As_{Ga}), we can estimate the antisite As_{III} defect concentration using Δa [8]. According to this estimation, the As_{III} concentration in the layers grown at T_g = 150°C is $8\cdot10^{19}$ cm^{-3}. As the temperature increases, [As_{III}] decreases. An increase in the flux ratio J_{As} / J_{III} results in an increase in the antisite defect concentration.

High concentration of As_{III} defects affects optical and electrical properties of *LT*-InGaAs. Low intensity of radiative recombination is typical of all *LT*-layers. In the PL spectra of *LT*-InGaAs, a weak edge band at 0.82 eV is observed. The intensity of this band decreases with decreasing growth temperature and increasing the flux ratio J_{As} / J_{III}, that is, with increasing the antisite arsenic concentration. The measurements of electrophysical properties show that all *LT*-InGaAs layers are of the electron-type conductivity. The free-electron concentration in the layers grown at T_g = 480°C equals $8 \cdot 10^{15}$ cm^{-3} and is determined by the background impurity concentration. With decreasing temperature, the electron concentration increases up to $1 \cdot 10^{18}$ cm^{-3} (Fig. 6*b*) and the electron mobility decreases by nearly an order of magnitude [8, 9]. An increase in the flux ratio J_{As} / J_{III} at T_g = 150°C results in a monotonous increase in the free charge-carrier concentration [9].

Since the layers were not doped during growth and the background impurity concentration was in no excess of $8 \cdot 10^{15}$ cm^{-3}, we can assume that the high electron concentration in *LT*-InGaAs is caused by intrinsic point defects, first of all by antisite arsenic As_{III}. The relatively shallow donor level E_c – 0.032 eV belongs to the defect As_{III} in the InGaAs solid solution [29, 30]. The dependences of the electron concentration on the growth conditions correlate with those for As_{III} defects: an increase in $[As_{III}]$ with decreasing temperature or increasing the flux ratio J_{As}/J_{III} is accompamied by an increase in the free charge-carrier concentration. This fact counts in favour of the electrical activity of the antisite As_{III} defect in *LT*-InGaAs. However, for all growth conditions, the electron concentration measured from the Hall effect is much lower than the antisite defect concentration estimated using the change in the lattice parameter ($n = 1 \cdot 10^{18}$ cm^{-3} and $[As_{III}] = 8 \cdot 10^{19}$ cm^{-3} at T_g = 150°C). This discrepancy can be due to a number of reasons:

1. A portion of the As_{III} donors is compensated by gallium vacancies or bound in ($As_{III} – V_{Ga}$) complexes. This is confirmed by the high compensation factor and low electron mobility of the *LT*-layers.

2. An estimation of the antisite defect concentration using Δa gives overestimated values. This is possible, if excess arsenic is located both in the group III element sites and interstitial positions (As_i) in the InGaAs lattice, and this was not taken into account.

Thus, the InGaAs layers grown at low temperature ($T_g \leq 300$°C) contain excess arsenic incorporated into the lattice mainly as antisite As_{III} defects. The As_{III} defect concentration increases with decreasing growth temperature and increasing the flux ratio J_{As}/J_{III}. A high free charge-carrier concentration caused by antisite As_{III} defects is typical of *LT*-InGaAs.

The effect of annealing on the *LT*-InGaAs structure

As in the case of *LT*-GaAs, clusters are formed in the film volume under annealing *LT*-InGaAs [8, 9, 13, 14]. The volume density and average diameter of clusters are $4…5 \cdot 10^{15}$ cm^{-3} and 10 nm, respectively, at annealing temperature 500°C.

The anneling of the InGaAs layers results both in the changes in the film volume and formation of thermal etch pits elongated along the <110> direction. In [31], the appearance of these pits is assumed to be due to selective etching of the two-dimensional arsenic precipitates located in the {111} planes of the film volume. However, our investigations show that these defects are located at the points where microtwin lamels outcrop onto the surface [13, 14].

After annealing of *LT*-InGaAs, the antisite As_{II} defect and, respectively, free charge-carrier concentrations decrease (Fig. 6*b*).

DISCUSSION

The regularities observed in the changes of the structure and properties of GaAs and InGaAs with decreasing growth temperature are similar and agree with the data published in the literature [17–20, 23–23, 29–32]. Growth of both materials at low temperatures ($T_g \leq 300$°C) and high arsenic fluxes ($J_{As} / J_{III} > 1$) results in the capture of excess arsenic, whose concentration increases with decreasing temperature up to the value 1.5 at. % at T_g = 150°C.

The incorporation of excess arsenic is accompanied by modification of the surface relief and internal structure of the GaAs and InGaAs layers. The most uniform surface without defects is observed for *LT*-GaAs and InGaAs layers grown at the flux ratio $J_{As} / J_{III} \approx 1$. Typical defects formed at increased arsenic fluxes are submicron growth pits. It can be assumed

that excess arsenic accumulating at the crystallization front at low temperatures [33] promotes the formation of stacking faults followed by the formation of growth pits at the intersection points of the stacking faults with the surface. The microstructure of the main part of the GaAs and InGaAs surface is formed by nano-islands, whose shape and size depend on the growth conditions. These islands result from the nucleation growth mechanism realized on the (001) surface.

Although the mechanisms of the excess arsenic incorporation and antisite defect formation in *LT*-layers were discussed in a number of works [16, 17, 34], they are still unclear. The As_{ex} incorporation is assumed to be due to the processes in the adsorption layer on the GaAs surface [16, 17]. With the decrease in the growth temperature and increase in the As_2 and As_4 fluxes, the surface coverage by adsorbed arsenic atoms and molecules increases. Since the As_2 molecules do not completely dissociate during the low-temperature epitaxial growth, they can be captured into the solid phase. Two-atomic arsenic molecules incorporated into the GaAs or InGaAs lattice can occupy two neighboring positions (As_{As}, As_{III}) giving rise to an antisite defect. Simultaneously, vacancies are generated in the group III element sublattice.

The point defects (As_{III}, V_{Ga}) formed as a result of the excess arsenic incorporation significantly affect the optical and electrical properties of *LT*-GaAs and InGaAs. These defects, being the centers of non-radiative recombination, considerably reduce the photoluminescence intensity. The antisite As_{III} defects determine the Fermi level position in *LT*-GaAs and InGaAs. High concentration of As_{III} defects causes shifting and finally pinning the Fermi level at a certain position. The deep donor levels ($E_c - 0.8$ eV) belong to the antisite As_{III} defects in GaAs. Therefore, the Fermi level is pinned near the middle of the band gap causing high specific resistance of undoped *LT*-GaAs layers. In *LT*-InGaAs, the antisite defects form relatively shallow donor levels and pin the Fermi level near the conduction band bottom causing reasonably high free-carrier concentration. The gallium vacancies present as simple defects (V_{Ga}) or complexes (Si_{Ga}–V_{Ga}, As_{Ga}–V_{Ga}) act as compensating centers.

During annealing, excess arsenic is precipitated in clusters. The formation of the As clusters is accompanied by a decrese in the point defect (As_{III}, V_{Ga}) concentration, which results in the corresponding change of optical and electrical properties of *LT*-GaAs and InGaAs.

CONCLUSION

The investigations show that GaAs and InGaAs grown by low-temperature MBE ($T_g \leq 300$°C) contain excess arsenic. The excess arsenic concentration depends on the growth conditions: growth temperature, As to Ga flux ratio, molecular form of As, and presence of doping impurities. The incorporation of excess arsenic results in the tetragonal distortion of the *LT*-layer lattice, change in the surface structure, and formation of As_{Ga}, As_i, and V_{Ga} point defects. The dominating point defect in GaAs and InGaAs with excess As is the antisite As_{III} defect. Because of high concentration, this defect exerts determining influence on the lattice parameter and optical and electrical properties of *LT*-layers. The growth conditions close to the stoichiometric ones ($J_{As} / J_{III} \approx 1$) make it possible to grow, at sufficiently low temperatures ($T_g \approx 150$°C), the *LT*-layers of GaAs and InGaAs with low defect concentration and the parameters close to those typical of the layers grown at conventional temperatures.

The authors thank their collegues A. K. Gutakovskii, A. E. Kunitsyn, B. R. Semyagin, M. A. Putyato, M. P. Yakubenya, S. E. Toropov, and S. V. Subach for fruitful cooperation.

This work was supported in part by the Russian Foundation for Basic Research, grant 05-02-16712a.

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