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ORIGINAL PAPER

Novel circuit design for content-addressable memory in QCA technology

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Abstract
The content-addressable memory is an especial memory cell that can search in its entire contents in one clock cycle. The Quantum-dot Cellular Automata (QCA) technology is also the promising nanotechnology for digital circuits implementation. This study presents and evaluates a new architecture for two-input XOR gate in the QCA technology. Then, the unique gate is developed using the developed XOR gate. The novel and efficient content-addressable memory is also developed using the developed unique gate. The QCADesigner tool is utilized to evaluate the functionally of these architectures. The implementation results prove that the developed content-addressable memory has 0.03 μm^2 area, 0.5 clock cycles, and 37 cells. The developed architectures provide advantages in comparison with other architectures in terms of area, latency, and cell count.

Keywords Nanotechnology · Nanoelectronics · Content-addressable memory · 2-input XOR gate · Quantum-dot cellular automata

1 Introduction

Nowadays, the traditional technologies such as CMOS technology have several drawbacks at Nano-scale. So, several kinds of nanotechnologies such as the CNTFET and the Quantum-dot Cellular Automata (QCA) are suggested for replacing these technologies [1–3]. The QCA technology is a new type of nanotechnology, which is used for digital circuits design [4–9]. There are several reported digital circuits implementation such as multiplexer circuits [10–14], counter circuits [15], full adder circuits [4, 16–21], shift register circuits [7, 22, 23], comparator circuits [24, 25], and memory circuits [5, 9, 26–29] in this technology. These implementation results demonstrate that digital circuits implementation in the QCA technology offer high-dense and high-speed circuits at Nano-scale [4–8]. So, this technology can be a promising technology for circuit design in non-transistor-based technology [16]. This new technology uses the QCA cell, which is constructed of 2 free electrons in 4 dots in square shape. Based on the columbic repulsion, 2 stable states are achieved in the cell [4–6, 8, 10, 15, 18–21, 30]. These 2 stable states can be utilized to determine the logic "0" and logic "1" in the digital circuits design [4–6, 11, 13, 18, 20, 21, 31].

On the other hand, the memory cell has an important role in digital circuits [29]. The Content-Addressable Memory (CAM) is an important kinds of memory cells for high-speed searching applications [32–35]. So, the QCA CAM circuit design is in the focal point of interesting research topics in the digital circuits design especially in digital computer circuits. There are several attempts to improve the performance of the QCA memory circuits design [5, 9, 26–29].

Walus et al. [28] had designed a 1-bit RAM that has 0.16 μm^2 area, 158 cells, and 2 clock cycles. Hashemi and Navi [26] had designed a 1-bit QCA D-flip flop and memory circuits that has 0.13 μm^2 area, 109 cells, and 1.75 clock cycles. Angizi et al. [5] had designed a 1-bit Majority Gate (MG)-based RAM that has 0.08 μm^2 area, 88 cells, and 1.5 clock cycles. Rasouli Heikalabad et al.

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[27] had offered a 1-bit content-addressable memory that has 0.14 μm^2 area, 100 cells, and 2 clock cycles. Sadoghifar and Rasouli Heikalabad [9] had suggested a 1-bit CAM that has 0.04 μm^2 area, 46 cells, and 0.5 clock cycles.

This study presents and evaluates a novel 2-input XOR gate in QCA technology. Then, a novel circuit is presented for unique gate in this technology. The novel and efficient 1-bit CAM are also developed using this novel circuit as building block. The QCADesigner tool version 2.0.3 is utilized for implementation of the designed circuits. These results confirm that the developed 2-input XOR gate requires 0.008 μm^2, 0.25 clock cycles, and 10 cells. The designed unique gate requires 0.01 μm^2 area, 0.5 clock cycles, and14 cells, and the developed CAM has 0.03 μm^2 area, 0.5 clock cycles, and 37 cells. The comparation results prove that the developed CAM has advantages compared with other CAMs.

This study outlines as follows: Section 2 introduces the background of the proposal circuits. Section 3 presents the developed QCA circuits. Section 4 presents the simulation results and comparation. Finally, the paper is concluded in Sect. 5.

2 Background

2.1 The QCA cell

The QCA cell is a building block in this technology, in which there are 4 dots and 2 free electrons in square shape cell. Fig. 1 displays a QCA cell [11, 30].

Based on the columbic reputation, two stable states are available in each cell. These states are utilized to show the logic "0" and logic "1" in digital circuits [7, 36].

2.2 The QCA gates

The QCA gates are building blocks for constricting the QCA circuits. There are three basic gates in this technology [6]: 1) Inverter Gate (IG), 2) MG, and 3) XOR gate [30]. Fig. 2 displays these basic gates [4, 30].

The MG output is indicated as M(A, B,C), where $M(A,B,C) = CA + BA + CB$. On the other hand, the inverter gate output shows the inverse value of the input, i.e., $IG(A) = \bar{A}$, where A denotes the input and the IG(A) denotes the output. The XOR output is XOR(A, B,C), where $XOR(A,B,C) = A \oplus B \oplus C$.

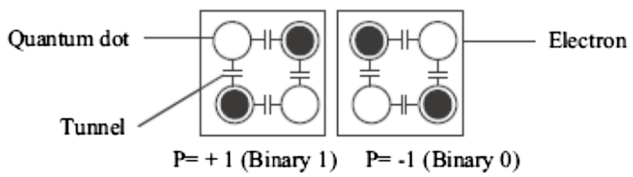

Fig. 1 The QCA cell structure [11]

2.3 The CAM circuit

The CAM is an especial kind of the memory cells that can search in its entire contents in one clock cycle. In this kind of memory, the stored data are accessed by searching for the content [33]. This kind of memory is suitable for high-speed purpose. As a result, several attempts [5, 9, 26–28] have been done to improve the circuits of memory especially this kind of memory.

Walus et al. [28] had described a 1-bit QCA Random Access Memory (RAM). Fig. 3 shows the described RAM in [28].

This memory has 158 cells, 0.16 μm^2 area, and 2 clock cycles.

Hashemi and Navi [26] had developed a 1-bit memory circuit that utilizes D-flip flops, and a multiplexer. This memory, which is shown in Fig. 4, has set/reset ability.

This memory has 0.13 μm^2 area, 109 cells, and 1.75 clock cycles.

Angizi et al. [5] had developed a 5-input MG. They had also suggested a 1-bit memory using this MG that is shown in Fig. 5.

This memory has 0.08 μm^2 area, 88 cells, and 1.5 clock cycles.

Rasouli Heikalabad et al. [27] had suggested a 1-bit CAM using a new 5-input minority gate that is displayed in Fig. 6.

Sadoghifar and Rasouli Heikalabad [9] had designed the 1-bit CAM that is shows in Fig. 7.

This CAM has 0.04 μm^2 area, 46 cells, and 0.5 clock cycles.

3 The designed architectures

3.1 The developed two-input XOR gate

Figure 8 displays the developed two-input XOR gate.

The developed circuit has 11 cells, 0.5 clock cycles, and 0.009 μm^2 area.

3.2 The proposed unique gate

To design the efficient content-addressable memory circuit, we utilize a unique gate that is defined based on the Eq. (1):

$$Q = (A \odot M) + S \tag{1}$$

Table 1 shows the desired operation of this unique gate.

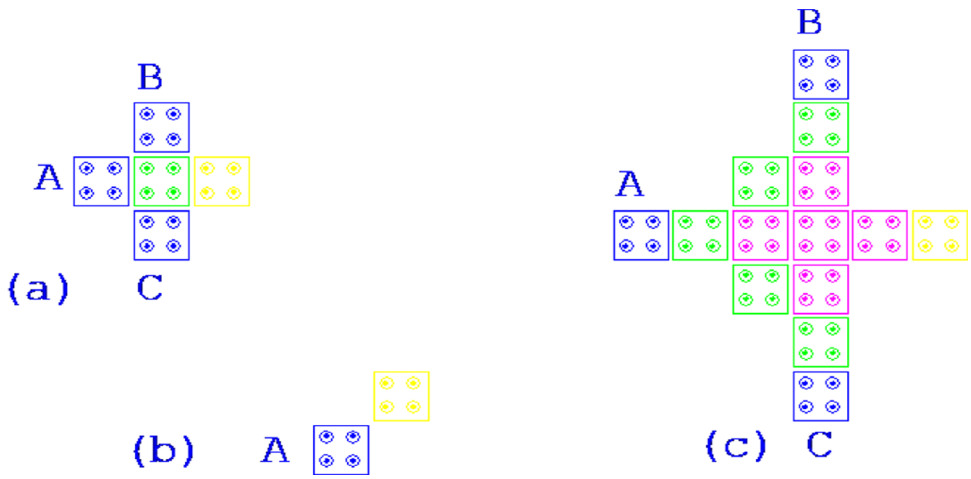

Fig. 2 The QCA gates: **a** Three-input MG, **b** IG, and **c** XOR gate [30]

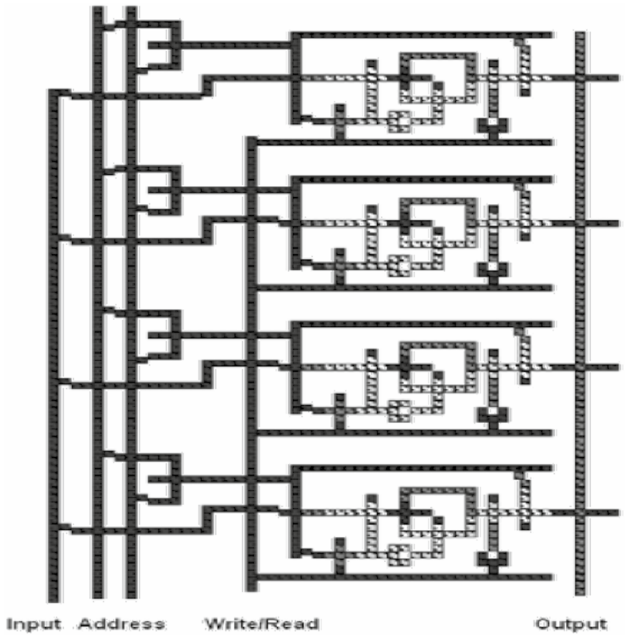

Fig. 3 The designed 1-bit QCA random access memory circuit in [28].

If S is “0” in Eq. (1), the output is equivalent to A⊙M. Otherwise, the output is equivalent to “1”. The proposed circuit for implementation of this equation is displayed in Fig. 9.

Based on Eq. (1), and Fig. 9, the proposed circuit for implementation of this equation contains the developed XNOR gate as building block, and one majority gate. This architecture has 0.01 μm^2 area, and 14 cells. This circuit is utilized for implementation of content-addressable memory as building block as described later.

3.3 The developed CAM

Figure 10 shows the developed CAM.

The proposed circuit for content-addressable memory required 0.03 μm^2 area, and 37 cells. The proposed circuit contains 2 components: the designed unique gate and memory unit. A control signal denoted by W/R controls the read and write operations in the memory unit. The developed unique gate's input, M, is shown as the output in this unit. Moreover, A and S are inputs in the suggested unique gate. The output of the developed content-addressable memory, which is also the unique gate output, is shown by Q. The output of the memory unit of the developed content-addressable memory is "1" when the control signal of the memory unit is "0". When the control signal of the memory unit is set to "1" the memory unit's output is "0" that means the read operation is performed. Furthermore, the output Q is "1" when the input S is "1" and the output Q is computed using the inputs M and A when the input S is "0".

4 The results and discussion

The accuracy of the suggested circuits is checked using QCADesigner tool version 2.0.3.

4.1 The developed two-input XOR gate

Figure 11 displays the implementation results of the designed two-input XOR gate. For implementation, the Bistable approximation engine is utilized.

The implementation results of the designed XOR gate in comparison with other XOR gates are summarized in Table 2.

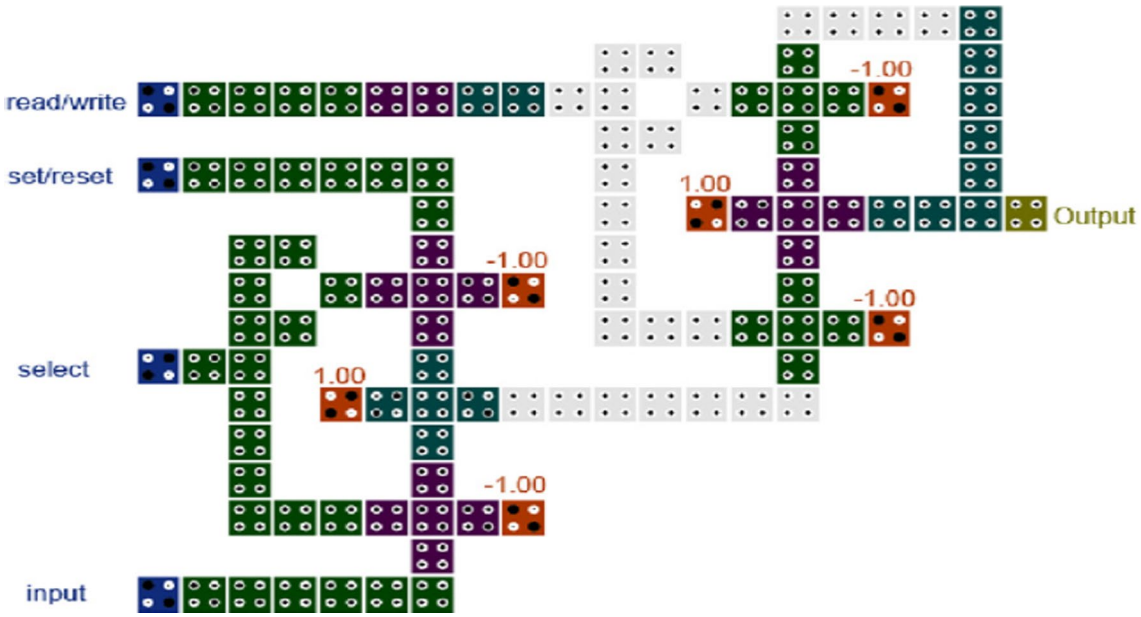

Fig. 4 The suggested QCA memory in [26]

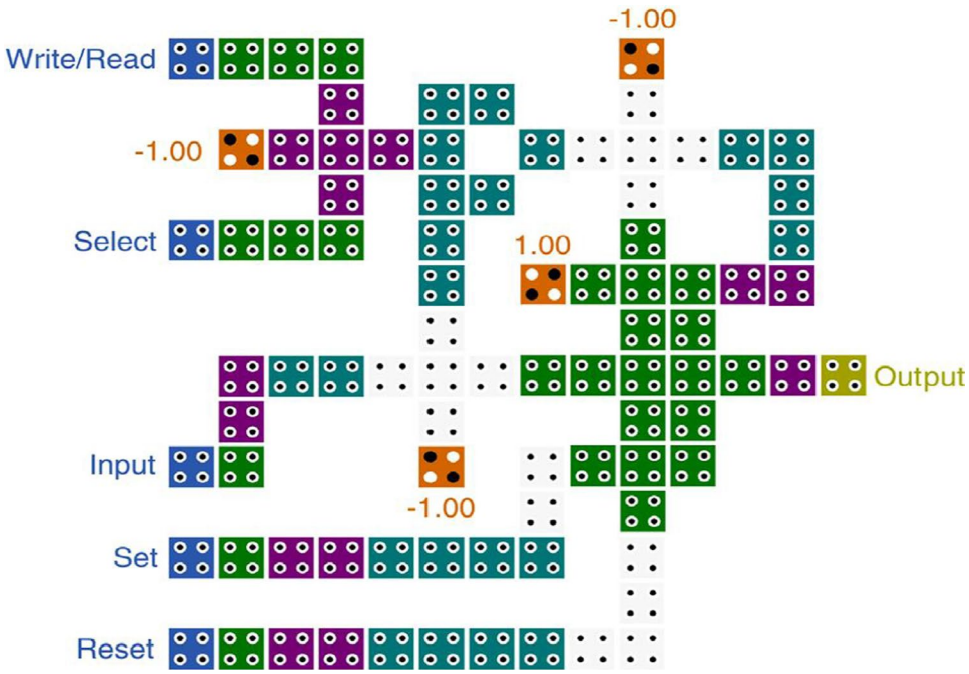

Fig. 5 The suggested 1-bit memory in [5]

Based on our results, the designed QCA XOR gate has advantages compared with other XOR gates in [31, 37–40] regarding area, cell count, and cost. For example, the designed 2-input QCA XOR gate provides improvements by about 25%, 21%, and 25% in comparison with that gates presented in [40] with regard to area, cell count, and cost, respectively.

4.2 The developed unique gate

Figure 12 illustrates the implementation results of the developed unique gate.

The simulation results prove that the functionally of the proposal unique gate is valid. In addition, these results show that the designed unique gate circuit requires 0.5

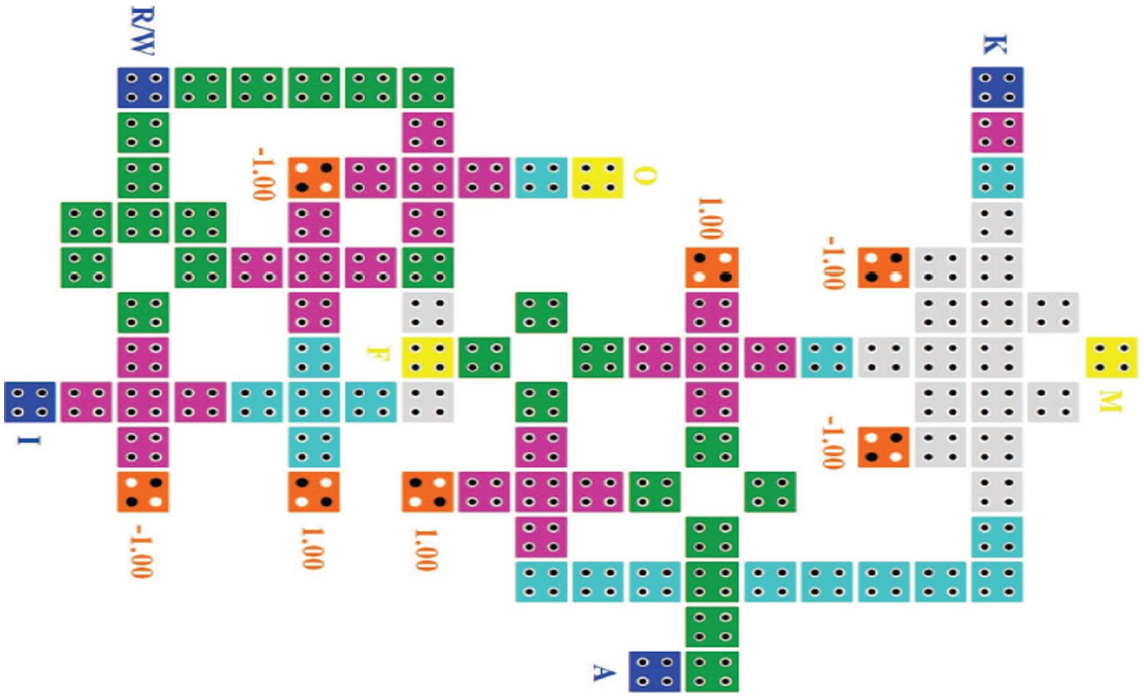

Fig. 6 The developed 1-bit CAM in [27]

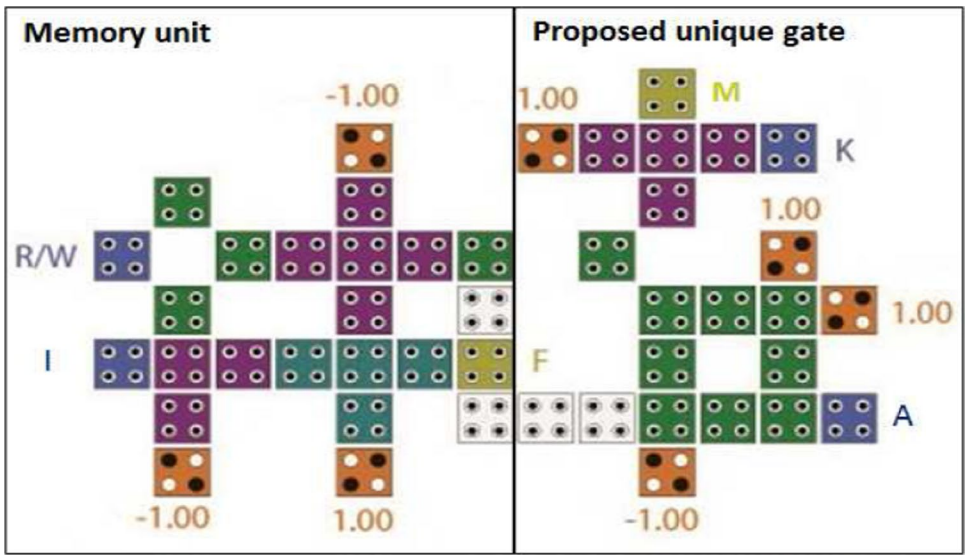

Fig. 7 The suggested 1-bit CAM in [9]

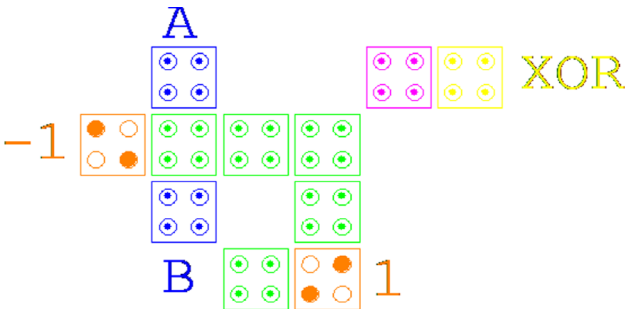

Fig. 8 The developed two-input XOR gate

Table 1 The operation table for the suggested unique gate

S	M	A	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	X	X	1

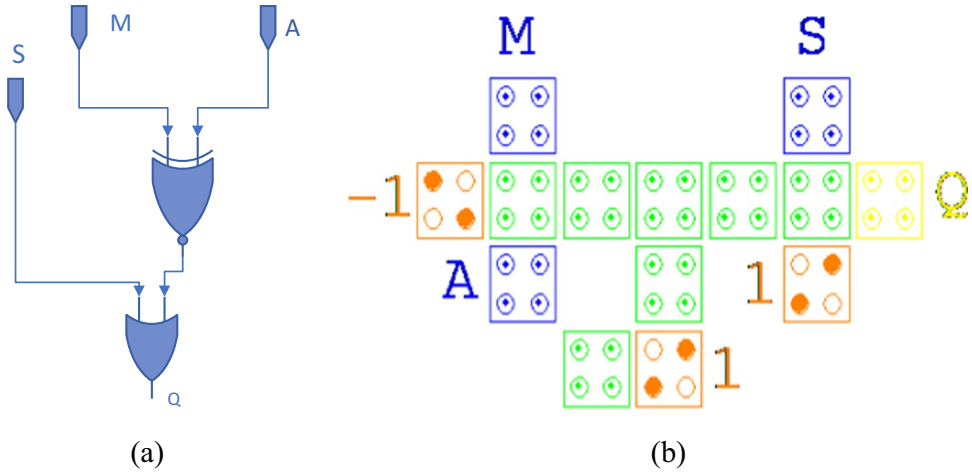

Fig. 9 The developed unique gate **a** logic diagram, **b** QCA layout

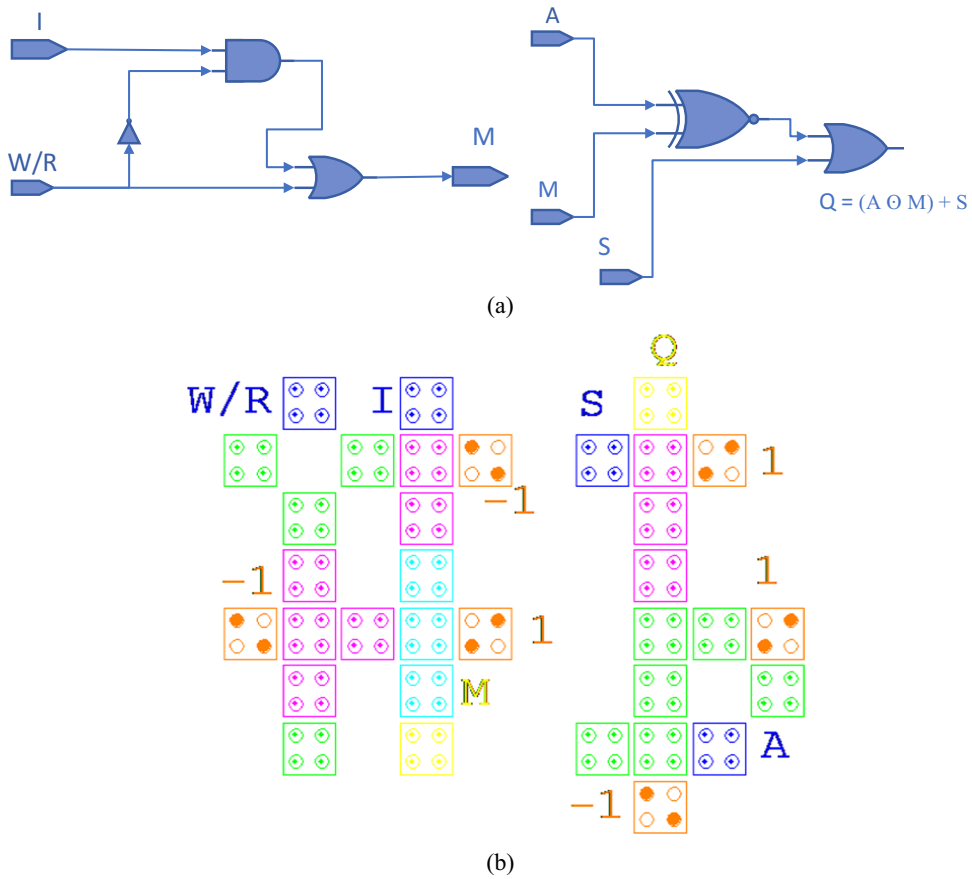

Fig. 10 The suggested content-addressable memory **a** logic diagram **b** QCA layout

clock cycles. The implementation results of the unique gates are summarized in Table 3.

Based on these results, the suggested unique gate has benefits regarding area, cell count, and cost compared to that design in [9]. The developed unique gate has 67%, 33%, and 67% improvements regarding area, cell count, and cost, respectively, in comparison whit that design in [9].

4.3 The suggested content-addressable memory

Figure 13 displays the implementation results of the suggested content-addressable memory.

The implementation results demonstrate that the functionality of the developed CAM is valid. Furthermore, the developed content-addressable memory requires 0.5 clock cycles. Table 4 summarizes the implementation results of the CAM circuits.

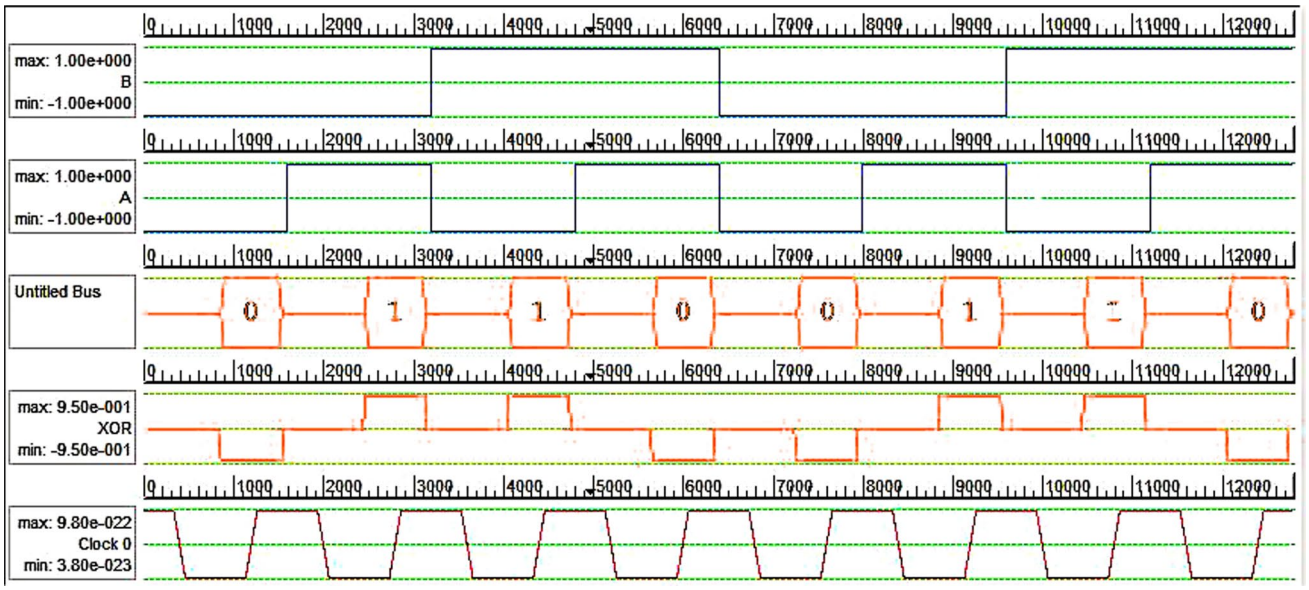

Fig. 11 The implementation results of the suggested XOR gate

Table 2 The comparative table for two-input XOR gates

Ref	Cell count	Latency (Clock Cycle)	Area (μm^2)	Cost = Area*Latency (clock cycle)
[37]	60	1.5	0.09	0.135
[31]	54	1.5	0.08	0.12
[38]	67	1.25	0.06	0.075
[39]	29	0.75	0.03	0.0225
[40]	14	0.5	0.012	0.006
This paper	11	0.5	0.009	0.0045

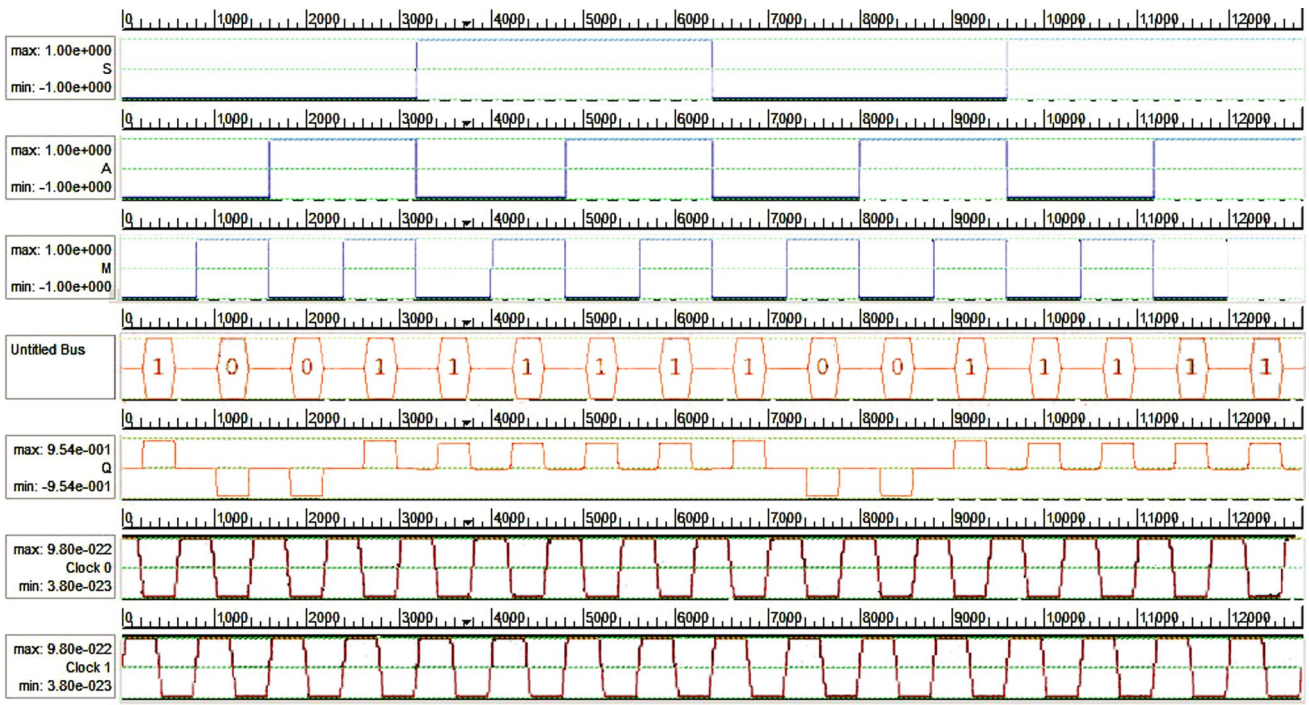

Fig. 12 The implementation results of the designed unique gate

Table 3 The implementation results of the unique gates

Ref	Cell count	Area (μm^2)	Latency (Clock Cycle)	Cost = Area*Latency (clock cycle)
[9]	21	0.03	0.5	0.015
This paper	14	0.01	0.5	0.005

Table 4 The implementation results of the CAM circuits

Reference	Cell count	Latency (Clock Cycle)	Area (μm^2)	Cost = Area*Latency (clock cycle)
[28] (RAM)	158	2	0.16	0.32
[26] (RAM)	109	1.75	0.13	0.227
[5] (RAM)	88	1.5	0.08	0.12
[27] (CAM)	100	2	0.14	0.28
[9] (CAM)	46	0.5	0.04	0.02
This paper (CAM)	37	0.5	0.03	0.015

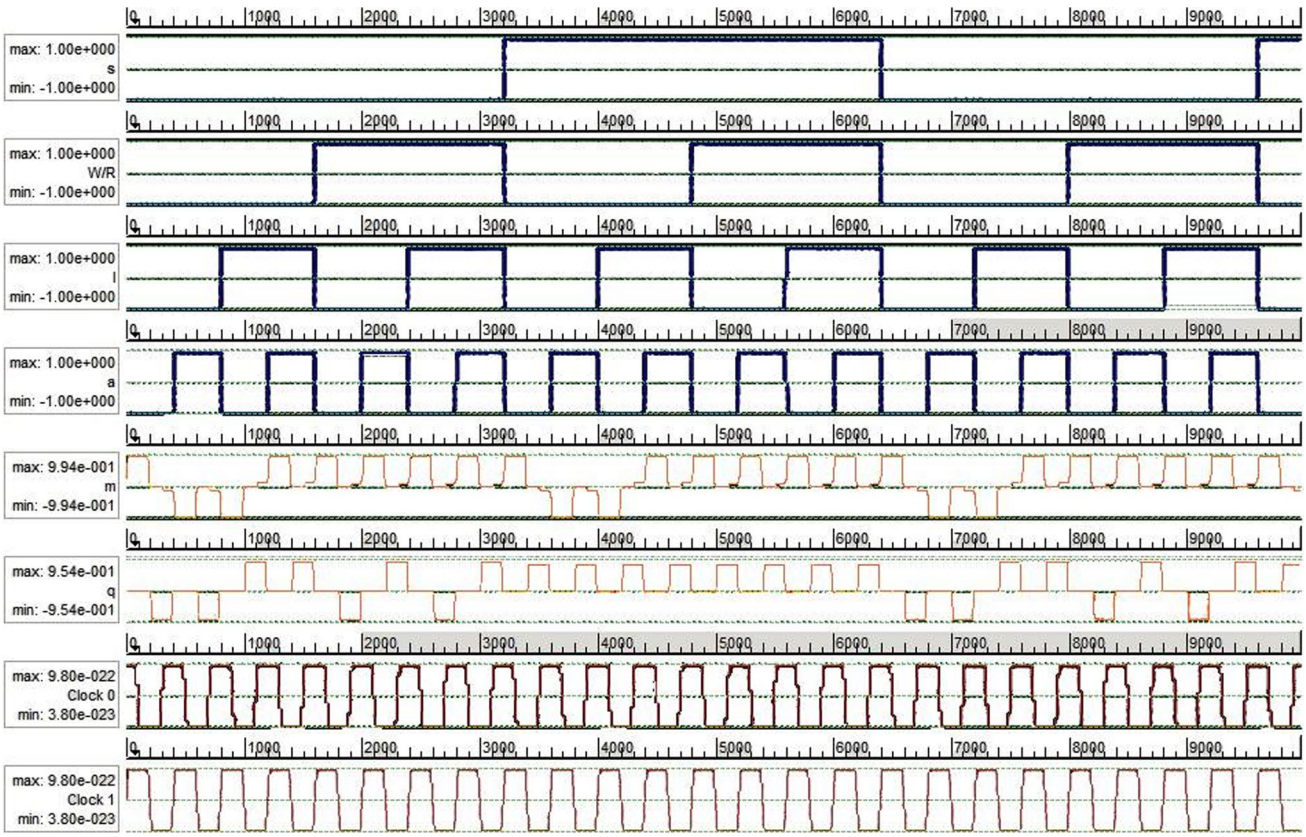

Fig. 13 The implementation results of the suggested CAM

Based on these results, the designed content-addressable memory has benefits regarding area, cell count, and cost in comparison with [5, 9, 26–28]. The proposed content-addressable memory has 25%, 20%, and 25% improvements compared to that design in [9] regarding area, cell count, and cost, respectively. It should be noted that although the QCA technology overcomes the drawbacks of the traditional technologies such as CMOS technology, this technology also introduces

new ones. Based on the research [41], a QCA cell's intrinsic switching time is on the order of terahertz. The real speed may be significantly lower, in the order of gigahertz and megahertz for molecular QCA and solid state QCA, respectively.

5 Conclusion

The QCA technology is the promising type of nanotechnology for the digital circuits' implementation. The CAM is also an especial type of memory cells that is suitable for high-speed searching applications. As a result, the implementation of efficient CAM circuit is interesting for researchers. This study investigated, presented and evaluated the novel QCA CAM circuit based on the novel unique gate and novel XOR gate that were developed in this study. The suggested QCA circuits were evaluated in the QCADesigner tool version 2.0.3. The implementation results proved that the suggested QCA CAM has 37 cells, 0.03 μm^2 area, and 0.5 clock cycles. The comparison results demonstrated that the developed QCA circuits provided benefits compared to other QCA circuits with regard to area, cell count, and cost.

Declarations

Conflict of interest The authors stat that there is no conflict of interest.

Data availability The datasets are available from the corresponding author on reasonable request.

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