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ORIGINAL PAPER

Designing a three-level full-adder based on nano-scale quantum dot cellular automata

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Abstract
Some of the vital problems around the conventional CMOS technology are leakage-power consumption, physical-scalability limits, and short-channel effects. These deficiencies have led to many studies about nano-scale designs. Quantum dot cellular automata (QCA) is a potential answer in nanotechnology. Scholars have considered the four-dot squared cell as the main factor in the QCA. Also, a full-adder is a fundamental unit in every digital system. However, the importance of cell and area consumption limitation in circuit designing has been completely ignored in most of the related studies. Therefore, in this paper, we have offered a one-bit multi-layer full-adder cell. The practical accuracy of the proposed circuits has been assessed using QCADesigner. According to the obtained results and the design, the presented design has efficient cell usage against all the prior designs regarding cell counts and area occupation, leading to around 7% improvement in cell number than the common full-adder design. The simulation outcomes have also shown that the introduced design has excellent efficiency regarding cell and area aspects.

Keywords Quantum dot cellular automata · Full-adder · QCA · Nanoelectronics

1 Introduction

The present silicon-based technology encounters many important challenges and problems, reducing its ability as a low-power method for the future [1, 2]. High energy consumption, large-parametric variations, and decreased-gate control are the main problems, noticeably limiting the design of low-power and robust systems [3]. Hence, the researchers are investigating many new technologies such as nanowire transistors [4], single-electron transistors (SET) [5], and quantum dot cellular automata (QCA) [6–9] as the possible substitutions for the conventional silicon-based technologies [10]. The QCA, as newly emerging nanotechnology, is very interesting for performing the future energy-efficient digital systems, leading to low-power consumption, high-speed operation, and a dense structure [11–13]. This technology provides a nano-scale answer and suggests a new high-speed computation technique [14–17]. It has four quantum dots (made of ordinary semiconductive materials [18]), each of which has two free electrons [19–21]. Logic operations are accomplished via the QCA. The flow of data occurs in the circuit through the Coulombic interaction of the electrons [22]. Its structure is an array of quantum cells [23–25]. Instead of ordinary charge flow, the polarization effect has been used [26–28]. A three-input majority gate, wire, and inverter are the three key components commonly applied to the QCA [29–31].

Up to now, many QCA-based designs have been offered, but arithmetic circuits could be more attractive among all of them because of their extensive use in numerous applications [32–34]. The performance of the full-adder directly influences the performance of the whole system because it is the main element of arithmetic circuits [35]. Enhancing the efficiency of the adder is vital for improving the performance of the entire system [36, 37]. Therefore, designing QCA-based adder circuits with less complexity, a small area, and less delay is going to be a highly needed desire in the future [38]. Also, making QCA gates having low-power consumption has recently become more vital [39].

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The main purpose of this research is to suggest a QCA-based full-adder design based on three-level cell placement. A new QCA-based full-adder has been proposed for outperforming the previously presented adders regarding the area, cell count, and delay. Concisely, the goals are as follows:

- Offering a three-level design for one-bit QCA-based full-adder;
- Decreasing the cell number in one-bit QCA-based full-adder;
- Decreasing the consumption area of one-bit QCA-based full-adder;
- Comparing the complexity of the presented design with other recently proposed designs.

The structure of the article is as follows: Part 2 provides an overview of the QCA technology and the related works. Part 3 presents a new model for the full-adder and its basic structures plus the operation of the preceding ones. Part 4 presents the simulation results. Finally, the last section provides conclusions and future work.

2 Background and related work

Here, we have reviewed the previous studies to better comprehend QCA technology's architecture and its impact on designing the full-adder.

2.1 Fundamentals of QCA

Lent, et al. [19] presented the QCA as a possible nano-scale technology to design logical devices. Various researchers have worked on developing new ideas for this technology. The QCA cell is a container with a limited number of dots distributed along the cell perimeter, where two charged particles can occupy these dots [40]. The arrangement of cell dots is such that the cell identifier can only have two stable states (or mechanical ground states) [41]. The cell has two polarizations to signify logic "0" and logic "1." Figure 1a shows the switching between two states, performed by mechanically enabling the charged particles to tunnel among the dots. Figure 1b indicates that the QCA cells can have two different statuses (+1 and −1). Information is exchanged between one cell and its neighboring cells as a result of the Coulombic interaction. It is just needed to force the input cell to a specific polarization, and the cell will force the adjacent cell to the same polarization. The information is carried across a wire of adjacent cells, as shown in Figs. 1c and 2 [42].

A major logic gate in the QCA is a three-input majority gate shown in Fig. 3a. As a result of electrostatic repulsion,

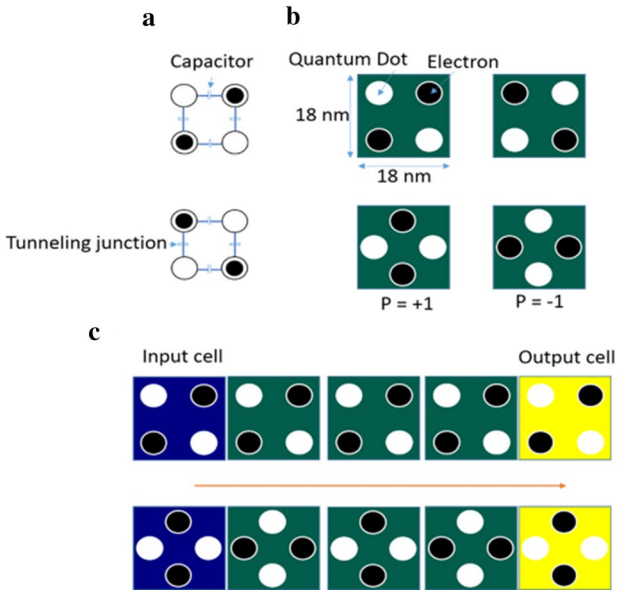

Fig. 1 The QCA cells; **a** functional diagram, **b** available cell types, and **c** QCA wire types [42]

the majority gate's central cells stabilize the polarization of the output.

We can attain an AND/OR gate by setting the polarization of one input of the majority gate to logic "1" or "0." When "0" is assigned to one input, the majority gate runs similar to the AND of the 2 other inputs. At the same time, if "1" is assigned to one input, the majority gate runs similar to the OR of the 2 other inputs. For instance, if the output is "1," then at least two inputs with logic "1" are needed. We can configure a majority gate to operate as an AND/OR gate. To reach this aim, we have set one input to $p=-1$ or $p=+1$ to have an AND or an OR, correspondingly. Figure 3b indicates the majority gate's function as a two-input OR gate, and Fig. 3c shows its function as a two-input AND gate.

In addition, the scientists have theorized an ideal and reduced organization for the five-input majority gate [45] to improve the area in the QCA-based 3-input majority gate compared to silicon-based technologies. The ideal design for a full-adder cell based on the 5-input majority gate has five gates: 3-input majority gates and two inverters. Up to now, many executions of a 5-input majority gate have been described [32, 46]. Figure 4a shows that it is not possible to access the input cells (B and C) through a solo level in the 1st QCA layout. Figure 4b shows another structure that other cells surround the output cell. Furthermore, the creators of 2 new architectures (Fig. 4c, which is presented in [47], and Fig. 4d, which is given in [46]) have tried to solve the mentioned shortcomings by suggesting a new device.

In QCA technology, there are four phases for the clock signal in the QCA circuit to ensure that the state switching is not abrupt but adiabatic. Due to the fact that in

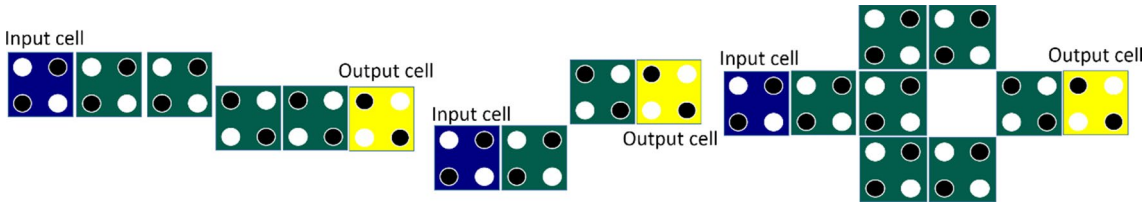

Fig. 2 The QCA inverter gates [43]

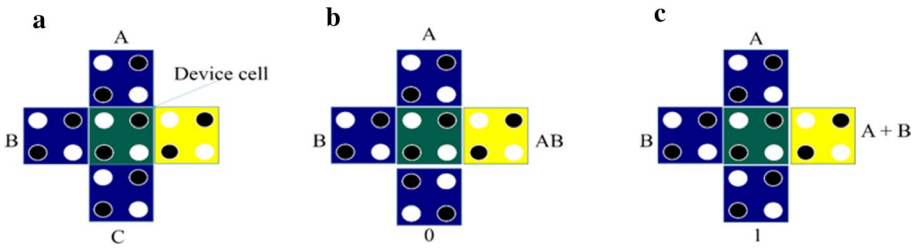

Fig. 3 **a** Three-input majority gate, **b** two-input OR gate, and **c** two-input AND gates [44]

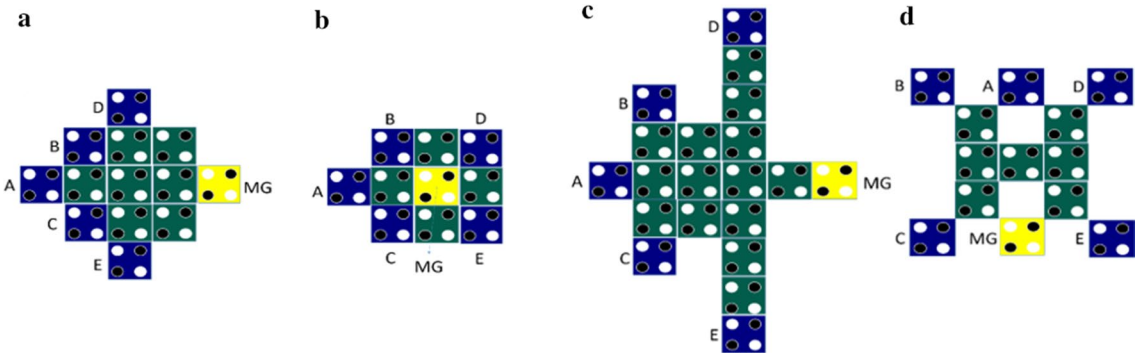

Fig. 4 The five-input majority gate; **a** the structure presented in [48], **b** the structure presented in [49], **c** the structure presented in [42] and **d** the structure presented in [42]

the sudden switching, the input is suddenly changed and attempted to relax in a ground mode using dissipating energy, the relaxation is uncontrolled and inelastic. So, it is probable that the circuit enters a metastable state determined by the local ground mode, not by the global one. The Landauer [50] and Bennet [51] clocking signals are two types of clocking signals commonly used for clocking the QCA circuits. Magnetic cellular automata (MCA) is a kind of QCA, where neighboring single-domain nanomagnets are responsible for the process and propagate the information through mutual interaction. Kumari and Bhanja [50] have proposed a spatially moving Landauer clocking design for MCA arrays. Figure 5 shows the Landauer clock waveform. Each clock signal has 4 steps: Switch, Hold, Release, and Relax. The Switch phase lasts until the full polarization of the cell. When the clock gets to the Hold step, the cell preserves its polarization. Finally, the cell becomes un-polarized at the low level of the clock (the Relax step).

Finally, in the QCA structures, making connections between components should be done efficiently to have better stability. Wire crossing is an essential factor in the QCA design to reach the mentioned goal. So far, three crossing methods have been suggested, having single-layer (Fig. 6a), multi-layer (Fig. 6b), and logical crossing (Fig. 6c) [42], respectively.

2.2 Related work

Up to now, great attempts have been made in different studies to show an efficient and simple model for one-bit full-adder cell; most of them have used a 3-input majority gate. The latest models have been studied in the following.

Navi, et al. [6] have introduced a five-input majority gate model, needing only two majority gates and two inverters implemented through diagonal cells. The full-adder design has been contrasted to the previous one based on complexity, area, and latency. The suggested adder has a

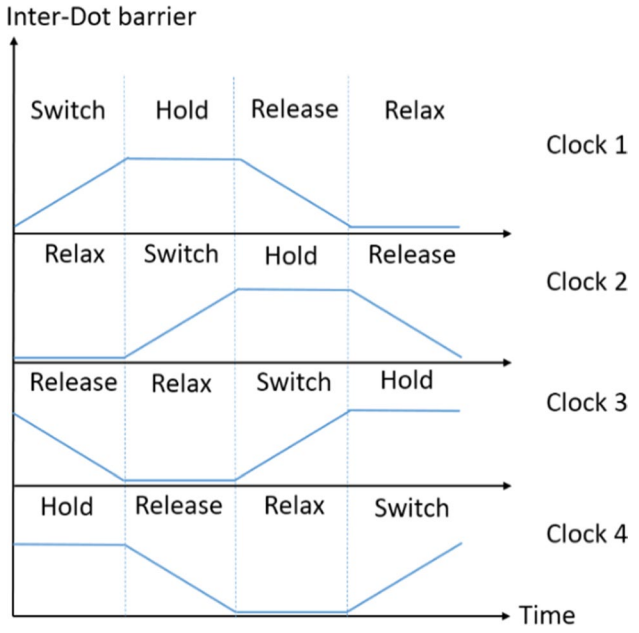

Fig. 5 The Landauer clock waveform [50]

good architecture, helping the upcoming arithmetic QCA-oriented circuit models. The suggested device has decreased cell counts and area, using a traditional type of QCA cells. The proposed design has a more straightforward structure and requires fewer cell counts and area than the previous designs, though it has an equal latency. Also, the proposed design of majority gates and full-adder has improved the designing of logical circuits.

Also, Molahosseini, et al. [32] have presented a simple 5-input majority gate for QCA full-adder. It is powerful regarding the implementation of digital functions. We can decrease the hardware request for a QCA model using gates like those. The circuit optimizes the number of gates, and clock steps, too. The challenge with this approach is the coupling problem among cells with other circuits. Some physical evidence has been presented to confirm the performance of the suggested device. QCADesigner has been applied to check the thorough functionality of the full-adder via computer simulations. The simulation results and physical relations have confirmed the usefulness of the design.

Also, Sayedsalehi, et al. [52] have proposed a model for the QCA-oriented full-adder. The increase of the carry signal through full-adder cells has been considered as the key cause of delay in the adder circuits. The full-adders have been suggested with the purpose of limiting the effect of the carry dissemination delay. This method has some benefits over some other methods: simple and efficient outline leading to very few gates, small zone, and less delay. QCADesigner tool has been employed to simulate the circuits for checking their functionality. We have shown the advantage of the introduced design compared to the current adders regarding gate counts, area, and latency.

Also, Navi, et al. [53] have proposed a configurable QCA circuit to do numerous logic functions like the AND and OR. The consumed hardware for a QCA model can be decreased, and numerous functions can be achieved through these kinds of circuits. Also, an efficient QCA design has been proposed as a full-adder, according to the designed circuits. They have also juxtaposed the proposed model with the preceding ones. The adder has excellent efficiency in terms of complexity, latency, and size.

Abedi, et al. [54] have presented a coplanar QCA-based crossover architecture for full-adders to decrease QCA cells

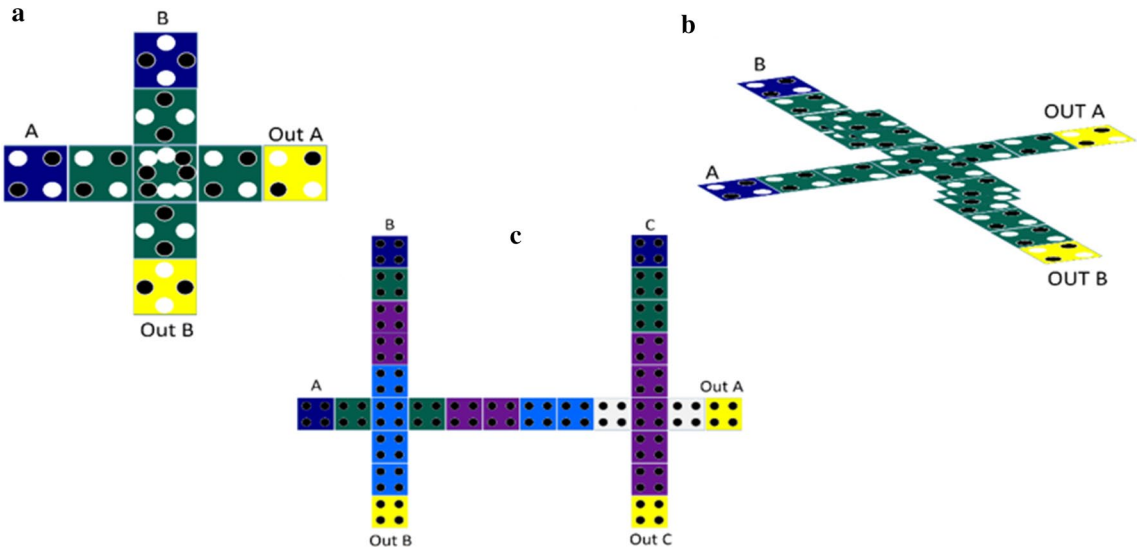

Fig. 6 The wire crossing. **a** Single-layer, **b** Multi-layer wire, and **c** Logical crossing [42]

and area consumption. The crossover has employed non-adjacent clock areas for 2 crossing wires. According to the obtained results, the enhancement is 23% and 48% for cell counts and the area, respectively, compared with that of the presented QCA-based design. The suggested QCA-oriented full-adder has been employed in designing QCA-based ripple carry adders, in which 17–41% advance in cell numbers and 22–69% in area occupation have been obtained compared with those of the previous ripple carry adder. The design cost is lower than that of the preceding QCA-oriented adders, according to the QCA-specific cost measurement, counting those with carry accelerating techniques.

Finally, Sarmadi, et al. [55] have suggested an improved one-bit full-adder relying on the QCA technology with six active layers. All the previous designs can be affected by the presented one-bit full-adder regarding cell numbers and area consumption. Six active layers in a creative approach have been employed to offer the correct functionality and the least viable occupation area using this circuit, resulting in keeping the suggested full-adder's size equal to a five-input majority gate. The complexity of the top layer and the cost of insinuation are the disadvantages of the proposed technique.

3 Proposed design

Here, we have introduced a novel QCA-oriented full-adder with a five-input majority gate [5, 15]. The structure of its cells follows the schematic design of Fig. 7. The operation of the design is shown in Fig. 8, which can be represented by:

$$\text{Carry} = \text{Maj3}(\text{A}, \text{B}, \text{C}) \tag{1}$$

$$\text{Sum} = \text{Maj5}\left(\text{A}, \text{B}, \text{C}, \overline{\text{Carry}}, \overline{\text{Carry}}\right) \tag{2}$$

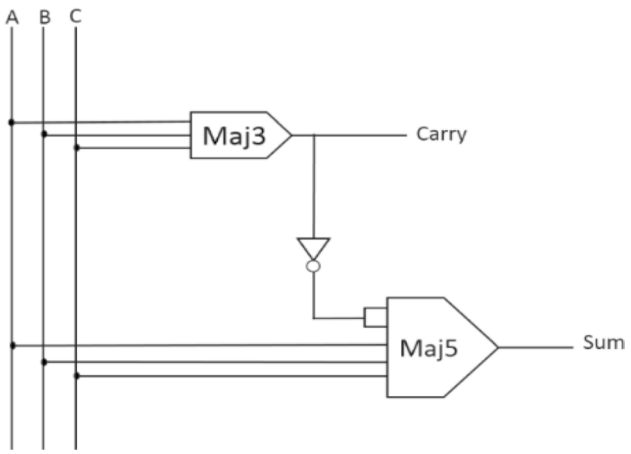

Fig. 7 The schematic of a one-bit full-adder cell [28, 56]

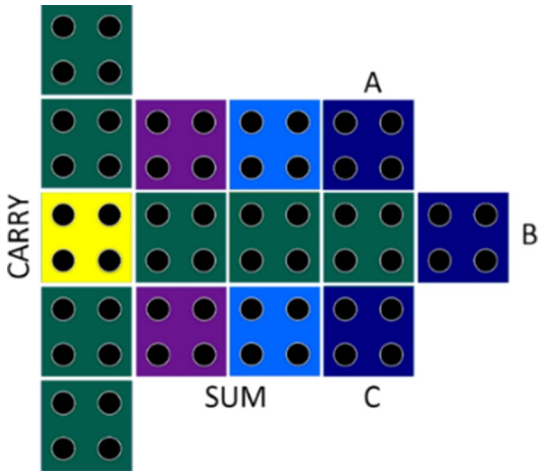

Fig. 8 The outline of the introduced QCA-based full-adder

The suggested full-adder design has been structured for proposing a high-speed adder to decrease the carry dissemination delay in bigger models. The proposed full-adder has 2 separate blocks, according to Fig. 8. The first block is a 3-input majority gate and produces the C_{out} signal. The other block contains a five-input majority gate and an inverter and produces the *Sum* signal. Each block has been managed at a different level. So, in the upper layer, C_{out} has been generated and transferred to the primary layer. The *Sum* signal has been generated by feeding the inputs and C_{out} to a 5-input majority gate.

Figure 9 shows the final layout views of the full-adder, according to the 5-input majority gate. This design has been managed in three layers to optimize the hardware requirements, the number of cells, and area occupation. The n-bit adders can also be implemented simply using this block.

Figure 10 shows the design, cell outline, and clock phases of the proposed adder. The first level has 3 inputs (*A, B, C*) and 1 output (*Carry*). The carry has been generated by means of three-input majority gate and directly sent to the

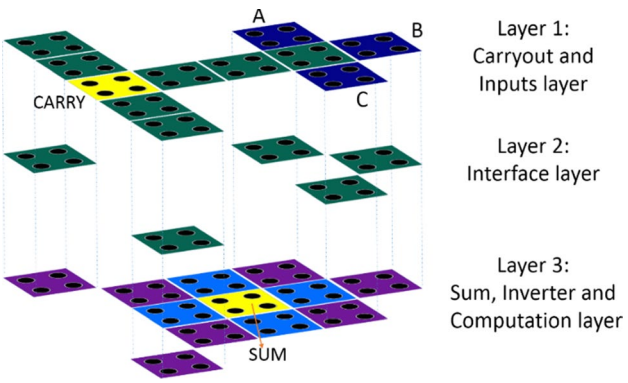

Fig. 9 The proposed one-bit full-adder cell in three different layers

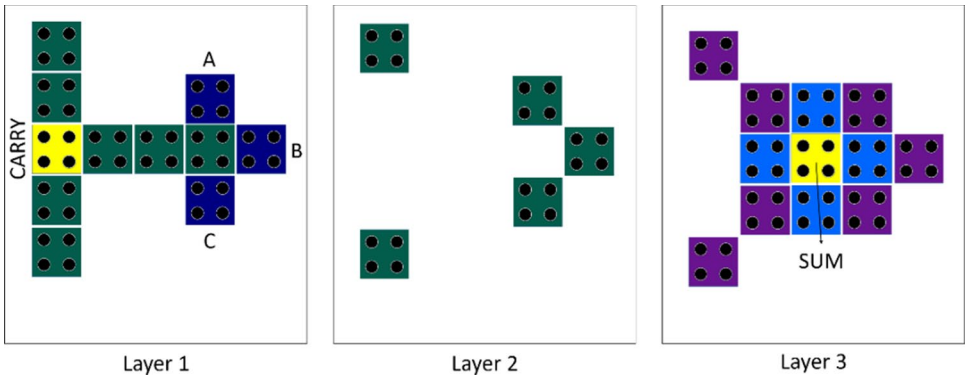

Fig. 10 Three diverse levels of the introduced QCA-oriented full-adder

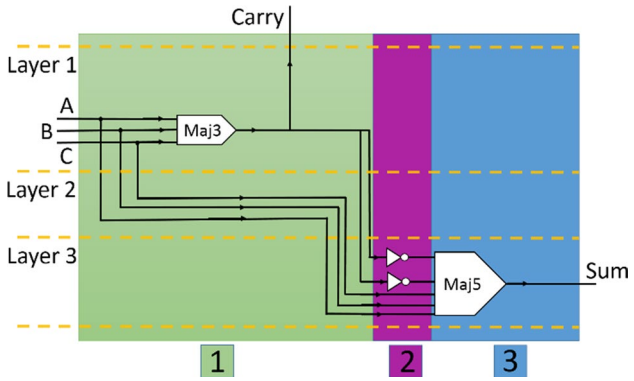

Fig. 11 The needed 4-step clock signals of the full-adder

Table 1 The truth table of full-adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

output (*Carry*). As *SUM* has been fed into the 5-input majority gate, we have needed an added clock step to have a steady throughput. Therefore, three clock phases are needed for producing the outputs, as shown in Fig. 11. Also, Table 1 shows the truth table of the one-bit full-adder circuit.

4 Simulation results

The introduced full-adder has been simulated via QCADesigner 2.0.3 [57]. This section provides a brief discussion about the simulation tools, accuracy analysis, and the simulation results.

Table 2 QCADesigner parameters for bistable approximation engine

Parameter	Value
Cell size	18 * 18 nm^2
Radius of effect	65 nm
Relative permittivity	12.9000000
Clock high	9.8e–22 J
Clock low	3.8e–23 J
Clock amplitude factor	2.000000
Clock shift	0.000000e + 000
Layer separation	11.5000 nm
Maximum iterations per sample	100
Number of samples	12,800
Convergence tolerance	0.001000

4.1 Simulation tool and parameters

Circuit creators need a swift and exact tool for simulating and designing to explain the performance of the QCA circuits. They can design a QCA circuit using QCADesigner among a set of CAD tools. QCADesigner is helpful in generating a fast and exact simulation and outline tool for QCA. The simulation of the QCA circuits has been done by QCADesigner [57]. The proposed full-adder and 3-input majority gate are simulated using the QCADesigner 2.0.3. The simulation engines are set to "Bistable Approximation" type as shown in Table 2. Also, the applied coherence vector parameters are shown in Table 3 [57].

4.2 Accuracy analysis

The simulation outcomes for the suggested one-bit full-adder are depicted in Fig. 12. The results for all combinations of the inputs (marked with the blue rectangle) are shown in Fig. 12. Based on the results, the suggested design is accurate, and the introduced QCA-oriented full-adder design outperforms the other ones. The first CARRY and SUM signals (marked with the red rectangle) waveforms have been

Table 3 QCADesigner parameters for coherence vector engine

Parameter	Value
Cell size	18 * 18 nm^2
Radius of effect	80 nm
Relative permittivity	12.9000000
Clock high	9.8e–22 J
Clock low	3.8e–23 J
Clock amplitude factor	2.000000
Clock shift	0.000000e+000
Layer separation	11.5000 nm
Maximum iterations per sample	–
Number of samples	–
Convergence tolerance	–

obtained after 0.25 and 0.75 clocking cycles (marked with the black rectangle), correspondingly.

4.3 Comparisons

Table. 4 shows four parameters of full-adders designs introduced in the related studies alongside the proposed design. The progress of the design is significant concerning the number of cells (intricacy) and the area. We have used 28 QCA cells in the introduced model. The area of the total plan has also been decreased in the proposed design. The delay is three in the proposed design, which is the minimum clock phase. Therefore, the introduced design has improved the area consumption and delay. Also, the configuration of the

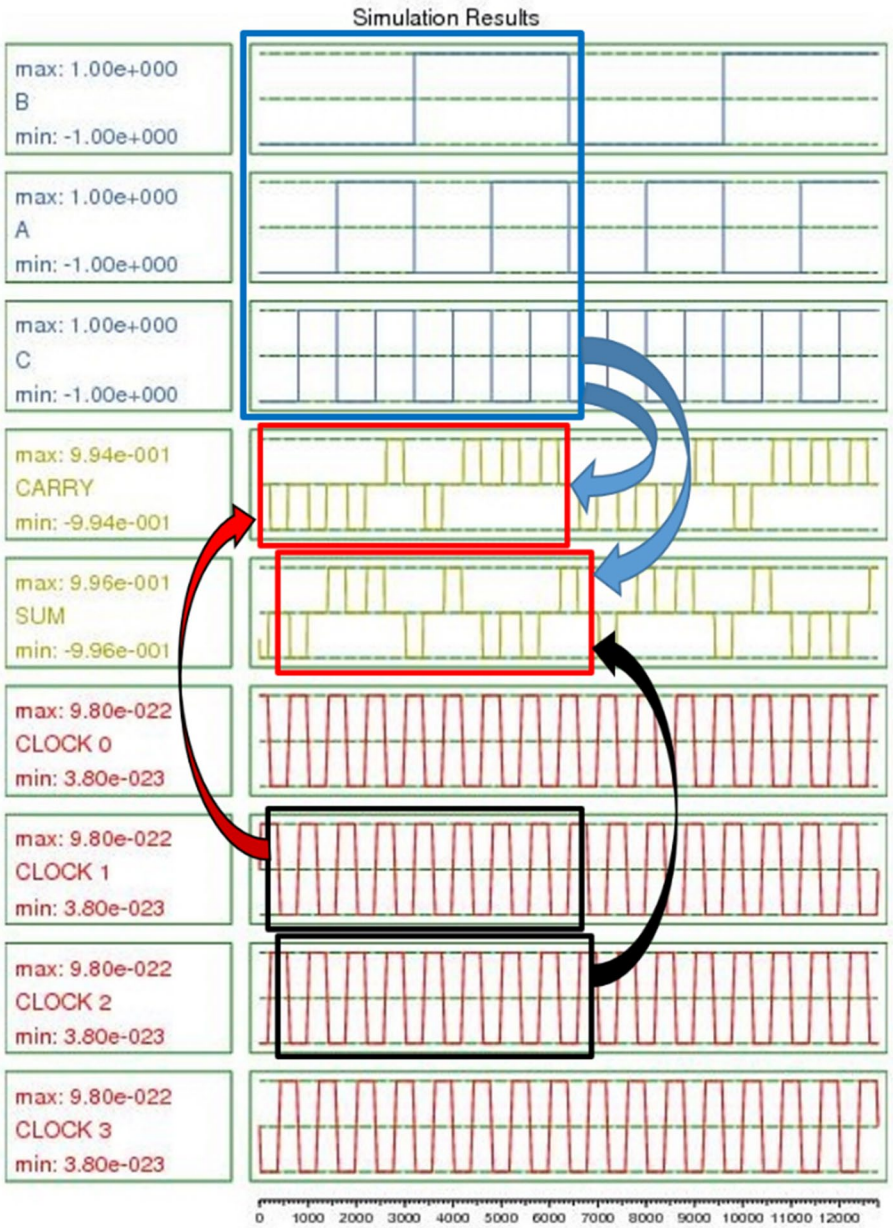

Fig. 12 The simulation outcomes of the introduced one-bit full-adder cell

Table 4 Comparisons among the proposed and state-of-the-art designs

Paper	Area (μm^2)	Cells	Delay (clock phase)	Layer(s)	Improvement (# of cells)
Proposed design	0.01	28	3	3	–
[58]	0.02	38	3	3	26%
[59]	0.04	41	2	1	32%
[60]	0.04	49	4	1	43%
[49]	0.04	51	3	3	45%
[46]	0.04	52	3	3	46%
[54]	0.04	59	4	1	52.5%
[55]	0.04	30	4	6	7%
[52]	0.02	31	3	3	10%
[52]	0.02	33	3	3	15%
[49]	0.05	79	7	3	64.5%
[61]	0.04	73	3	3	62%
[62]	0.09	78	3	1	64%
[6]	0.03	61	3	3	54%
[63]	0.62	292	14	1	90%
[41]	0.17	145	4	1	80%

QCA cells is important for effectiveness and performance. This design provides nearby more than 7% enhancement in cell numbers.

5 Conclusion

We have suggested a 3-level full-adder based on QCA arithmetic units. We have examined the average leakage and switching power dissipations by using a precise QCA power dissipation design. We have employed three active layers, in an innovative approach, to provide the proper functionality and the least occupation area with this circuit, leading to keeping the size of the introduced full-adder cell equal to that of a 5-input majority gate. After completing the administration and verification processes using the QCADesigner environment, we have reached an effective circuit optimization compared with the current models regarding the number of cells and area occupation.

The introduced optimal structure can help design the future QCA-based nano-scale circuits. We have designed a new full-adder, and it will be helpful for the designing of bigger units. Also, we have considered the offered model as a good answer for designing with the least count of QCA-based cells with fewer crossovers.

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