ORIGINAL PAPER

A new binary to gray code converter based on quantum-dot cellular automata nanotechnology

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Abstract

Quantum-dot cellular automata (QCA) is one of the most prominent technologies in nanometer-scale with appreciable reduction of size and power consumption and high switching frequency to overcome the scaling limitations of complementary metal-oxide semiconductor. On the other hand, code converters play a key role in signal processing and efficient network designs. The researchers have focused on emerging nano-devices that can identify errors throughout information transfer. Therefore, in this research, a new QCA-based 4-bit binary to gray converter circuit employing the appropriate configuration of the XOR gate as a basic building block has been suggested. The layout has been generated using the QCADesigner simulation tool to test the functionality of the code converter. The performance results indicated that the proposed converter works properly and has optimum performance parameters such as latency, complexity, and consumed area as compared to the current schemes.

Keywords Quantum-dot cellular automata (QCA) · Digital communication · Binary · Gray · Code converter · XOR gate · Nanoscale

1 Introduction

Quantum-dot cellular automata (QCA) is pledging nanotechnology which is a possible candidate to design different logical circuits at the nanoscale. Nowadays, the designer uses a complementary metal-oxide semiconductor (CMOS), but overcoming to its physical limitations is difficult [1–4]. Among many suggested alternatives, QCA is the vision toward the modern era of nanotechnology to create digital electronic devices without employing the transistors for reaching fast and low-power dissipation with smaller dimensions [5–9]. In QCA devices, the fundamental element is a quantum cell with four quantum dots that can house two mobile electrons [10–13]. QCA develops a device based on quantum effects and conveys information between inputs to output by changing the charge configuration [14–17]. Thus,

the electron orientations show the data in contrast to the existing flow of CMOS circuits.

A code converter is a combinational circuit that must be inserted between the two systems for their compatibility even each of them uses a distinct binary code for the same information. The basic goal of code converters is to enhance the efficiency of signal processing systems [18–21]. QCA-based code converters are significant circuit components to change information from one format to another [22, 23]. Gray code converter is very applicable in the error detection process during information transfer via communication systems and is employed for improving the switching activity. Therefore, the importance of optimization and proper functionality of code converter circuits to enhance efficiency is well known in the digital world.

Since the XOR gate is a fundamental structure to build communication circuits in arithmetic and logical units, in this research, a new design of 4-bit binary to gray code converter is implemented in QCA technology by applying an efficient QCA-based XOR gate. The design is driven toward less complexity, minimum clock zones, and no crossover. Presented architecture and its parameters are compared to prove efficiency. The three major goals of this paper can be summarized as follows:

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- Proposing a structure of 4-bit QCA binary to gray converter according to the introduced QCA based two-input XOR gate.
- Evaluating the proposed design from the viewpoint of consumed area, complexity, and speed.
- Verifying and simulating the suggested design via QCADesigner.

The rest of the article is arranged as follows: Sect. 2 reports the relevant literature survey from several code converters in QCA. A new design of binary to gray converter circuit using the new implementation of the XOR gate is described in Sect. 3. The QCA layout of the suggested circuits along with simulation results is discussed in Sect. 4, and the comparison results of the existing designs are given in this section. At last, the conclusions and future works are drawn in Sect. 5.

2 Related work

Waje and Dakhole [24] have suggested a new XOR gate using coupled majority voter minority gate (CMVMIN), which is used for binary to gray code converter design in QCA technology. The new XOR gate uses QCA-based CMVMIN, majority voter, and two NOT gates. In this work, three XOR gates are required to implement a code converter. The number of used multilayer crossovers in the presented 4-bit code converter can increase the performance of the design. The proposed designs are also capable in terms of area, complexity, and latency.

Also, Bhoi et al. [25] have been proposed a robust design of XOR, which is used in the construction of reversible code converter and binary incrementer. Presented two-input XOR gate is employed to design an efficient QCA Feynman gate. The code converter and binary incrementer are designed based on efficient Feynman gates. In the proposed binary to the gray circuit, the outputs are attained correctly with zero latency. The designs provide less cell count, low clock zones, and no crossover.

Furthermore, a QCA-based design of binary to gray converter employing layered T gate has been proposed by Chakraborty et al. [14]. The layered T gate includes two inputs and one output cells that are located in the main cell layer and one fixed polarization cell that is placed in the upper layer. Polarization $+1$ or -1 to fixed polarization cell produces NAND or NOR gate. The proposed layered T code converter requires a minimum cell number, which causes the circuit to be more compact and stable.

Finally, efficient binary/gray converters with the help of a two-input LTEx module has been introduced by Mukherjee et al. [12]. In this work, QCA-based two-input XOR is
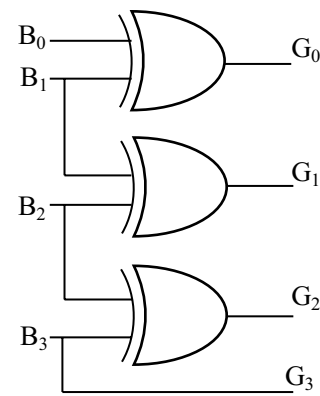

Fig. 1 Logical schematic of 4-bit binary to gray code converter

implemented using a layered T gate, namely the LTEx module. This module has four layered T NAND (LT NAND) gates. The two-input LTEx module is extended to design the n-bit binary/gray converters. The QCA-based design in this article for n-bit converter layouts considers the suitable formulation of cost, area, and delay.

3 Proposed design

XOR gate has high importance in many digital logic applications such as error detection and correction, as well as in arithmetic and logical units. Therefore, the implementation of the XOR gate is required to design the binary to gray converter. Traditionally, XOR gate implementation includes majority and inverter gates due to its logical function. In this section, a two-input XOR gate by only one majority gate is introduced. XOR gate works based on inputs that are organized with a clock phase and impact of the cells on each other. In the XOR, the expected output would be obtained by the influence of the cell to each other according to different combinations of inputs. The logical expression of two-input XOR is $XOR\ (A,\ B) = A'B + AB'$.

Code converters are combinational circuits that convert code into another which is encoded in logic arrays to improving the efficiency of signal processing systems [18]. A binary to gray converter receives binary numbers as input, processes it, and produces the equivalent gray code as output [22]. In the remainder of this section, a new circuit of a 4-bit binary to gray converter is offered by employing a two-input XOR gate as the principal element in all code converters. The logic expressions of converter outputs are given in Eq. (1) [26]. The implementation of a 4-bit proposed converter is composed of three XOR gates. The logical schematic of this converter is shown in Fig. 1.

Table 1 Truth table representations of 4-bit binary to gray code converter

Binary inputs				Gray outputs			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

$$G_3 = B_3 \quad G_2 = B_3 \oplus B_2 \quad G_1 = B_2 \oplus B_1 \quad G_0 = B_1 \oplus B_0 \tag{1}$$

The binary signals B_3, B_2, B_1, and B_0 are four input signals of the 4-bit binary to gray converter, which is processed to produce the outputs G_3, G_2, G_1, and G_0. The truth table of this converter circuit is reported in Table 1.

4 Simulation results

This section includes QCA implementation of the suggested code converter and its simulation result along with describing the simulation tool and the comparison with available designs.

4.1 Simulation tool

QCADesigner is a precision tool that is used for modeling and simulation of the QCA-based circuit evolved at the ATIPS Laboratory. Standard CAD features and diverse QCA simulation engines of this tool allow us to layout and verify each QCA design [27]. The functionality of the proposed structure is surveyed by QCADesigner 2.0.3. All of the software settings and simulation parameters encompass the default values of this tool.
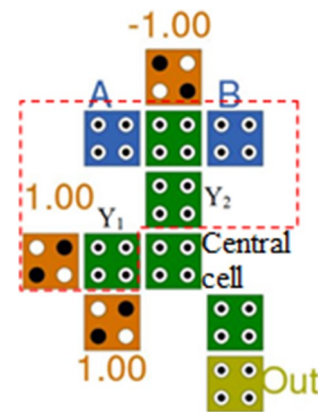
Fig. 2 The layout of two-input XOR gate in QCA

Table 2 The truth table of two-input XOR gate

A	B	Central Cell	OUT
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0

4.2 Layout of the proposed design

The QCA layout and truth table of two-input XOR are represented in Fig. 2 and Table 2, respectively. XOR implementation is based on a one-layer approach and without any crossover wire. The number of cells needed to implement the XOR gate is 11 cells and covers an area of approximately $0.02\ \mu m^2$. Table 2 describes the truth table of the two-input

XOR gate; if A and B inputs are equal to 0 or 1, Y_2 cell imposes value to the central cell and the output will be 0. Otherwise, Y_1 defines the amount of central cell. According to Fig. 2, six cells of the inside of the dotted line affect the central cell.

Figure 3 illustrates the QCA layout of a 4-bit binary to gray converter circuit with the presented XOR gate. QCA implementation of the offered converter is based on one layered approach and without any crossover wire. This structure includes 39 QCA cells, which are arranged in a 0.05 μm^2 area. The output from a proposed code converter can be obtained without delay.

4.3 Accuracy analysis

The result gained from XOR gate simulation is shown in Fig. 4. Two waveforms with diverse frequencies are applied at inputs A and B. The XOR output is high when one of the inputs is 1 and when both of the inputs have the same value, the XOR output is low. The output is obtained correctly without any latency.

Results of the proposed 4-bit binary to gray code converter using three XOR gate are exhibited in Fig. 5. Four

Fig. 3 The layout of 4-bit binary to gray converter in QCA

waveforms with diverse frequencies are applied at inputs B_0, B_1, B_2, and B_3. If inputs $B_3B_2I_1I_0 = 0000$ are applied at the first clock, then outcomes $G_3G_2G_1G_0 = 0000$ is reached, and if inputs $B_3B_2B_1B_0 = 1000$ are applied at the second clock then $G_3G_2G_1G_0 = 1100$ appears in outputs, and so on. The results appear in outputs correctly with zero latency.

4.4 Comparisons

The performance of the suggested QCA-based XOR gate and its implementations as code converter and previous designs are assessed by means of the conventional metrics to compare the feature of the new designs. A comparative study of various parameters like effective area, latency, and complexity for proposed structures of XOR gate and code converter with available designs are performed in Tables 3 and 4. As it is shown in Table 3, the presented XOR gate is superior compared to other designs and provides better efficiency. According to Table 4, it can be shown that the proposed QCA layout of code converters is better than the common structures due to lower cell count, delay, and effective area. In addition, the proposed converter is designed without wire crossing and based on a single-level method.
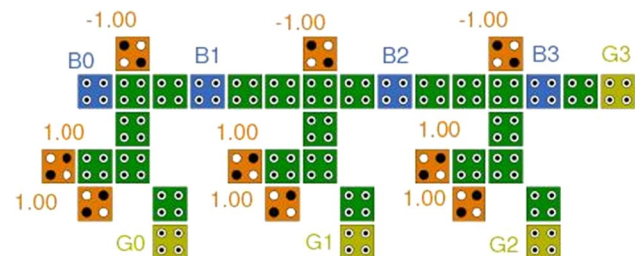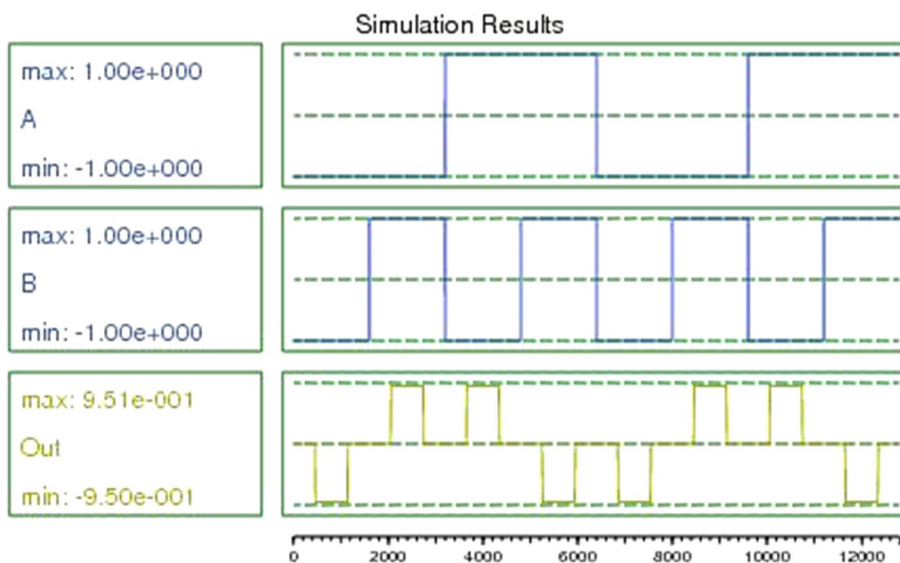
5 Conclusion and future work

This paper emphasis the design of an efficient QCA-based 4-bit binary to gray code converter with the help of the design of an improved QCA-based two-input XOR gate. This work attempts to achieve the efficient design of the binary to gray converter. The simulation results of all layouts have verified the functionality of the proposed plans. Designing the suggested layouts is done using the QCADesigner

Fig. 4 Simulation of the suggested XOR gate

Fig. 5 Simulation of proposed 4-bit binary to gray code converter
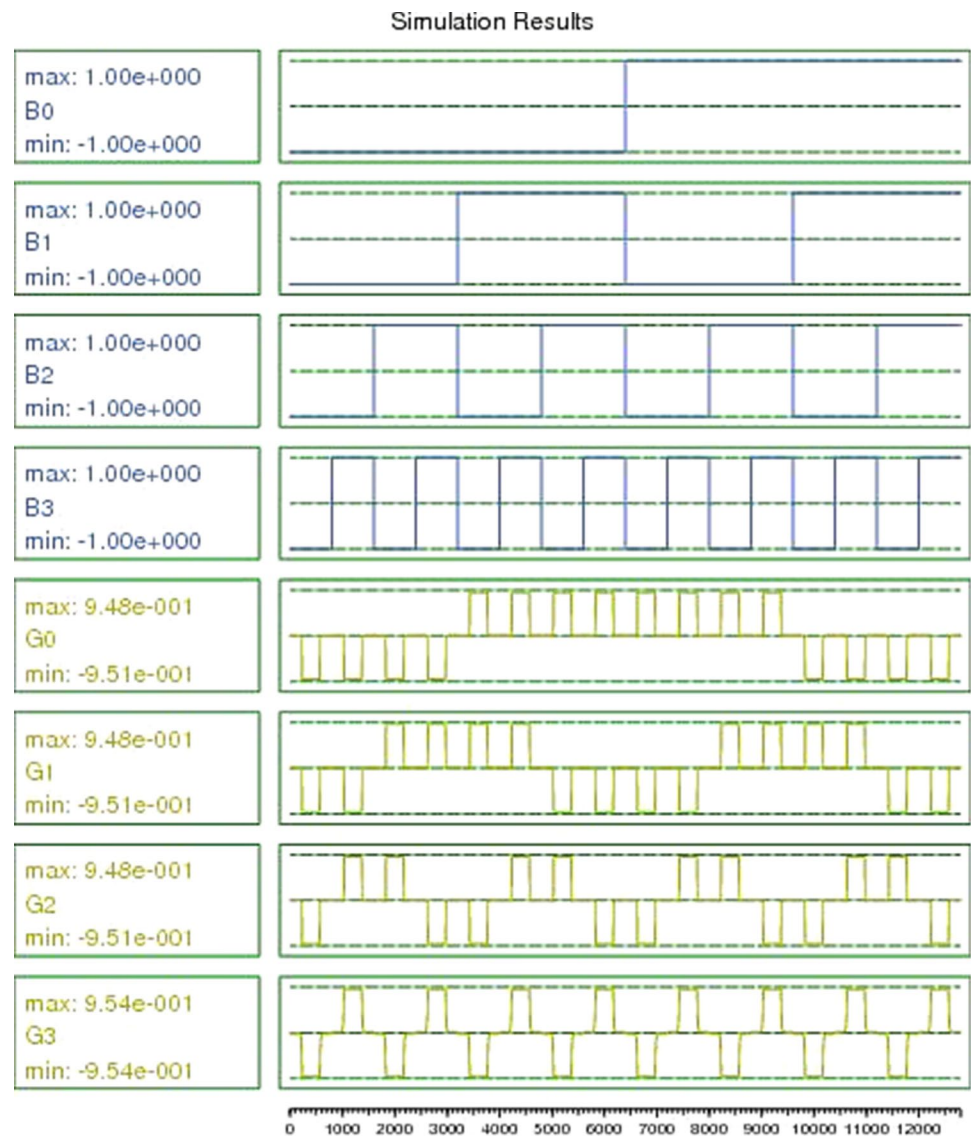
Table 3 Comparative analysis of QCA layouts of XOR gate

Two-input XOR	Number of cells	Effective area (μm2)	Latency
In [28]	28	0.02	0.75
In [29]	14	0.04	0.5
In [30]	18	0.01	0.75
In [31]	13	0.012	0.5
In [25]	13	0.02	0.5
Proposed	11	0.02	0.25

tool. Offered single layer approaches achieve the desirable outcome by improving the QCA metrics like effective area, latency, and cell count. A suggested QCA-based code converter has achieved a higher efficiency compared to previous available works. In the future, more emphasis will be on overcoming the defect challenges which makes the circuit more stable. The proposed designs could be a promising step to use in digital communication systems in smaller dimensions as well as in greater bit code converter circuits in the future.

Table 4 Comparative analysis of QCA layouts of proposed 4-bit binary to gray converter with existing designs

4-bit binary to gray converter	Number of cells	Effective area (μm^2)	Latency (clock cycle)	Types of wire crossing	Crossover
In [24]	133	0.14	0.75	Multilayer	1
In [18]	131	0.18	0.75	Not required	0
In [32]	127	0.41	0.75	Multilayer	3
In [33]	225	0.43	1	Multilayer	2
In [30]	92	0.10	0.75	Coplanar	1
In [25]	44	0.07	0.5	Not required	0
In [22]	88	0.19	0.75	Multilayer	0
Proposed	39	0.05	0.25	Not required	0

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