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ORIGINAL PAPER

Design and implementation of circuit-switched network based on nanoscale quantum-dot cellular automata

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Abstract
Quantum-dot cellular automata (QCA) is a nanoscale technology to design digital circuits in nano-measure which acts based on electron's interaction. The technology of collecting, processing and distributing information is growing rapidly, but the growth in demand for advanced methods in data processing has always been greater than the speed of growth of these technologies. Hence, computer networks play an important role in providing a resource sharing and facilitating user communications. The circuit-switched network is one of the main components for sending input signals between different users within the network. In this paper, a minimal and optimal design of the circuit-switched network is presented at a single level in QCA. The proposed design is studied and compared with existing designs in terms of fault tolerant under stuck-at 0 and 1. There is also a physical analysis for the proposed circuit-switched network.

Keywords Nanotechnology · Circuit-switched network · Quantum-dot cellular automata · Fault tolerant · Kink energy

1 Introduction

Recently, CMOS technology has been used to design digital circuits. CMOS technology is faced with leakage current and increasing power consumption challenges because of increasing size of the designed circuits. Today, QCA shows good attributes such as high speed, small size and low consuming power. QCA is a nanotechnology to design the circuit of the digital systems which based on electrons interaction, and it is used to design the circuits in nanoscales [1–3]. Computer networks are so important because they simplify the communications between different users to share the resources. The shared resources can be hardware, software and information. Switch is one of the main and important ingredients in computer networks which have enough potential to change the communication's method. Using switch makes the users to able to send the information with network at the same time; however, sending speed of the information do not effect on availability of the other users. Circuit switching of the network is one of the main parts to send input signals between different users in network. In this paper, new structure for the multiplexer is used to present a single level design for circuit switching of the network. These efforts are done to compare this structure with the existing ones to be minimized and optimized over the number of the cells, delay and complexity. Also, the proposed design has been analyzed for the tolerance of stuck-at 0 and 1, which is optimal compared to existing designs. The proposed design is also analyzed in the form of physical analysis.

2 Review of quantum-dot cellular automata

Quantum-dot cellular automata are a technology which can run at high frequency, low consuming power and nano-measured size. This technology can be used instead of CMOS technology. The smallest unit in quantum-dot cellular automata is quantum cell which contains four quantum dots. Figure 1a, b shows two cells with 90° and 45° which are in quantum-dot cellular automata [4].

There are two free electrons in each quantum cell. Due to the existence of a coulomb repulsive force between electrons, they have to be farthest away. Therefore, there will be two stable states of electrons sets in quantum cell. These states are shown as -1 and $+1$. Figure 2a, b, respectively, shows these states [4–6].

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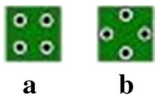


Fig. 1 **a** Quantum cell with 90° and **b** quantum cell with 45°

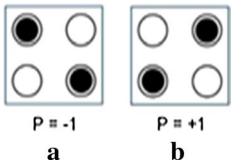


Fig. 2 **a** Electrons on main diameter and **b** electrons on adjunct diameter

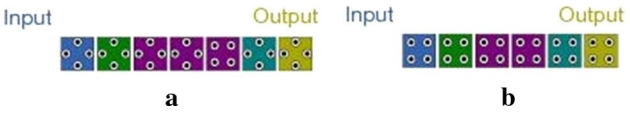


Fig. 3 **a** 45° wire in QCA and **b** 90° wire in QCA

Wires transfer information in quantum-dot cellular automata like any other technologies. Quantum wires are made with quantum cells in quantum-dot cellular automata. There are two types of quantum-dot cellular automata wires which are 45° and 90° that are, respectively, shown in Fig. 3a, b [4–7].

There are different ways to transfer the current in crossover circuits in quantum-dot cellular automata. These methods are crossing the 45° and 90° wires from each other, designing multilayer and using clock functionality. The 45° and 90° wires can transfer current from each other without interference. Multilayer designing is one of the layouts in quantum-dot cellular automata which crossover sections are designed in different layers. Other type is that wires with two different clock zones transfer the current without interference, as shown in Fig. 4a–c [5–23].

Fundamental gates are the majority and inverter gates in quantum-dot cellular automata. Majority gates have two types: three-input and five-input. The voter cell transfers

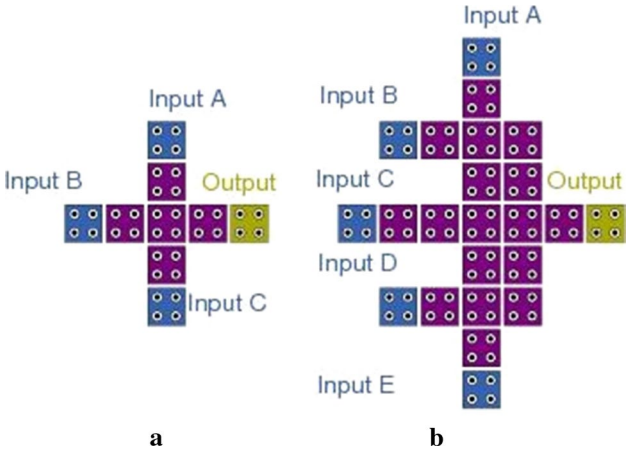


Fig. 5 **a** 3 input majority gate in quantum-dot cellular automata and **b** 5 input majority gate in quantum-dot cellular automata

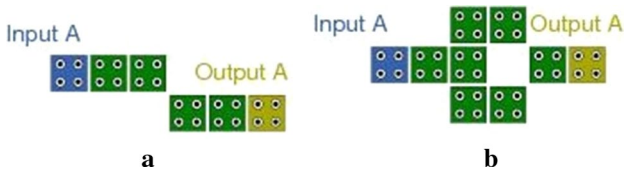


Fig. 6 **a** Oblique inverter gate and **b** pair inverter gate

the majority of the input to the output in majority gates. Figure 5a, b, respectively, shows the three-input and five-input majority gates [24–26].

Inverter gate transfers the inverse of the input to the output. Figure 6a, b, respectively, shows the oblique and pair inverter gates in quantum-dot cellular automata [24–27].

Clocking scheme is used to sync the information in designing of the complicated structures in quantum-dot cellular automata. Clock cycle of the quantum-dot cellular automata contains four phases: switch, hold, release and relax. At switch phase, the movement of electrons inside

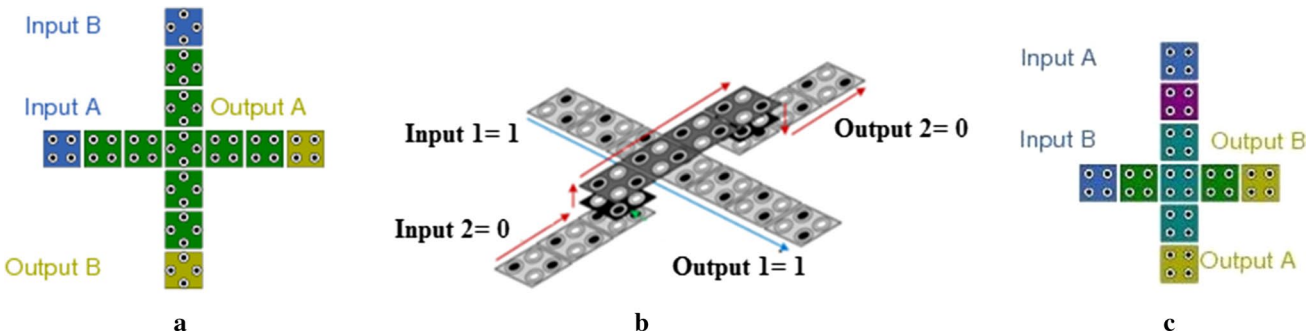


Fig. 4 **a** Crossover, **b** multilayer and **c** different zones

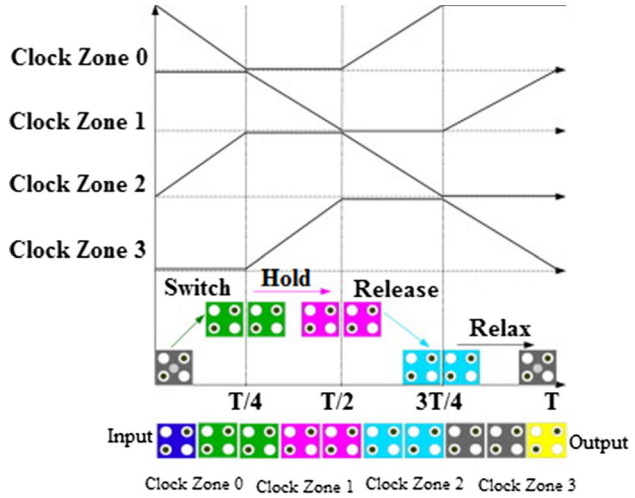


Fig. 7 Phases of the clock cycle in quantum-dot cellular automata

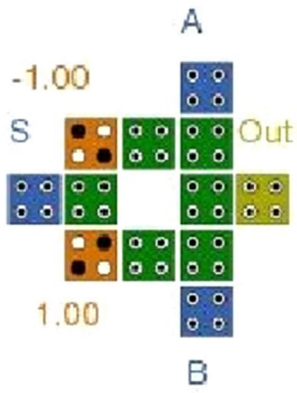
of the cell is slowly decreased. At hold phase, the electrons are stable inside of the cell. At release phase, the speed of the electrons is being increasing. At relax phase, the electrons move freely inside of the cell. Figure 7 shows the phases of the clock cycle in quantum-dot cellular automata [28–30].

Table 1 Truth table of the crossbar switch circuit

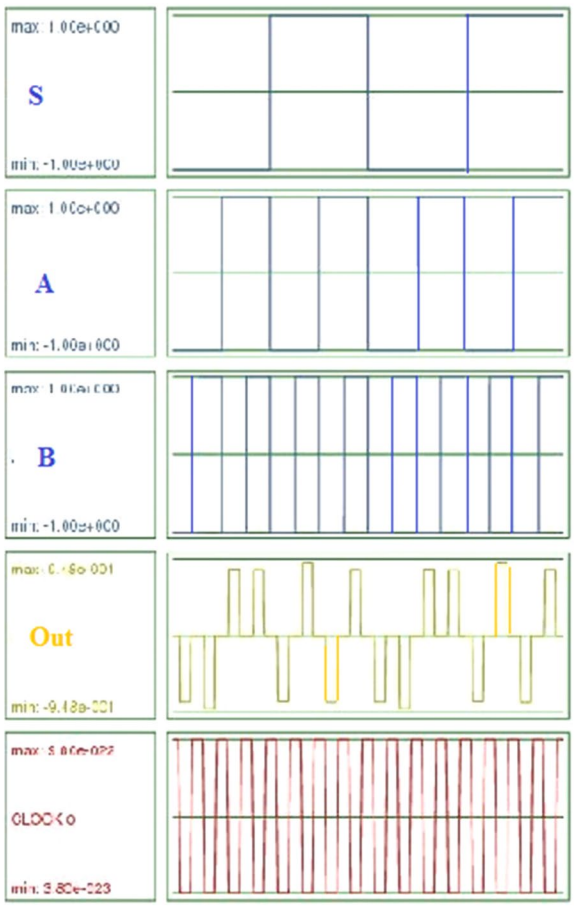
S	A	B	C	D
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	1

3 Related work

In this section, the presented structure by Jadav Chandra Das [31] has been studied which is the design of circuit-switched network in single layer. It has presented a new crossbar switch to design circuit switching network. The crossbar switch contains two multiplexers which includes control signal, two inputs A and B and two outputs C and



a



b

Fig. 8 **a** Multiplexer structure presented by Mr. Mazaher Naji in quantum-dot cellular automata [32] and **b** the result of the simulation

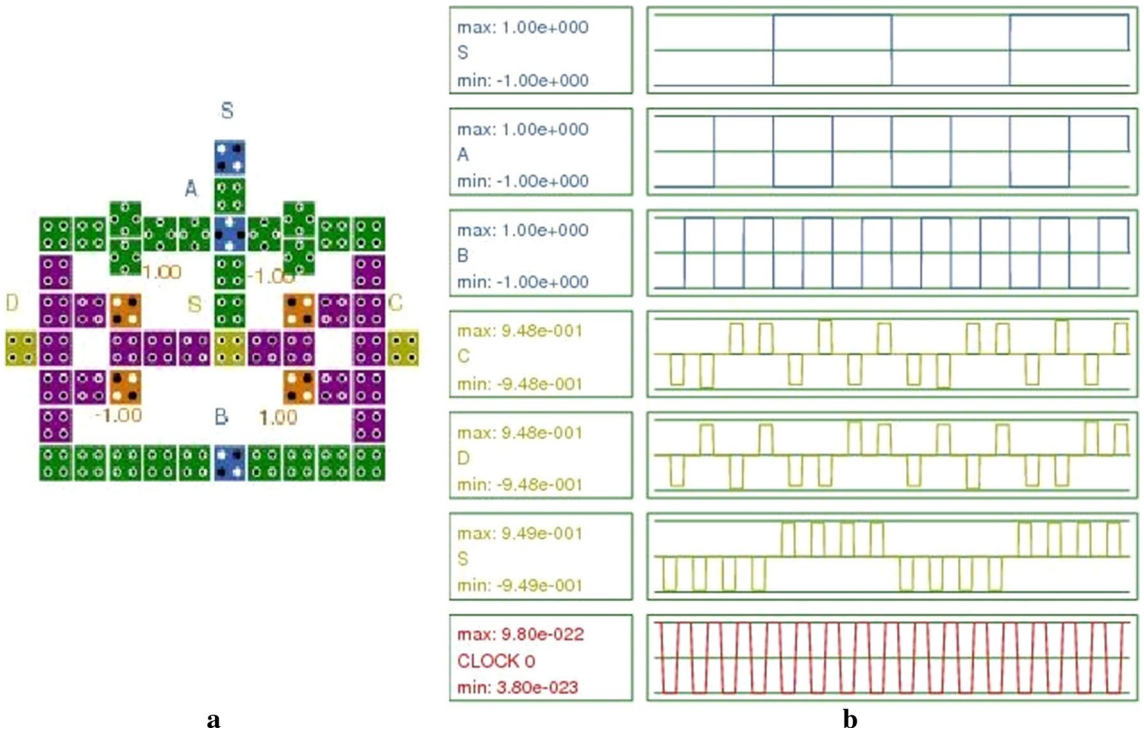


Fig. 9 **a** Designing and implementing of the crossbar switch circuit and **b** the simulation results

Table 2 Suggested crossbar switch circuit's fault tolerant analysis in face of the stuck-at 0 and 1

Test vector (SAB)	000	001	010	011	100	101	110	111
Expected output (CD)	00	01	10	11	00	10	01	11
S stuck-at 0	00	01	10	11	00	01	10	11
S stuck-at 1	00	10	01	11	00	10	01	11
A stuck-at 0	00	01	00	01	00	10	00	10
A stuck-at 1	10	11	10	11	01	11	01	11
B stuck-at 0	00	00	10	10	00	00	01	01
B stuck-at 1	01	01	11	11	10	10	11	11
C stuck-at 0	00	01	00	01	00	00	01	01
C stuck-at 1	10	11	10	11	10	10	11	11
D stuck-at 0	00	00	10	10	00	10	00	10
D stuck-at 1	01	01	11	11	01	11	01	11
SA stuck-at 0	00	01	00	01	00	01	00	01
SA stuck-at 1	01	11	01	11	01	11	01	11
AB stuck-at 0	00	00	00	00	00	00	00	00
AB stuck-at 1	11	11	11	11	11	11	11	11
SB stuck-at 0	00	00	10	10	00	00	10	10
SB stuck-at 1	10	10	11	11	10	10	11	11
CD stuck-at 0	00	00	00	00	00	00	00	00
CD stuck-at 1	11	11	11	11	11	11	11	11
SAB stuck-at 0	00	00	00	00	00	00	00	00
SAB stuck-at 1	11	11	11	11	11	11	11	11

Table 3 Truth table of the transmitter circuit

S0	S	A	B	T_{out}
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

D. The crossbar switch uses two test vectors 010 and 101 for experiment, and the results show that it is 90% fault tolerant in the face of stuck-at 0 and 1. In the following, a new crossbar switch, including transmitter and receiver, is designed which transmitter includes three multiplexers, two control signals, two input lines A and B and one output line. Transmitter and receiver get connected together to design circuit switching network.

4 Designing of the suggested circuit-switched network

Circuit switching network is one of the main parts to send input signals between different users in the network. Circuit switching network contains two parts: transmitter and receiver. A crossbar switch is needed to guide the input signals to the output in circuit switching network.

4.1 Crossbar switch circuit design

Crossbar switch's duty is to change the input path from one output line to another output line. The multiplexer structure presented by Mr. Mazaher Naji [32] is used to design crossbar switch circuit. The multiplexer contains 12 cells and 1 delay at clock zone. The control signal's S duty is to guide input to the output line. For control signal S = 0, the input A will be seen at output line. If signal control is S = 1, the input B will be seen at output line. Figure 8a, b shows, respectively, the structure and results of the simulation for the multiplexer [32].

The crossbar switch circuit in this paper contains two 2 × 1 multiplexers, and it is controlled by control signal S. The crossbar switch includes inputs A and B and outputs C and D. If control signal is S = 0, the inputs A and B are seen, respectively, in outputs C and D line. But if the control signal is S = 1, the inputs A and B get transferred to the outputs

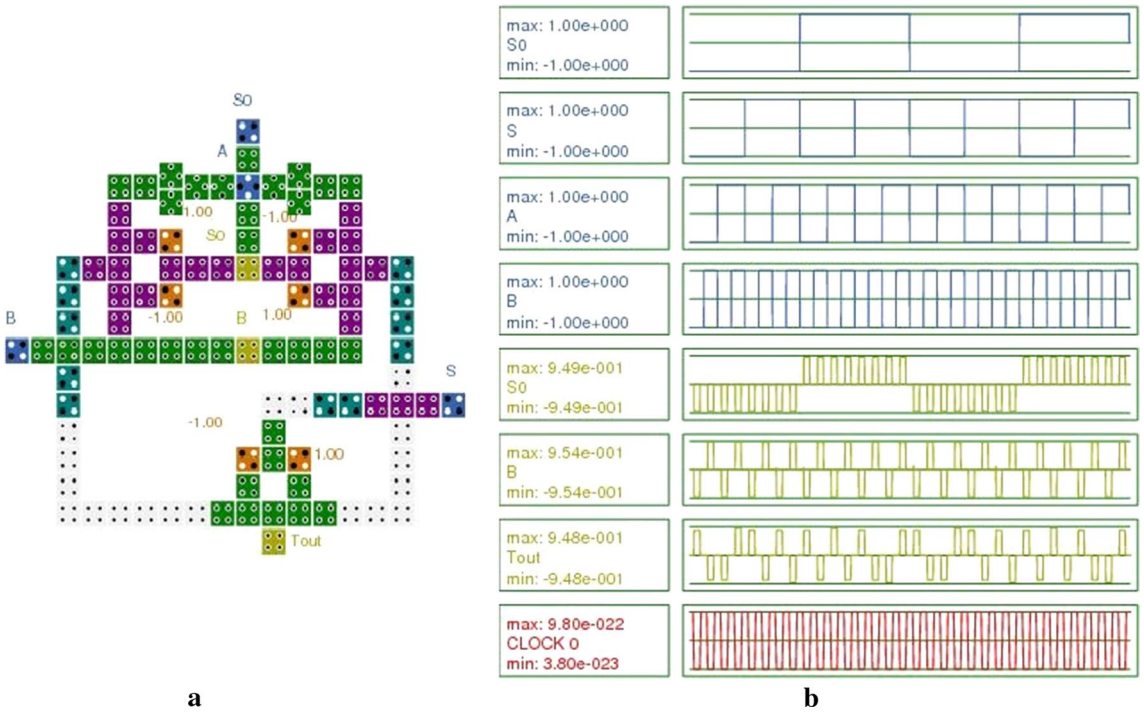


Fig. 10 **a** Designing and implementing of the transmitter circuit in quantum-dot cellular automata and **b** the results of the simulation

Table 4 Transmitter circuit fault tolerant analysis under (a) S0 stuck-at 0 or 1, (b) S stuck-at 0 or 1, (c) S0 and S stuck-at 0 or 1

S0	S	Expected output (T_{out})	S0 stuck-at 0 or 1	Faulty output ($T_{out)}$
(a) S0 stuck-at 0 or 1				
0	0	A	1 0	B
0	1	B	1 1	A
1	0	B	0 0	A
1	1	A	0 1	B
S0	S	Expected output (T_{out})	S stuck-at 0 or 1	Faulty output (T_{out})
(b) S stuck-at 0 or 1				
0	0	A	0 1	B
0	1	B	0 0	A
1	0	B	1 1	A
1	1	A	1 0	B
S0	S	Expected output (T_{out})	S0 and S stuck-at 0 or 1	Faulty output (T_{out})
(c) S0 and S stuck-at 0 or 1				
0	0	A	0 0 or 1 1	A
0	1	B	0 0 or 1 1	A
1	0	B	0 0 or 1 1	A
1	1	A	0 0 or 1 1	A

Table 5 Truth table of the receiver circuit

S	S0	I	C	D
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

D and C. Table 1 shows the truth table of the suggested crossbar switch circuit.

Figure 9a, b shows, respectively, designing and implementing of the crossbar switch circuit and its simulation's results. The suggested crossbar switch circuit's delay is two clock zones, and it contains 52 quantum cells.

The suggested crossbar switch circuit has been analyzed for fault tolerant under stuck-at 0 and 1, and the results are shown in Table 2. The crossbar switch circuit that presented by Jadav Chandra Das and Debashis De [31] uses two test vectors 010 and 101 for the experiment, and its fault tolerant is 90%. The suggested crossbar switch circuit in this paper uses two test vectors 101 and 110 for the experiment, and the fault tolerant of it is 95%. If we use three test vectors 001, 101 and 110, the suggested crossbar switch's fault tolerant is 100%.

4.2 Transmitter designing

A crossbar switch circuit and a 2×1 multiplexer are used to design transmitter circuit. The outputs of the crossbar switch circuit are as 2×1 multiplexer inputs. The transmitter includes two input lines A and B and one output line T_{out}. S0 and S are, respectively, the control signals of the crossbar switch circuit and 2×1 multiplexer. If the control signals S0 and S have the same values, the input A will be seen at output line T_{out}. But if the control signals S0 and S do not have same values, the input B gets transferred to the output line T_{out}. Table 3 shows the truth table of the transmitter circuit.

Figure 10a, b shows, respectively, the designing and implementing of the transmitter circuit in quantum-dot

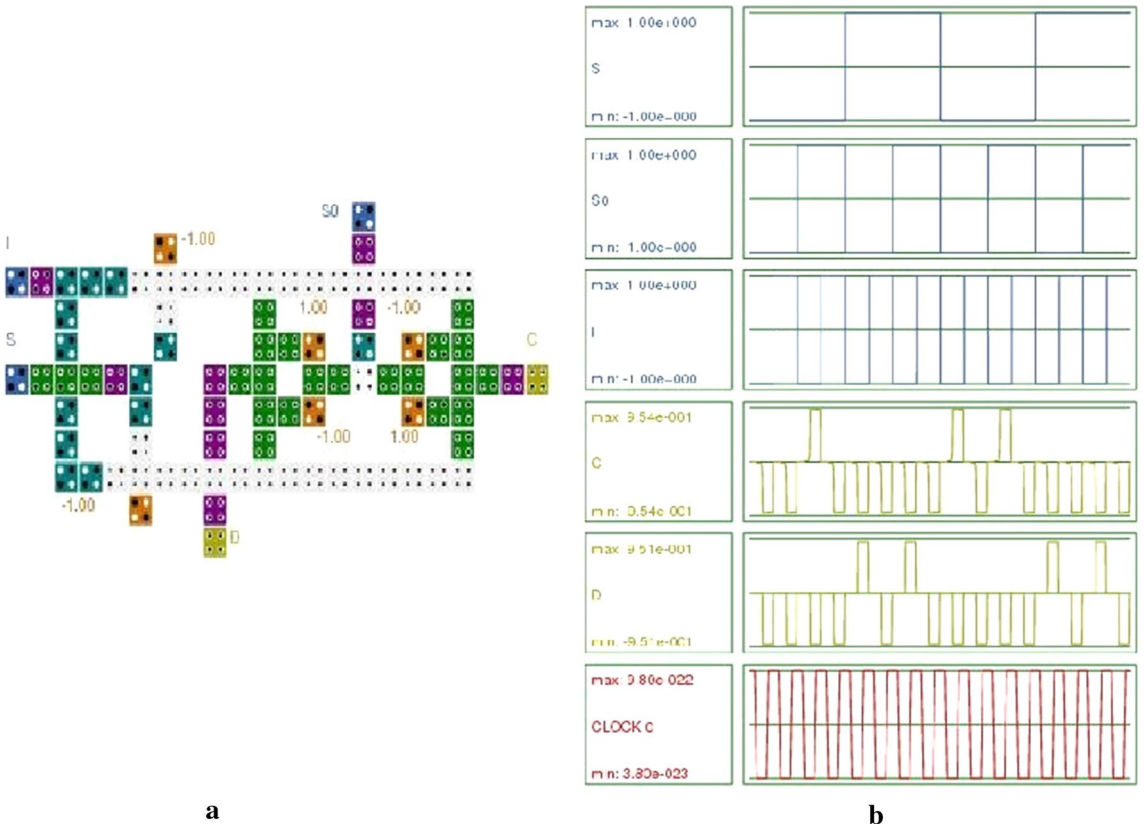


Fig. 11 **a** Designing and implementing of the receiver circuit in quantum-dot cellular automata and **b** the results of the simulation

cellular automata and the results of the simulation. The transmitter circuit delay is one clock cycle, and it contains 101 quantum cells.

Table 4(a)–(c) shows the result of the fault tolerant under stuck-at 0 and 1. As shown in Table 4(a) and (b), if the stuck-at 0 and 1 occurs on S0 and S, all components of the S0 and S have fault and the fault is recognizable. As shown in Table 4(c), if stuck-at 0 and 1 occurs simultaneously on S0 and S and if S0 and S have unequal values, a fault occurs and that fault is recognizable.

4.3 Receiver circuit designing

A 1×2 demultiplexer and a crossbar switch circuit are used to design receiver circuit. The output of the 1×2 demultiplexer is as input of the crossbar switch circuit. Receiver circuit contains one input line I and two output lines C and D. S and S0 are, respectively, the control signals of the 1×2 demultiplexer and crossbar switch circuit. The input I will be seen in output line C when the control signals S and S0 have same values. But if control signals S and S0 do not have same values, the input I transferred to the output line D. Table 5 shows the truth table of the receiver circuit.

Figure 11a, b shows, respectively, designing and implementing of the receiver circuit in quantum-dot cellular automata and the results of the simulation. Receiver circuit delay is 6 clock zones and contains 88 quantum cells.

The receiver circuit's fault tolerant under stuck-at 0 or 1 has been analyzed, and its result is shown in Table 6(a)–(c). As shown in table 6(a) and (b), if stuck-at 0 and 1 occurs on S and S0, all of the fault components occur for S and S0 and the fault is diagnosable. Based on the results of Table 6(c), if stuck-at 0 and 1 occurs simultaneously on S0 and S and if S0 and S have unequal values, a fault occurs and that fault is recognizable.

4.4 Circuit-switched network designing

Transmitter and receiver circuits get connected to each other to design the suggested circuit-switched network. In fact, output of the transmitter circuit is connected to the demultiplexer input of the receiver circuit. Therefore, circuit switching network contains two transmitter users A and B and two receiver users C and D which are connected with a unique channel. The proposed circuit includes four control signals S1, S2, S3 and S4. Control signals S1 and S2 are,

Table 6 Receiver circuit's fault tolerant analysis under (a) S stuck-at 0 or 1, (b) S0 stuck-at 0 or 1 and (c) S0 and S stuck-at 0 or 1

S	S0	Expected output (C D)	S stuck-at 0 or 1	Faulty output (C D)
(a) S at 0 or 1				
0	0	I 0	1 0	0 I
0	1	0 I	1 1	I 0
1	0	0 I	0 0	I 0
1	1	I 0	0 1	0 I
S	S0	Expected output (C D)	S0 stuck-at 0 or 1	Faulty output (C D)
(b) S0 at 0 or 1				
0	0	I 0	0 1	0 I
0	1	0 I	0 0	I 0
1	0	0 I	1 1	I 0
1	1	I 0	1 0	0 I
S	S0	Expected output (C D)	S0 and S stuck-at 0 or 1	Faulty output (C D)
(c) S0 and S at 0 or 1				
0	0	I 0	0 0 or 1 1	I 0
0	1	0 I	0 0 or 1 1	I 0
1	0	0 I	0 0 or 1 1	I 0
1	1	I 0	0 0 or 1 1	I 0

Table 7 Suggested switching circuit of communication path

S4	S3	S2	S1	Communication path	C	D
0	0	0	0	A→C	A	0
0	0	0	1	A→D	0	A
0	0	1	0	A→D	0	A
0	0	1	1	A→C	A	0
0	1	0	0	B→C	B	0
0	1	0	1	B→D	0	B
0	1	1	0	B→D	0	B
0	1	1	1	B→C	B	0
1	0	0	0	B→C	B	0
1	0	0	1	B→D	0	B
1	0	1	0	B→D	0	B
1	0	1	1	B→C	B	0
1	1	0	0	A→C	A	0
1	1	0	1	A→D	0	A
1	1	1	0	A→D	0	A
1	1	1	1	A→C	A	0

Table 8 Simulation parameters

Parameters	Value
Temperature	1.000000
Relaxation time	$1.000000e^{-015}$
Time setup	$1.000000e^{-016}$
Total simulation time	$7.000000e^{-011}$
Clock high	$9.800000e^{-022}$
Clock low	$3.800000e^{-023}$
Clock shift	$0.000000e^{+000}$
Clock amplitude factor	2.000000
Radius of effect	80.000000
Relative permittivity	12.900000
Layer separation	11.500000

respectively, crossbar switch and 2×1 multiplexer inputs in transmitter, and control signals S3 and S4 are, respectively, 1×2 demultiplexer and crossbar switch inputs in receiver. Table 7 shows suggested switching circuit of communication path.

The suggested design is simulated by QCA designer 2.0.3 software using coherence vector specifications. Table 8 shows the parameters of the simulation.

Figure 12a, b shows designing and implementing of the suggested circuit switching network in quantum-dot cellular automata and the results of the simulation. Circuit switching network's delay is two clock cycles and contains 207 quantum cells.

The fault tolerant of suggested circuit switching network is analyzed under stuck-at 0 or 1, and the simulation results are shown in Tables 9(a)–(h), 10, 11 and 12.

In Table 9(a), if stuck-at 0 or 1 occurs on control signals S1 or S2 for input 0000, respectively, one of the fault situations 1000 or 0100 will happen. Therefore, the faulty path will be B → C. The other input analysis method is same.

In Table 9(b), if stuck-at 0 or 1 occurs on control signals S3 or S4 for input 0010, respectively, one of the fault situations 0000 or 0011 will happen. Therefore, the faulty path will be A → C. The other input analysis method is same.

In Table 9(c), if stuck-at 0 or 1 occurs simultaneously on each control signals S1 and S2 for 1100 input, one of the fault situations 0000 or 1100 will happen. Therefore, the

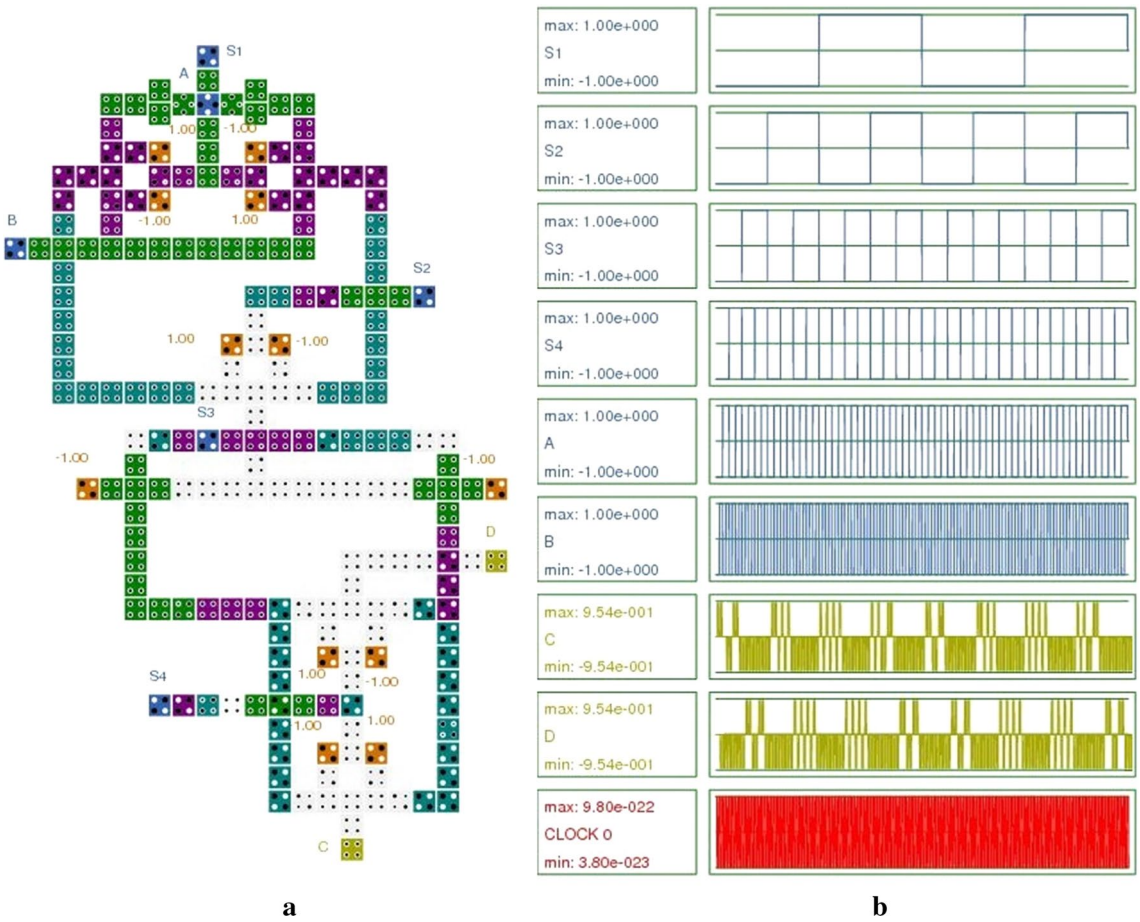


Fig. 12 **a** Designing and implementing of the suggested circuit switching network in quantum-dot cellular automata and **b** the simulation results

Table 9 Circuit switching network's fault tolerant analysis under (a) S1 or S2 stuck-at 0 or 1, (b) S3 or S4 stuck-at 0 or 1, (c) S1 and S2 stuck-at 0 or 1, (d) S1 and S3 stuck-at 0 or 1, (e) S1 and S4 stuck-at 0 or 1, (f) S2 and S3 stuck-at 0 or 1, (g) S2 and S4 stuck-at 0 or 1 and (h) S3 and S4 stuck-at 0 or 1

S1	S2	S3	S4	Expected path	S1 or S2 stuck-at 0 or 1 (faulty path)
(a) S1 or S2 stuck-at 0 or 1					
0	0	0	0	A→C	B→C
0	0	0	1	A→D	B→D
0	0	1	0	A→D	B→D
0	0	1	1	A→C	B→C
0	1	0	0	B→C	A→C
0	1	0	1	B→D	A→D
0	1	1	0	B→D	A→D
0	1	1	1	B→C	A→C
1	0	0	0	B→C	A→C
1	0	0	1	B→D	A→D
1	0	1	0	B→D	A→D
1	0	1	1	B→C	A→C
1	1	0	0	A→C	B→C
1	1	0	1	A→D	B→D
1	1	1	0	A→D	B→D
1	1	1	1	A→C	B→C
S1	S2	S3	S4	Expected path	S3 or S4 stuck-at 0 or 1 (faulty path)
(b) S3 or S4 stuck-at 0 or 1					
0	0	0	0	A→C	A→D
0	0	0	1	A→D	A→C
0	0	1	0	A→D	A→C
0	0	1	1	A→C	A→D
0	1	0	0	B→C	B→D
0	1	0	1	B→D	B→C
0	1	1	0	B→D	B→C
0	1	1	1	B→C	B→D
1	0	0	0	B→C	B→D
1	0	0	1	B→D	B→C
1	0	1	0	B→D	B→C
1	0	1	1	B→C	B→D
1	1	0	0	A→C	A→D
1	1	0	1	A→D	A→C
1	1	1	0	A→D	A→C
1	1	1	1	A→C	A→D
S1	S2	S3	S4	Expected path	S1 and S2 stuck-at 0 or 1 (faulty path)
(c) S1 and S2 stuck-at 0 or 1					
0	0	0	0	A→C	Fault free
0	0	0	1	A→D	A→D
0	0	1	0	A→D	A→D
0	0	1	1	A→C	Fault free
0	1	0	0	B→C	A→C
0	1	0	1	B→D	A→D
0	1	1	0	B→D	A→D

Table 9 (continued)

S1	S2	S3	S4	Expected path	S1 and S2 stuck-at 0 or 1 (faulty path)
0	1	1	1	B → C	A → C
1	0	0	0	B → C	A → C
1	0	0	1	B → D	A → D
1	0	1	0	B → D	A → D
1	0	1	1	B → C	A → C
1	1	0	0	A → C	Fault free
1	1	0	1	A → D	A → D
1	1	1	0	A → D	A → D
1	1	1	1	A → C	Fault free
S1	S2	S3	S4	Expected path	S1 and S3 stuck-at 0 or 1 (faulty path)
(d) S1 and S3 stuck-at 0 or 1					
0	0	0	0	A → C	Fault free B → D
0	0	0	1	A → D	Fault free B → C
0	0	1	0	A → D	A → C B → D
0	0	1	1	A → C	A → D B → C
0	1	0	0	B → C	Fault free A → D
0	1	0	1	B → D	Fault free A → C
0	1	1	0	B → D	B → C A → D
0	1	1	1	B → C	B → D A → C
1	0	0	0	B → C	A → C B → D
1	0	0	1	B → D	A → D B → C
1	0	1	0	B → D	Fault free A → C
1	0	1	1	B → C	Fault free A → D
1	1	0	0	A → C	B → C A → D
1	1	0	1	A → D	B → D A → C
1	1	1	0	A → D	Fault free B → C
1	1	1	1	A → C	Fault free B → D
S1	S2	S3	S4	Expected path	S1 and S4 stuck-at 0 or 1 (faulty path)
(e) S1 and S4 stuck-at 0 or 1					
0	0	0	0	A → C	Fault free B → D
0	0	0	1	A → D	A → C B → D

Table 9 (continued)

S1	S2	S3	S4	Expected path	S1 and S4 stuck-at 0 or 1 (faulty path)
0	0	1	0	A → D	Fault free B → C
0	0	1	1	A → C	A → D B → C
0	1	0	0	B → C	Fault free A → D
0	1	0	1	B → D	A → D B → C
0	1	1	0	B → D	A → C Fault free
0	1	1	1	B → C	A → C B → D
1	0	0	0	B → C	A → C B → D
1	0	0	1	B → D	A → C Fault free
1	0	1	0	B → D	A → D B → C
1	0	1	1	B → C	A → D Fault free
1	1	0	0	A → C	A → D B → C
1	1	0	1	A → D	Fault free B → C
1	1	1	0	A → D	A → C B → D
1	1	1	1	A → C	Fault free B → D
S1	S2	S3	S4	Expected path	S2 and S3 stuck-at 0 or 1 (faulty path)
(f) S2 and S3 stuck-at 0 or 1					
0	0	0	0	A → C	Fault free B → D
0	0	0	1	A → D	Fault free B → C
0	0	1	0	A → D	A → C B → D
0	0	1	1	A → C	A → D B → C
0	1	0	0	B → C	A → D Fault free
0	1	0	1	B → D	A → D B → C
0	1	1	0	B → D	A → C Fault free
0	1	1	1	B → C	A → D Fault free
1	0	0	0	B → C	A → D Fault free
1	0	0	1	B → D	A → C Fault free
1	0	1	0	B → D	A → D B → C

Table 9 (continued)

S1	S2	S3	S4	Expected path	S2 and S3 stuck-at 0 or 1 (faulty path)
1	0	1	1	B → C	A → C B → D
1	1	0	0	A → C	A → D B → C
1	1	0	1	A → D	A → C B → D
1	1	1	0	A → D	Fault free B → C
1	1	1	1	A → C	Fault free B → D
S1	S2	S3	S4	Expected path	S2 and S4 stuck-at 0 or 1 (faulty path)
(g) S2 and S4 stuck-at 0 or 1					
0	0	0	0	A → C	Fault free B → D
0	0	0	1	A → D	A → C B → D
0	0	1	0	A → D	Fault free B → C
0	0	1	1	A → C	A → D B → C
0	1	0	0	B → C	A → C B → D
0	1	0	1	B → D	A → C Fault free
0	1	1	0	B → D	A → D B → C
0	1	1	1	B → C	A → D Fault free
1	0	0	0	B → C	A → D Fault free
1	0	0	1	B → D	A → D B → C
1	0	1	0	B → D	A → C Fault free
1	0	1	1	B → C	A → C B → D
1	1	0	0	A → C	A → D B → C
1	1	0	1	A → D	Fault free B → C
1	1	1	0	A → D	A → C B → D
1	1	1	1	A → C	Fault free B → D
S1	S2	S3	S4	Expected path	S3 and S4 stuck-at 0 or 1 (faulty path)
(h) S3 and S4 stuck-at 0 or 1					
0	0	0	0	A → C	Fault free
0	0	0	1	A → D	A → C
0	0	1	0	A → D	A → C
0	0	1	1	A → C	Fault free

Table 9 (continued)

S1	S2	S3	S4	Expected path	S3 and S4 stuck-at 0 or 1 (faulty path)
0	1	0	0	B→C	Fault free
0	1	0	1	B→D	B→C
0	1	1	0	B→D	B→C
0	1	1	1	B→C	Fault free
1	0	0	0	B→C	Fault free
1	0	0	1	B→D	B→C
1	0	1	0	B→D	B→C
1	0	1	1	B→C	Fault free
1	1	0	0	A→C	Fault free
1	1	0	1	A→D	A→C
1	1	1	0	A→D	A→C
1	1	1	1	A→C	Fault free

Table 10 Circuit switching network's fault tolerant analysis in front of stuck fault S1, S2 and S3 at 0 or 1 or stuck fault S1, S2 and S4 at 0 or 1

S1	S2	S3	S4	Expected path	S1 and S2 and S3 stuck-at 0 or 1 or S1 and S2 and S4 stuck-at 0 or 1 (faulty path)
0	0	0	0	A→C	Fault free A→D
0	0	0	1	A→D	A→C Fault free
0	0	1	0	A→D	A→C Fault free
0	0	1	1	A→C	Fault free A→D
0	1	0	0	B→C	A→C A→D
0	1	0	1	B→D	A→C A→D
0	1	1	0	B→D	A→C A→D
0	1	1	1	B→C	A→C A→D
1	0	0	0	B→C	A→C A→D
1	0	0	1	B→D	A→C A→D
1	0	1	0	B→D	A→C A→D
1	0	1	1	B→C	A→C A→D
1	1	0	0	A→C	Fault free A→D
1	1	0	1	A→D	A→C Fault free
1	1	1	0	A→D	A→C Fault free
1	1	1	1	A→C	Fault free A→D

Table 11 Circuit switching network's analysis under S1, S3 and S4 stuck-at 0 or 1 or S2, S3 and S4 stuck-at 0 or 1

S1	S2	S3	S4	Expected path	S1 and S3 and S4 stuck-at 0 or 1 or S2 and S3 and S4 stuck-at 0 or 1 (faulty path)
0	0	0	0	A → C	Fault free B → C
0	0	0	1	A → D	A → C B → C
0	0	1	0	A → D	A → C B → C
0	0	1	1	A → C	Fault free B → C
0	1	0	0	B → C	A → C Fault free
0	1	0	1	B → D	A → C B → C
0	1	1	0	B → D	A → C B → C
0	1	1	1	B → C	A → C Fault free
1	0	0	0	B → C	A → C Fault free
1	0	0	1	B → D	A → C B → C
1	0	1	0	B → D	A → C B → C
1	0	1	1	B → C	A → C Fault free
1	1	0	0	A → C	Fault free B → C
1	1	0	1	A → D	A → C B → C
1	1	1	0	A → D	A → C B → C
1	1	1	1	A → C	Fault free B → C

faulty path is our favor and there is no fault. But if stuck-at 0 or 1 occurs simultaneously on each control signals S1 and S2 for 0101 input, one of the fault situations 0001 or 1101 will happen. Therefore, the faulty path is A → D. The other input analysis method is same.

In Table 9(d), if stuck-at 0 or 1 occurs simultaneously on each control signals S1 and S3 for 1011 input, one of two situations 0001 or 1011 will happen. Therefore, the output paths will be one of B → C or A → D, which B → C has no fault and A → D path has fault. But if stuck-at 0 or 1 occurs simultaneously on each control signals S1 and S3 for 1101 input, one of two fault situations 0101 or 1111 will happen. Therefore, the output paths will be B → D or A → C, which they have faults. The other input analysis method is same.

In Table 9(e), if stuck-at 0 or 1 occurs simultaneously on each control signals S1 and S4 for input 0100, one of two situations 0100 or 1101 will happen. Therefore, the output path will be one of B → C or A → D, which B → C path has no fault and A → D path has fault. But if stuck-at 0 or 1 occurs simultaneously on each control signal S1 and S4 for input 1000, one of two fault situations 0000 or 1001 will happen. Therefore, the output paths are A → C and B → D, which they have faults. The other input analysis method is same.

In Table 9(f), if stuck-at 0 or 1 occurs simultaneously on each control signals S2 and S3 for input 0110, one of two situations 0110 or 0000 will happen. Therefore, the output paths will be B → D or A → C, which B → D path has no fault and A → C has fault. But if stuck-at 0 or 1 occurs

Table 12 Circuit switching network's fault tolerant analysis under S1, S2, S3 and S4 stuck-at 0 or 1

S1	S2	S3	S4	Expected path	S1 and S2 and S3 and S4 stuck-at 0 or 1 (faulty path)
0	0	0	0	A→C	Fault free
0	0	0	1	A→D	A→C
0	0	1	0	A→D	A→C
0	0	1	1	A→C	Fault free
0	1	0	0	B→C	A→C
0	1	0	1	B→D	A→C
0	1	1	0	B→D	A→C
0	1	1	1	B→C	A→C
1	0	0	0	B→C	A→C
1	0	0	1	B→D	A→C
1	0	1	0	B→D	A→C
1	0	1	1	B→C	A→C
1	1	0	0	A→C	Fault free
1	1	0	1	A→D	A→C
1	1	1	0	A→D	A→C
1	1	1	1	A→C	Fault free

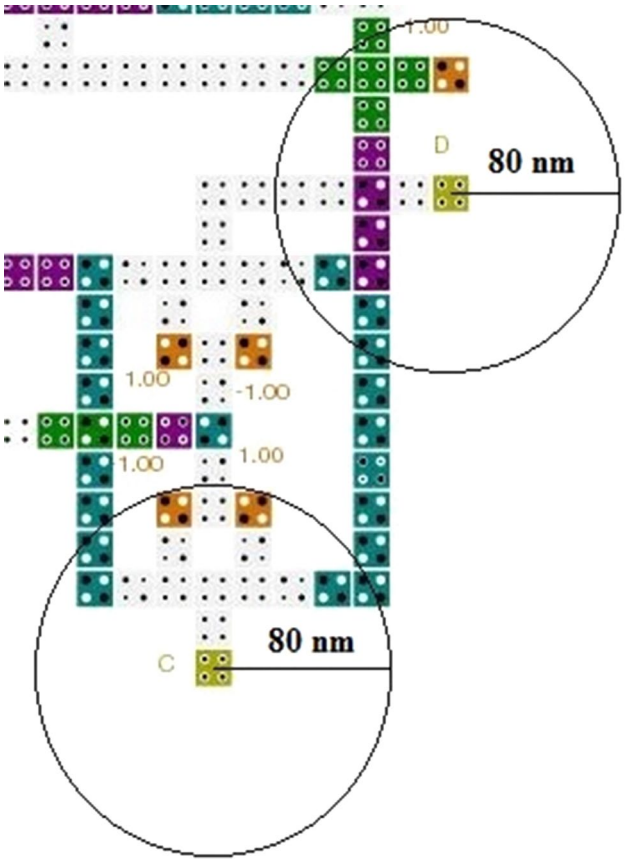


Fig. 13 Effect region on output cells

simultaneously on each control signals S2 and S3 for input 1010, one of two fault situations 1000 or 1110 will happen. Therefore, the output path will be B→C or A→D, which both of them have fault. The other input analysis method is same.

In Table 9(g), if stuck-at 0 or 1 occurs simultaneously on each control signals S2 and S4 for input 0010, one of the fault situations 0010 or 0111 will happen. Therefore, the output path is one of A→D or B→C, which A→D path has no fault and B→C path has fault. But if stuck-at 0 or 1 occurs simultaneously in each control signals S2 and S4 for input 0011, one of the fault situations 0010 or 0111 will happen. Therefore, the output fault path is A→D or B→C, which both of them have fault. The other input analysis method is same.

In Table 9(h), if stuck-at 0 or 1 occurs simultaneously on each two control signals S3 and S4 for input 1100, one of two situations 1100 or 1111 will happen. Therefore, the output path will be A→C, which is without fault. But if stuck-at 0 or 1 occurs simultaneously on each two control signals S3 and S4 for input 0001, one of two situations 0000 or 0011 will happen. Therefore, the output path is A→C which has fault. The other input analysis method is same.

Table 10 shows two situation of the fault tolerant analysis because the occurrence of stuck-at 0 or 1 on control signals S1, S2 and S3 causes the results as same as the occurrence of stuck-at 0 or 1 on control signals S1, S2 and S4. If stuck-at 0 or 1 occurs simultaneously on control signals S1, S2 and S3 for input 0010, one of two situations 0000 or 1110 will happen. Therefore, the output path is one of A→C and A→D paths, which A→C path has fault and A→D has no fault. So if stuck-at 0 or 1 occurs simultaneously on control signals S1, S2 and S4 for input 0010, one of two situations 0010 or 1111 will happen. Therefore, the output path is one of A→D and A→C paths, which A→D path has no fault and A→C has fault.

Table 11 shows two situations of the fault tolerant analysis because occurrence of stuck-at 0 or 1 on control signals S1, S3 and S4 have the result as same as occurrence of stuck-at 0 or 1 on control signals S2, S3 and S4. If stuck-at 0 or 1 occurs simultaneously on control signal S1, S3 and S4 for input 0110, one of two situations 0100 or 1111 will happen. Therefore, one of B→C and A→C is output path, which both of them have fault. So if stuck-at 0 or 1 occurs simultaneously on control signal S2, S3 and S4 for input 0110, one of two situations 0000 or 0111 will happen. Therefore, the output path will be one of A→C or B→C, which both of them have fault.

In Table 12, if stuck-at 0 or 1 occurs simultaneously on four control signals S1, S2, S3 and S4, for all possible input components, one of two situations 0000 or 1111 will happen which output path will be A→C. The A→C path

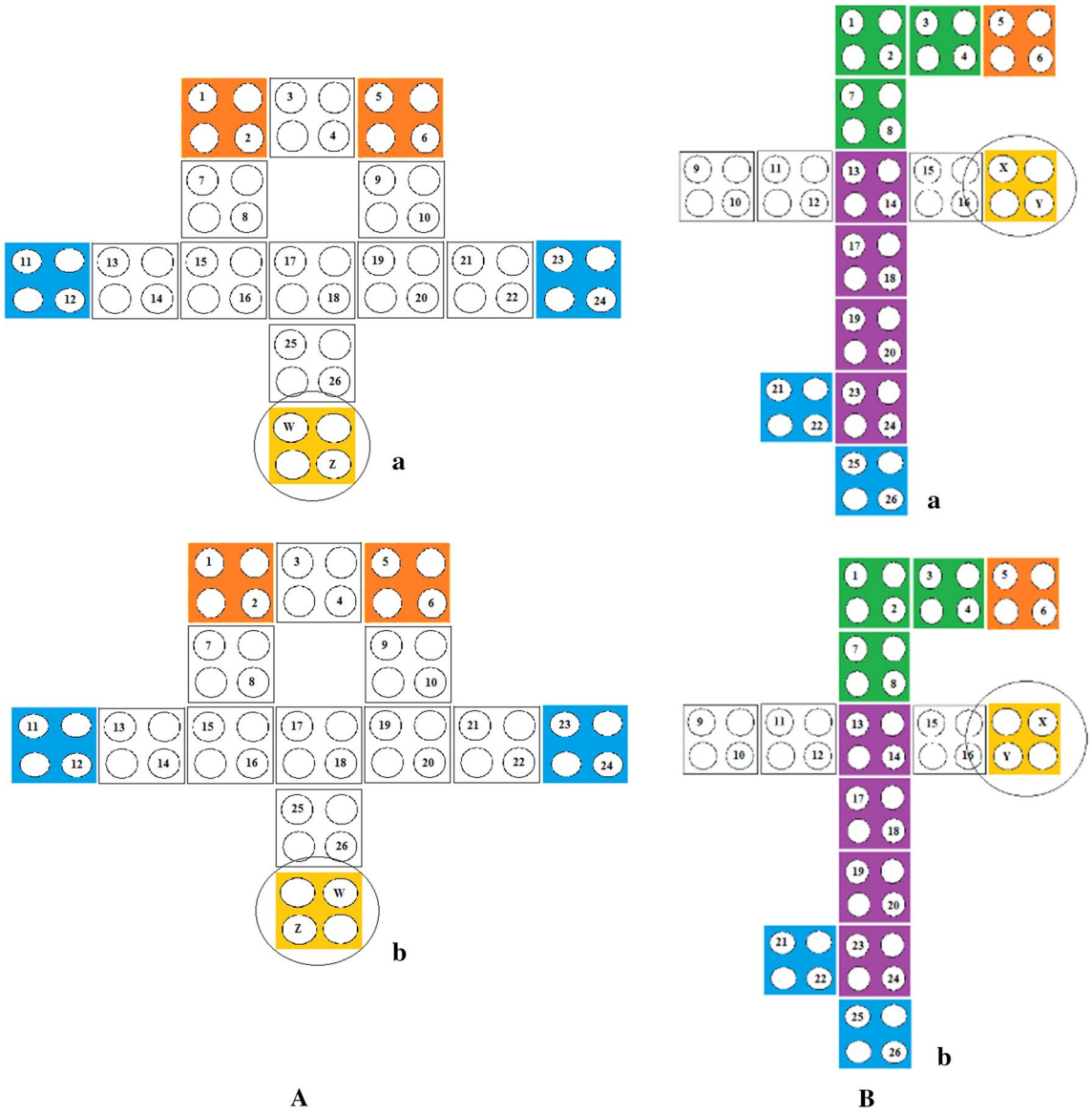


Fig. 14 **a** Numbered quantum points for the quantum cells and output C cell's polarization. **b** Numbered quantum points for the quantum cells and output D cell's polarization

Table 13 Calculation of the kink energy for output cell C in (a) the first situation in suggested circuit switching network and (b) the second situation in suggested circuit switching network

Electron W	Electron Z
(a) First situation in suggested circuit switching network	
$U_1 = 23.04\times10^{-29}/82.46\times10^{-9} = 0.27\times10^{-20}$ (J)	$U_1 = 23.04\times10^{-29}/105.1\times10^{-9} = 0.21\times10^{-20}$ (J)
$U_2 = 23.04\times10^{-29}/62.03\times10^{-9} = 0.37\times10^{-20}$ (J)	$U_2 = 23.04\times10^{-29}/82.46\times10^{-9} = 0.27\times10^{-20}$ (J)
$U_3 = 23.04\times10^{-29}/80\times10^{-9} = 0.28\times10^{-20}$ (J)	$U_3 = 23.04\times10^{-29}/99.63\times10^{-9} = 0.23\times10^{-20}$ (J)
$U_4 = 23.04\times10^{-29}/64.56\times10^{-9} = 0.35\times10^{-20}$ (J)	$U_4 = 23.04\times10^{-29}/80\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_5 = 23.04\times10^{-29}/82.46\times10^{-9} = 0.27\times10^{-20}$ (J)	$U_5 = 23.04\times10^{-29}/98.02\times10^{-9} = 0.23\times10^{-20}$ (J)
$U_6 = 23.04\times10^{-29}/72.71\times10^{-9} = 0.31\times10^{-20}$ (J)	$U_6 = 23.04\times10^{-29}/82.46\times10^{-9} = 0.27\times10^{-20}$ (J)
$U_7 = 23.04\times10^{-29}/63.24\times10^{-9} = 0.36\times10^{-20}$ (J)	$U_7 = 23.04\times10^{-29}/86.76\times10^{-9} = 0.26\times10^{-20}$ (J)
$U_8 = 23.04\times10^{-29}/42.04\times10^{-9} = 0.54\times10^{-20}$ (J)	$U_8 = 23.04\times10^{-29}/63.24\times10^{-9} = 0.36\times10^{-20}$ (J)
$U_9 = 23.04\times10^{-29}/63.24\times10^{-9} = 0.36\times10^{-20}$ (J)	$U_9 = 23.04\times10^{-29}/78.02\times10^{-9} = 0.29\times10^{-20}$ (J)
$U_{10} = 23.04\times10^{-29}/56.63\times10^{-9} = 0.40\times10^{-20}$ (J)	$U_{10} = 23.04\times10^{-29}/63.24\times10^{-9} = 0.36\times10^{-20}$ (J)
$U_{11} = 23.04\times10^{-29}/72.11\times10^{-9} = 0.31\times10^{-20}$ (J)	$U_{11} = 23.04\times10^{-29}/97.20\times10^{-9} = 0.23\times10^{-20}$ (J)
$U_{12} = 23.04\times10^{-29}/47.41\times10^{-9} = 0.48\times10^{-20}$ (J)	$U_{12} = 23.04\times10^{-29}/72.11\times10^{-9} = 0.31\times10^{-20}$ (J)
$U_{13} = 23.04\times10^{-29}/56.56\times10^{-9} = 0.40\times10^{-20}$ (J)	$U_{13} = 23.04\times10^{-29}/82.02\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_{14} = 23.04\times10^{-29}/31.11\times10^{-9} = 0.74\times10^{-20}$ (J)	$U_{14} = 23.04\times10^{-29}/56.56\times10^{-9} = 0.40\times10^{-20}$ (J)
$U_{15} = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)	$U_{15} = 23.04\times10^{-29}/69.33\times10^{-9} = 0.33\times10^{-20}$ (J)
$U_{16} = 23.04\times10^{-29}/22.09\times10^{-9} = 1.04\times10^{-20}$ (J)	$U_{16} = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)
$U_{17} = 23.04\times10^{-29}/40\times10^{-9} = 0.57\times10^{-20}$ (J)	$U_{17} = 23.04\times10^{-29}/60.72\times10^{-9} = 0.37\times10^{-20}$ (J)
$U_{18} = 23.04\times10^{-29}/28.42\times10^{-9} = 0.81\times10^{-20}$ (J)	$U_{18} = 23.04\times10^{-29}/40\times10^{-9} = 0.57\times10^{-20}$ (J)
$U_{19} = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)	$U_{19} = 23.04\times10^{-29}/58.03\times10^{-9} = 0.39\times10^{-20}$ (J)
$U_{20} = 23.04\times10^{-29}/43.90\times10^{-9} = 0.52\times10^{-20}$ (J)	$U_{20} = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)
$U_{21} = 23.04\times10^{-29}/56.56\times10^{-9} = 0.40\times10^{-20}$ (J)	$U_{21} = 23.04\times10^{-29}/62.03\times10^{-9} = 0.37\times10^{-20}$ (J)
$U_{22} = 23.04\times10^{-29}/62.03\times10^{-9} = 0.37\times10^{-20}$ (J)	$U_{22} = 23.04\times10^{-29}/56.56\times10^{-9} = 0.40\times10^{-20}$ (J)
$U_{23} = 23.04\times10^{-29}/72.11\times10^{-9} = 0.31\times10^{-20}$ (J)	$U_{23} = 23.04\times10^{-29}/71.61\times10^{-9} = 0.32\times10^{-20}$ (J)
$U_{24} = 23.04\times10^{-29}/81.04\times10^{-9} = 0.28\times10^{-20}$ (J)	$U_{24} = 23.04\times10^{-29}/72.11\times10^{-9} = 0.31\times10^{-20}$ (J)
$U_{25} = 23.04\times10^{-29}/20\times10^{-9} = 1.15\times10^{-20}$ (J)	$U_{25} = 23.04\times10^{-29}/42.04\times10^{-9} = 0.54\times10^{-20}$ (J)
$U_{26} = 23.04\times10^{-29}/18.11\times10^{-9} = 1.27\times10^{-20}$ (J)	$U_{26} = 23.04\times10^{-29}/20\times10^{-9} = 1.15\times10^{-20}$ (J)
$U_{TW} = 13.18\times10^{-20}$ (J)	$U_{TZ} = 9.74\times10^{-20}$ (J)
$U_T = 22.92\times10^{-20}$ (J)	
Electron W	Electron Z
(b) Second situation in suggested circuit switching network	
$U_1 = 23.04\times10^{-29}/88.56\times10^{-9} = 0.26\times10^{-20}$ (J)	$U_1 = 23.04\times10^{-29}/100.01\times10^{-9} = 0.23\times10^{-20}$ (J)
$U_2 = 23.04\times10^{-29}/65.14\times10^{-9} = 0.35\times10^{-20}$ (J)	$U_2 = 23.04\times10^{-29}/80.02\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_3 = 23.04\times10^{-29}/82\times10^{-9} = 0.28\times10^{-20}$ (J)	$U_3 = 23.04\times10^{-29}/98\times10^{-9} = 0.23\times10^{-20}$ (J)
$U_4 = 23.04\times10^{-29}/62\times10^{-9} = 0.37\times10^{-20}$ (J)	$U_4 = 23.04\times10^{-29}/82\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_5 = 23.04\times10^{-29}/80.02\times10^{-9} = 0.28\times10^{-20}$ (J)	$U_5 = 23.04\times10^{-29}/100.01\times10^{-9} = 0.23\times10^{-20}$ (J)
$U_6 = 23.04\times10^{-29}/65.14\times10^{-9} = 0.35\times10^{-20}$ (J)	$U_6 = 23.04\times10^{-29}/88.56\times10^{-9} = 0.26\times10^{-20}$ (J)
$U_7 = 23.04\times10^{-29}/71.02\times10^{-9} = 0.32\times10^{-20}$ (J)	$U_7 = 23.04\times10^{-29}/80.52\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_8 = 23.04\times10^{-29}/46.51\times10^{-9} = 0.49\times10^{-20}$ (J)	$U_8 = 23.04\times10^{-29}/60.03\times10^{-9} = 0.38\times10^{-20}$ (J)
$U_9 = 23.04\times10^{-29}/60.03\times10^{-9} = 0.38\times10^{-20}$ (J)	$U_9 = 23.04\times10^{-29}/80.52\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_{10} = 23.04\times10^{-29}/46.51\times10^{-9} = 0.49\times10^{-20}$ (J)	$U_{10} = 23.04\times10^{-29}/71.02\times10^{-9} = 0.32\times10^{-20}$ (J)
$U_{11} = 23.04\times10^{-29}/87.65\times10^{-9} = 0.26\times10^{-20}$ (J)	$U_{11} = 23.04\times10^{-29}/83.45\times10^{-9} = 0.27\times10^{-20}$ (J)
$U_{12} = 23.04\times10^{-29}/63.90\times10^{-9} = 0.36\times10^{-20}$ (J)	$U_{12} = 23.04\times10^{-29}/58\times10^{-9} = 0.39\times10^{-20}$ (J)
$U_{13} = 23.04\times10^{-29}/70.45\times10^{-9} = 0.32\times10^{-20}$ (J)	$U_{13} = 23.04\times10^{-29}/70.45\times10^{-9} = 0.32\times10^{-20}$ (J)
$UU_{14} = 23.04\times10^{-29}/45.65\times10^{-9} = 0.50\times10^{-20}$ (J)	$U_{14} = 23.04\times10^{-29}/45.65\times10^{-9} = 0.50\times10^{-20}$ (J)
$U_{15} = 23.04\times10^{-29}/55.17\times10^{-9} = 0.41\times10^{-20}$ (J)	$U_{15} = 23.04\times10^{-29}/61.35\times10^{-9} = 0.37\times10^{-20}$ (J)
$U_{16} = 23.04\times10^{-29}/29.73\times10^{-9} = 0.77\times10^{-20}$ (J)	$U_{16} = 23.04\times10^{-29}/40.04\times10^{-9} = 0.57\times10^{-20}$ (J)
$U_{17} = 23.04\times10^{-29}/43.86\times10^{-9} = 0.52\times10^{-20}$ (J)	$U_{17} = 23.04\times10^{-29}/58\times10^{-9} = 0.39\times10^{-20}$ (J)

Table 13 (continued)

Electron W	Electron Z
$U_{18}=23.04\times10^{-29}/22\times10^{-9}=1.04\times10^{-20}$ (J)	$U_{18}=23.04\times10^{-29}/43.86\times10^{-9}=0.52\times10^{-20}$ (J)
$U_{19}=23.04\times10^{-29}/40.04\times10^{-9}=0.57\times10^{-20}$ (J)	$U_{19}=23.04\times10^{-29}/61.35\times10^{-9}=0.37\times10^{-20}$ (J)
$U_{20}=23.04\times10^{-29}/29.73\times10^{-9}=0.77\times10^{-20}$ (J)	$U_{20}=23.04\times10^{-29}/55.17\times10^{-9}=0.41\times10^{-20}$ (J)
$U_{21}=23.04\times10^{-29}/45.65\times10^{-9}=0.50\times10^{-20}$ (J)	$U_{21}=23.04\times10^{-29}/70.45\times10^{-9}=0.32\times10^{-20}$ (J)
$U_{22}=23.04\times10^{-29}/45.65\times10^{-9}=0.50\times10^{-20}$ (J)	$U_{22}=23.04\times10^{-29}/70.45\times10^{-9}=0.32\times10^{-20}$ (J)
$U_{23}=23.04\times10^{-29}/58\times10^{-9}=0.39\times10^{-20}$ (J)	$U_{23}=23.04\times10^{-29}/83.45\times10^{-9}=0.27\times10^{-20}$ (J)
$U_{24}=23.04\times10^{-29}/63.90\times10^{-9}=0.36\times10^{-20}$ (J)	$U_{24}=23.04\times10^{-29}/87.65\times10^{-9}=0.26\times10^{-20}$ (J)
$U_{25}=23.04\times10^{-29}/26.90\times10^{-9}=0.85\times10^{-20}$ (J)	$U_{25}=23.04\times10^{-29}/38\times10^{-9}=0.60\times10^{-20}$ (J)
$U_{26}=23.04\times10^{-29}/2\times10^{-9}=11.52\times10^{-20}$ (J)	$U_{26}=23.04\times10^{-29}/26.90\times10^{-9}=0.85\times10^{-20}$ (J)
$U_{TW}=23.21\times10^{-20}$ (J)	$U_{TZ}=9.5\times10^{-20}$ (J)
$U_{T}=32.71\times10^{-20}$ (J)	

has no fault for inputs 0000, 0011, 1100 and 1111 and has fault for other inputs.

5 Calculation of kink's energy for proposed circuit-switched network

A cell polarization of the quantum-dot cellular automata is determined by coulomb interaction between cells. According to Eq. 1, the difference between electrostatic energies of two polarized neighbor cells is named kink energy [33].

$$E_{\text{kink}} = E_{\text{opp.polarization}} - E_{\text{same.polarization}} \tag{1}$$

Figure 13 shows the effect region on the output cells of the suggested circuit switching network.

The difference of kink energy is calculated between two neighbor cells i and j, which the cell i is taken constant in one situation and the cell j gets polarized in both of the situations. Equation 2 shows the kink energy calculation between two neighbor cells [33].

$$E_{i,j} = E_{i,j\,\text{opp.polarization}} - E_{i,j\,\text{same.polarization}} \tag{2}$$

Figure 14a, b shows numbered quantum points for the quantum cells, as well as the polarization of output cells D and C.

At first, the electrostatic energy of each cell and its effect on output is calculated by Eq. 3 to compute kink energy [33, 34].

$$U = K\,Q_1Q_2/R = 23.04\times10^{-29}/R \tag{3}$$

The calculated kink energy for suggested circuit switching network is equal with sum of electrostatic energies of all cells. The results of the calculations are shown, respectively, in Tables 13(a), (b) and 14(a), (b) for polarized situation of the output cells C and D. It is considered that the quantum cell's size is taken 18×18 nm and the distance between two neighbor cells is taken 2 nm.

Each output cell has stable situation which they have less kink energy. Based on Table 13(a) and (b), output cell C has less kink energy in the first situation, and therefore, the first situation is more stable. Also, the results of Table 14(a) and (b) show that the output cell D has lower kink energy in first situation, and therefore, the first situation is more stable.

6 Evaluation results and conclusion

The main purpose of the paper is presenting a fault tolerant circuit-switched network with the lowest cells, delay and complexity. Also, the operation of presented circuit is analyzed physically. The designed circuit switching networks by we and Jadav Chandra Das are compared and analyzed in details in Tables 15, 16 and 17, and in general in Table 18.

As shown in Table 15, the presented crossbar switch has 75% less delay and 85% less cell number than Jadav Chandra Das's design [31]. Also, the presented crossbar switch's fault tolerant has 5% more than Jadav Chandra Das's crossbar switch with two test vector. The presented crossbar switch has 100% fault tolerant with three test vector.

As shown in Table 16, the presented transmitter circuit has 58% less delay and 41% less cell number. The fault tolerant of transmitter circuit presented in part 4-2 is analyzed, and the results show that it has 100% fault tolerant.

As shown in Table 17, the presented receiver circuit has 58% less delay and 46% less cell number than Jadav Chandra

Table 14 Calculation of the kink energy for output cell D in (a) the first situation in suggested circuit switching network and (b) the second situation in suggested circuit switching network

Electron X	Electron Y
(a) First situation in suggested circuit switching network	
$U_1 = 23.04\times10^{-29}/56.56\times10^{-9} = 0.40\times10^{-20}$ (J)	$U_1 = 23.04\times10^{-29}/82.02\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_2 = 23.04\times10^{-29}/31.11\times10^{-9} = 0.74\times10^{-20}$ (J)	$U_2 = 23.04\times10^{-29}/56.56\times10^{-9} = 0.40\times10^{-20}$ (J)
$U_3 = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)	$U_3 = 23.04\times10^{-29}/69.33\times10^{-9} = 0.33\times10^{-20}$ (J)
$U_4 = 23.04\times10^{-29}/22.09\times10^{-9} = 1.04\times10^{-20}$ (J)	$U_4 = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)
$U_5 = 23.04\times10^{-29}/40\times10^{-9} = 0.57\times10^{-20}$ (J)	$U_5 = 23.04\times10^{-29}/60.72\times10^{-9} = 0.37\times10^{-20}$ (J)
$U_6 = 23.04\times10^{-29}/28.42\times10^{-9} = 0.81\times10^{-20}$ (J)	$U_6 = 23.04\times10^{-29}/40\times10^{-9} = 0.57\times10^{-20}$ (J)
$U_7 = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)	$U_7 = 23.04\times10^{-29}/69.33\times10^{-9} = 0.33\times10^{-20}$ (J)
$U_8 = 23.04\times10^{-29}/22.09\times10^{-9} = 1.04\times10^{-20}$ (J)	$U_8 = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)
$U_9 = 23.04\times10^{-29}/80\times10^{-9} = 0.28\times10^{-20}$ (J)	$U_9 = 23.04\times10^{-29}/99.63\times10^{-9} = 0.23\times10^{-20}$ (J)
$U_{10} = 23.04\times10^{-29}/64.56\times10^{-9} = 0.35\times10^{-20}$ (J)	$U_{10} = 23.04\times10^{-29}/80\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_{11} = 23.04\times10^{-29}/60\times10^{-9} = 0.38\times10^{-20}$ (J)	$U_{11} = 23.04\times10^{-29}/80.04\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_{12} = 23.04\times10^{-29}/45.69\times10^{-9} = 0.50\times10^{-20}$ (J)	$U_{12} = 23.04\times10^{-29}/60\times10^{-9} = 0.38\times10^{-20}$ (J)
$U_{13} = 23.04\times10^{-29}/40\times10^{-9} = 0.57\times10^{-20}$ (J)	$U_{13} = 23.04\times10^{-29}/60.72\times10^{-9} = 0.37\times10^{-20}$ (J)
$U_{14} = 23.04\times10^{-29}/28.42\times10^{-9} = 0.81\times10^{-20}$ (J)	$U_{14} = 23.04\times10^{-29}/40\times10^{-9} = 0.57\times10^{-20}$ (J)
$U_{15} = 23.04\times10^{-29}/20\times10^{-9} = 1.15\times10^{-20}$ (J)	$U_{15} = 23.04\times10^{-29}/42.04\times10^{-9} = 0.54\times10^{-20}$ (J)
$U_{16} = 23.04\times10^{-29}/18.11\times10^{-9} = 1.27\times10^{-20}$ (J)	$U_{16} = 23.04\times10^{-29}/20\times10^{-9} = 1.15\times10^{-20}$ (J)
$U_{17} = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)	$U_{17} = 23.04\times10^{-29}/58.03\times10^{-9} = 0.39\times10^{-20}$ (J)
$U_{18} = 23.04\times10^{-29}/43.90\times10^{-9} = 0.52\times10^{-20}$ (J)	$U_{18} = 23.04\times10^{-29}/44.72\times10^{-9} = 0.51\times10^{-20}$ (J)
$U_{19} = 23.04\times10^{-29}/56.56\times10^{-9} = 0.40\times10^{-20}$ (J)	$U_{19} = 23.04\times10^{-29}/62.03\times10^{-9} = 0.37\times10^{-20}$ (J)
$U_{20} = 23.04\times10^{-29}/62.03\times10^{-9} = 0.37\times10^{-20}$ (J)	$U_{20} = 23.04\times10^{-29}/56.56\times10^{-9} = 0.40\times10^{-20}$ (J)
$U_{21} = 23.04\times10^{-29}/84.85\times10^{-9} = 0.27\times10^{-20}$ (J)	$U_{21} = 23.04\times10^{-29}/88.58\times10^{-9} = 0.26\times10^{-20}$ (J)
$U_{22} = 23.04\times10^{-29}/88.58\times10^{-9} = 0.26\times10^{-20}$ (J)	$U_{22} = 23.04\times10^{-29}/84.85\times10^{-9} = 0.27\times10^{-20}$ (J)
$U_{23} = 23.04\times10^{-29}/72.11\times10^{-9} = 0.31\times10^{-20}$ (J)	$U_{23} = 23.04\times10^{-29}/71.61\times10^{-9} = 0.32\times10^{-20}$ (J)
$U_{24} = 23.04\times10^{-29}/81.04\times10^{-9} = 0.28\times10^{-20}$ (J)	$U_{24} = 23.04\times10^{-29}/72.11\times10^{-9} = 0.31\times10^{-20}$ (J)
$U_{25} = 23.04\times10^{-29}/89.44\times10^{-9} = 0.25\times10^{-20}$ (J)	$U_{25} = 23.04\times10^{-29}/84.89\times10^{-9} = 0.27\times10^{-20}$ (J)
$U_{26} = 23.04\times10^{-29}/100.43\times10^{-9} = 0.22\times10^{-20}$ (J)	$U_{26} = 23.04\times10^{-29}/89.44\times10^{-9} = 0.25\times10^{-20}$ (J)
$U_{TX} = 14.32\times10^{-20}$ (J)	$U_{TY} = 10.45\times10^{-20}$ (J)
$U_T = 24.77\times10^{-20}$ (J)	
Electron X	Electron Y
(b) Second situation in suggested circuit switching network	
$U_1 = 23.04\times10^{-29}/70.45\times10^{-9} = 0.32\times10^{-20}$ (J)	$U_1 = 23.04\times10^{-29}/70.45\times10^{-9} = 0.32\times10^{-20}$ (J)
$U_2 = 23.04\times10^{-29}/45.65\times10^{-9} = 0.50\times10^{-20}$ (J)	$U_2 = 23.04\times10^{-29}/45.65\times10^{-9} = 0.50\times10^{-20}$ (J)
$U_3 = 23.04\times10^{-29}/55.17\times10^{-9} = 0.41\times10^{-20}$ (J)	$U_3 = 23.04\times10^{-29}/61.35\times10^{-9} = 0.37\times10^{-20}$ (J)
$U_4 = 23.04\times10^{-29}/29.73\times10^{-9} = 0.77\times10^{-20}$ (J)	$U_4 = 23.04\times10^{-29}/40.04\times10^{-9} = 0.57\times10^{-20}$ (J)
$U_5 = 23.04\times10^{-29}/43.86\times10^{-9} = 0.52\times10^{-20}$ (J)	$U_5 = 23.04\times10^{-29}/58\times10^{-9} = 0.39\times10^{-20}$ (J)
$U_6 = 23.04\times10^{-29}/22\times10^{-9} = 1.04\times10^{-20}$ (J)	$U_6 = 23.04\times10^{-29}/43.86\times10^{-9} = 0.52\times10^{-20}$ (J)
$U_7 = 23.04\times10^{-29}/61.35\times10^{-9} = 0.37\times10^{-20}$ (J)	$U_7 = 23.04\times10^{-29}/55.17\times10^{-9} = 0.41\times10^{-20}$ (J)
$U_8 = 23.04\times10^{-29}/40.04\times10^{-9} = 0.57\times10^{-20}$ (J)	$U_8 = 23.04\times10^{-29}/29.73\times10^{-9} = 0.77\times10^{-20}$ (J)
$U_9 = 23.04\times10^{-29}/98\times10^{-9} = 0.23\times10^{-20}$ (J)	$U_9 = 23.04\times10^{-29}/82\times10^{-9} = 0.28\times10^{-20}$ (J)
$U_{10} = 23.04\times10^{-29}/82\times10^{-9} = 0.28\times10^{-20}$ (J)	$U_{10} = 23.04\times10^{-29}/62\times10^{-9} = 0.37\times10^{-20}$ (J)
$U_{11} = 23.04\times10^{-29}/78\times10^{-9} = 0.29\times10^{-20}$ (J)	$U_{11} = 23.04\times10^{-29}/62.64\times10^{-9} = 0.36\times10^{-20}$ (J)
$U_{12} = 23.04\times10^{-29}/62.64\times10^{-9} = 0.36\times10^{-20}$ (J)	$U_{12} = 23.04\times10^{-29}/42\times10^{-9} = 0.54\times10^{-20}$ (J)
$U_{13} = 23.04\times10^{-29}/58\times10^{-9} = 0.39\times10^{-20}$ (J)	$U_{13} = 23.04\times10^{-29}/43.86\times10^{-9} = 0.52\times10^{-20}$ (J)
$U_{14} = 23.04\times10^{-29}/43.86\times10^{-9} = 0.52\times10^{-20}$ (J)	$U_{14} = 23.04\times10^{-29}/22\times10^{-9} = 1.04\times10^{-20}$ (J)
$U_{15} = 23.04\times10^{-29}/38\times10^{-9} = 0.60\times10^{-20}$ (J)	$U_{15} = 23.04\times10^{-29}/26.90\times10^{-9} = 0.85\times10^{-20}$ (J)
$U_{16} = 23.04\times10^{-29}/26.90\times10^{-9} = 0.85\times10^{-20}$ (J)	$U_{16} = 23.04\times10^{-29}/2\times10^{-9} = 11.52\times10^{-20}$ (J)
$U_{17} = 23.04\times10^{-29}/61.35\times10^{-9} = 0.37\times10^{-20}$ (J)	$U_{17} = 23.04\times10^{-29}/40.04\times10^{-9} = 0.57\times10^{-20}$ (J)

Table 14 (continued)

Electron X	Electron Y
$U_{18}=23.04\times10^{-29}/55.17\times10^{-9}=0.41\times10^{-20}$ (J)	$U_{18}=23.04\times10^{-29}/29.73\times10^{-9}=0.77\times10^{-20}$ (J)
$U_{19}=23.04\times10^{-29}/70.45\times10^{-9}=0.32\times10^{-20}$ (J)	$U_{19}=23.04\times10^{-29}/45.65\times10^{-9}=0.50\times10^{-20}$ (J)
$U_{20}=23.04\times10^{-29}/70.45\times10^{-9}=0.32\times10^{-20}$ (J)	$U_{20}=23.04\times10^{-29}/45.65\times10^{-9}=0.50\times10^{-20}$ (J)
$U_{21}=23.04\times10^{-29}/98.40\times10^{-9}=0.23\times10^{-20}$ (J)	$U_{21}=23.04\times10^{-29}/73.23\times10^{-9}=0.31\times10^{-20}$ (J)
$U_{22}=23.04\times10^{-29}/98.40\times10^{-9}=0.23\times10^{-20}$ (J)	$U_{22}=23.04\times10^{-29}/73.23\times10^{-9}=0.31\times10^{-20}$ (J)
$U_{23}=23.04\times10^{-29}/83.45\times10^{-9}=0.27\times10^{-20}$ (J)	$U_{23}=23.04\times10^{-29}/58\times10^{-9}=0.39\times10^{-20}$ (J)
$U_{24}=23.04\times10^{-29}/87.65\times10^{-9}=0.26\times10^{-20}$ (J)	$U_{24}=23.04\times10^{-29}/63.90\times10^{-9}=0.36\times10^{-20}$ (J)
$U_{25}=23.04\times10^{-29}/98.81\times10^{-9}=0.23\times10^{-20}$ (J)	$U_{25}=23.04\times10^{-29}/73.78\times10^{-9}=0.31\times10^{-20}$ (J)
$U_{26}=23.04\times10^{-29}/105.84\times10^{-9}=0.21\times10^{-20}$ (J)	$U_{26}=23.04\times10^{-29}/82.96\times10^{-9}=0.27\times10^{-20}$ (J)
$U_{TX}=10.87\times10^{-20}$ (J)	$U_{TY}=23.62\times10^{-20}$ (J)
$U_{T}=34.49\times10^{-20}$ (J)	

Table 15 Comparing suggested crossbar switch with Jadav Chandra Das's crossbar switch

Structure	Delay (clock zone)	Cell number	Fault tolerant with 2 test vector (%)	Fault tolerant with 3 test vector
Proposed	2	52	95	100%
[31]	8	124	90	Not reviewed

Table 16 Comparing suggested transmitter circuit with Jadav Chandra Das's transmitter circuit

Structure	Delay (clock zone)	Cell number
Proposed	5	101
[31]	12	174

Table 17 Comparing suggested receiver circuit with Jadav Chandra Das's receiver circuit

Structure	Delay (clock zone)	Cell number
Proposed	5	88
[31]	12	166

Table 18 Comparing suggested circuit switching network with Jadav Chandra Das's circuit switching network

Structure	Delay (clock zone)	Cell number
Proposed	6	207
[31]	28	381

Das's design. The fault tolerant of receiver circuit presented in part 4-3 is analyzed, and the results show that it has 100% fault tolerant.

As shown in Table 18, the suggested circuit switching network has 78% less delay and 45% less cell number than Jadav Chandra Das's design. The fault tolerant of suggested circuit switching network is analyzed, and the results show that it has 100% fault tolerant.

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