ORIGINAL PAPER

Design of reversible parity generator and checker for the implementation of nano-communication systems in quantum-dot cellular automata

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Abstract

Complementary metal-oxide semiconductor (CMOS) technology may face so much problems in future due to the smaller size of transistors and increase in circuits' volume and chips temperature. A new technology that can be a good alternative to CMOS circuits is quantum-dot cellular automata (QCA). These technologies have features such as a very low power consumption, high speed and small dimensions. In nano-communication system, error detection and correction in a receiver message are major factors. In addition, circuit reversibility in QCA helps designs a lot. In this research, generator and checker circuit of the reversible parity and eventually their nano-communication system are designed reversible using odd parity bit. The proposed circuits and the theoretical values are tested by QCADesigner 2.0.3 simulator to show the correct operation of the circuits. According to the simulation results, the proposed circuits compared with the previous structure improve delay by 90–75–35% in generator and checker structures of parity and their reversibility of nano-communication system, respectively. The proposed circuits are used in nano-transmitters and nano-receivers.

Keywords Nano-communication system · Quantum-dot cellular automata · Parity generator · Parity checker · Reversible

1 Introduction

Reversibility processing is considered as one of the most important discussions in nanotechnology which is the complementary of CMOS technology, since CMOS technology has several physical constraints: one of them is large dimensions of CMOS technology compared with QCA [1]. QCA does not store logical value as voltage, but stores it in logical forms of 0 and 1, i.e., electrons' position is based on exclusive electrons' position inside the dots as shown in Fig. 1. Logical value 0 or the same of − 1 in 3-input majority gate shows AND function, and logical value 1 indicates OR function, as shown in Fig. 2 [1–6]. In QCA, the logical values that apply inside the points will initialize in a square which has 4 points at the corners and the points that are in the opposite corners will be occupied diagonally due to the electrons Coulomb repulsion force [7]. In fact, by initialize

to the point, polarity modes in QCA will be implemented. QCA has achieved very high operational speed due to the lack of voltage and less heat which can help improve circuit performance a lot. QCA cells have 4 phases: relax, release, hold and switch which have phase difference of 90° to each other. In switch phase, the cell is polarized due to the Coulomb interaction with the adjacent cells [8]. As soon as the cell reaches certain polarity, it retains its current mode in hold phase. Cell's polarity is reduced in release phase and finally disappears as soon as it reaches relax phase [8–21], as shown in Fig. 3. Various circuits are implemented by QCA in nano-communication devices for parity generator and parity checker which all of them have been tested and approved by QCADesigner, but most of the circuits are not reversible [22, 23]. In nano-circuits, reversibility plays an important role in error detection due to the lack of data loss and also having communication without loss. In addition, most of these irreversible circuits do not describe delay and cell's count separately. In [24], the parity generator and parity checker and their nano-communication circuit have been designed reversibly using odd parity bit, but their circuits have more cells and delay. Thus, in this paper, a circuit is proposed using exclusive-OR gate which is both reversible

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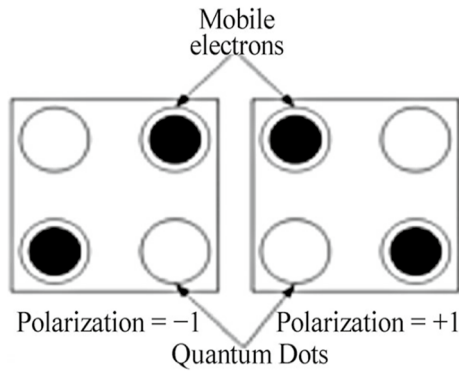
Fig. 1 QCA cell

and has much less cells than [24] circuits. All the circuits have been designed and approved by QCA Designer 2.0.3.

2 Pervious works

In this section, we review the previous structures.

2.1 Feynman gate

It is a 2×2 reversible gate. This gate has 2 inputs A, B mapped to the outputs P, Q as $P = A$ and $Q = A \oplus B$ [24]. Figure 4a, b shows the block diagram and QCA layout of it, respectively.

2.2 Reversible odd parity generator of Chandra et al.

Suppose that 3 inputs A, B, C are 3-bit massages which are to be sent and P_b is an odd parity generator, the operation of this circuit is that the output will be "1" when the number of 1 s in the message is even. In other words, all the inputs become "0" or one of the inputs is "0" [24]. According to

Table 1, it can be found that odd parity bit will be achieved from XNOR result of three inputs A, B, C. The block diagram and QCA layout of Chandra et al. using Feynman gate are shown in Fig. 5a, b, respectively. Truth table of the circuit is shown in Table 1.

In Fig. 5, the reversible odd parity generator circuit is designed by 2 Feynman gates and 6 majority gates in which GAR1 and GAR2 are garbage values.

2.3 Reversible odd parity checker of Chandra et al.

Odd parity checker controls the transmitted data from parity generator and checks its validity. If the parity output of the 4 bits (3 message bits plus parity bit) is even, an error will occur during transmission. Therefore, the transmitted binary information is originally odd [24]. When an error occurs, the output value of the odd parity checker is "1" ($P_c = 1$(, i.e., the number of 1 s in 4 bits is even. Table 2 shows the truth table of reversible odd parity checker.

Block diagram and QCA layout of reversible odd parity checker circuit from Chandra et al. using Feynman gate are shown in Fig. 6a, b, respectively.
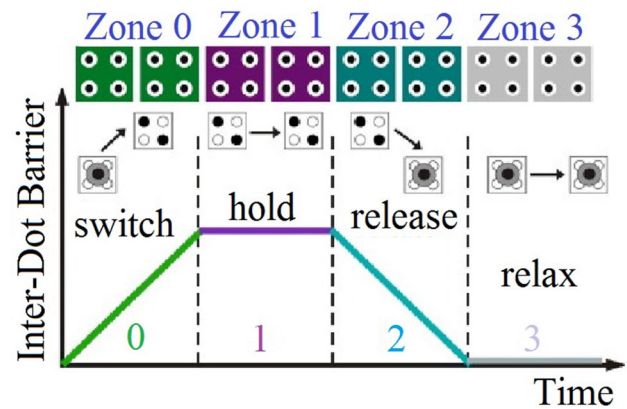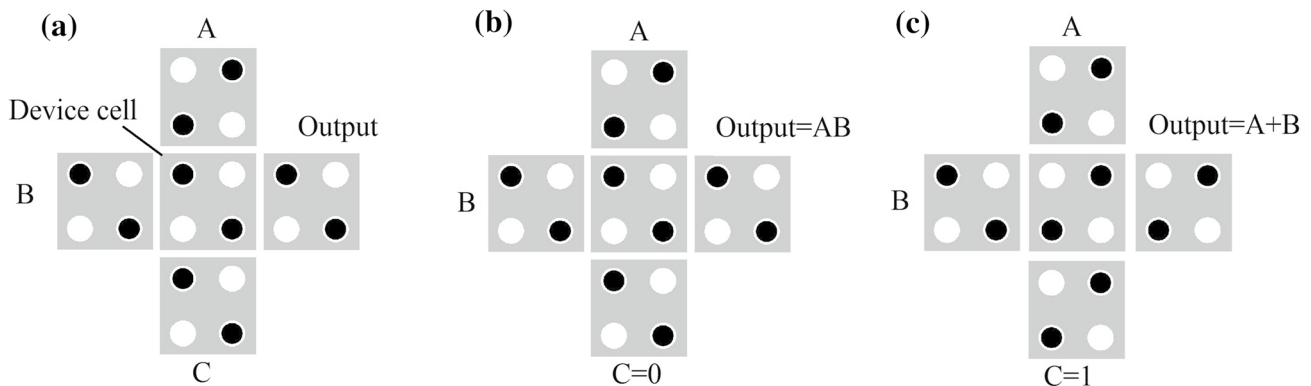

Fig. 3 Clocking phases in QCA

Fig. 2 **a** Majority gate, **b** AND gate, **c** OR gate

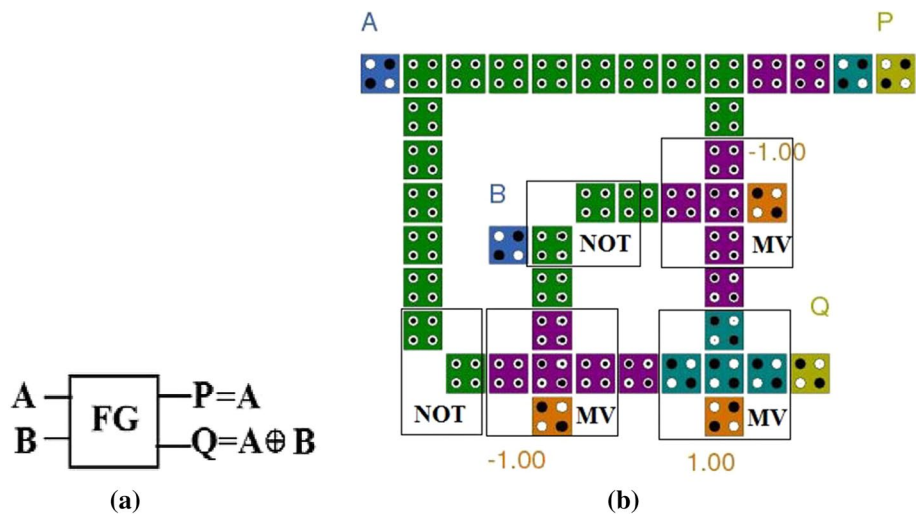**Fig. 4** Feynman gate **a** block diagram, **b** QCA layout

Table 1 Truth table of the reversible odd parity generator

3-bit message			Generated parity bit P_b
A	B	C	
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

2.4 Nano-communication system of parity generator and parity checker circuit from Chandra et al.

Figure 7a, b shows QCA block diagram and QCA layout of nano-communication system of the parity generator and

parity checker circuit from Chandra et al. using gates in Figs. 5b and 6b.

2.5 3-Input Exclusive-OR gate

Figure 8a, b shows block diagram and QCA layout of an exclusive-OR gate, respectively. It has low complexity and is very high speed. Similar to 5-input majority gate, it has 11 QCA cells which is known as TIEO or three-input exclusive-OR [25]. Table 3 shows the truth table of TIEO gate.

2.6 2-Input Exclusive-OR gate

Figure 9 is a 2-input XOR. This gate unlike other gates uses explicit interactions between QCA cells. In fact, no majority gate is used in this gate. So, it has a significant reduction in area, delay and number of cells [26].
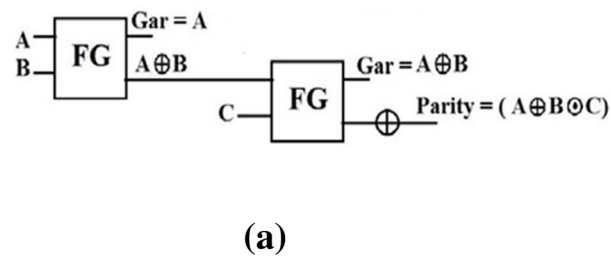

Fig. 5 The reversible odd parity generator circuit using the Feynman gate **a** block diagram, **b** QCA layout

Table 2 Truth table of the reversible odd parity checker

4-bit message (including parity bit P_b)				Parity bit error check
A	B	C	P_b	P_c
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

3 Proposed circuit of reversible odd parity checker and generator

In this section, we explain the proposed structures.

3.1 Proposed reversible odd parity generator

Suppose that 3 inputs A, B, C are 3-bit messages that are to be transmitted. P_b is output of parity generator. P_b parity bit is such that all 1 s in the message are odd.

The truth table is shown in Table 4. With regard to the truth table, it can be found that the output will be 1 when the number of 1 s in the message is even or one of the inputs is zero. In this case, $P_b = 1$; otherwise, $P_b = 0$.

Figure 10a, b shows block diagram and QCA layout of the proposed reversible odd parity generator, respectively. The proposed circuit is designed using TIEO gate which in fact XOR values of inputs A, B, C and garbage values of GAR1, GAR2 will be generated by TIEO gate. Eventually, the generated XOR value will propagate through inverter gate and will generate XNOR value of inputs A, B, C which is the same odd parity generator.

3.2 Proposed reversible odd parity checker

Odd parity checker controls the transmitted data from parity generator and checks its validity. If the parity output of the 4 bits (3-bit message bits plus parity bit) is even, an error will occur during transmission [27]. When an error occurs, the output value of the odd parity checker is "1" ($P_c = 1($, i.e., the number of 1 s in 4 bits is even. Table 5 shows the truth table of proposed reversible odd parity checker.

According to the truth table shown in Table 5, the circuit of proposed reversible odd parity checker will result from XNOR inputs A, B, C and P_b. Therefore, block diagram and QCA layout of the proposed reversible odd parity checker circuit are shown in Fig. 11a, b, respectively. According to Fig. 11a, in fact XOR will generate 3-input XOR A, B, C, i.e., $A \oplus B \oplus C$ with 2 garbage values equal to inputs A, C firstly. Then, the generated XOR value of inputs A, B, C will generate output $A \oplus B \oplus C \oplus P_b$ through 2-input XOR gate with P_b. The generated output value $A \oplus B \oplus C \oplus P_b$ with the garbage value equal to $A \oplus B \oplus C$ will be propagated
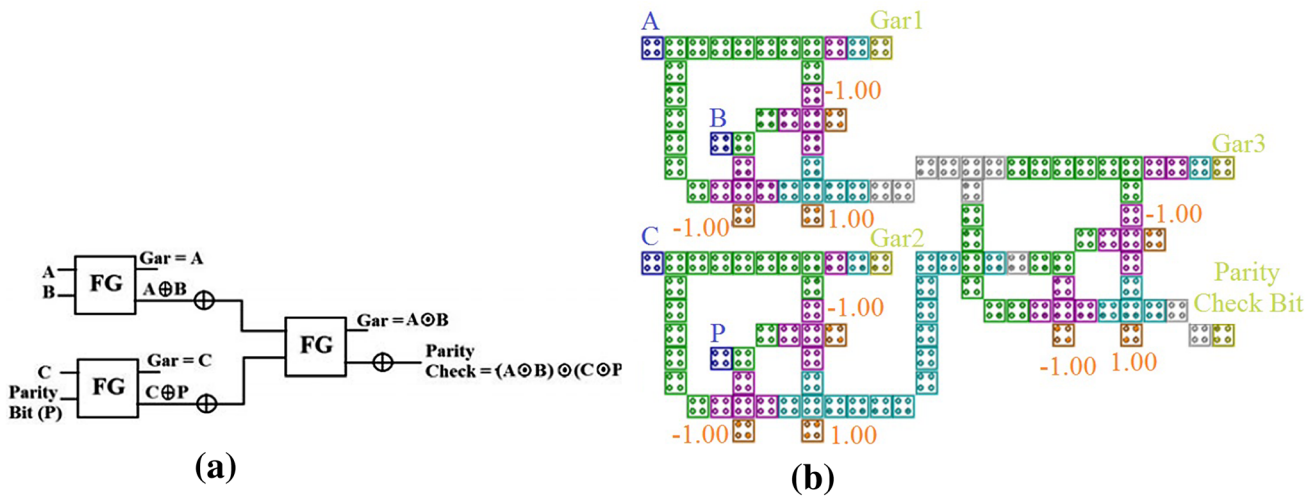

Fig. 6 The reversible odd parity checker circuit using the Feynman gate **a** block diagram, **b** QCA layout
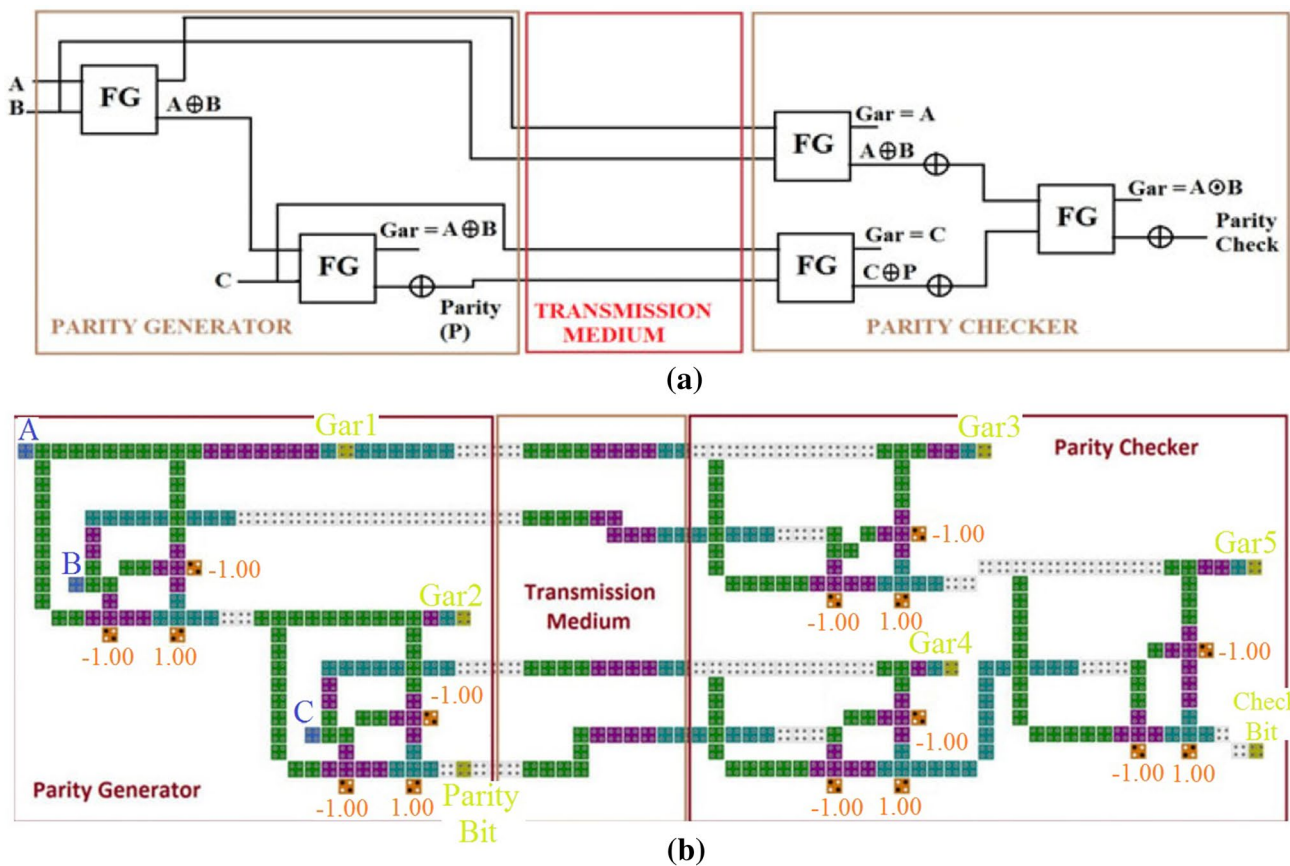
Fig. 7 Reversible nano-communication system **a** block diagram; **b** QCA layout
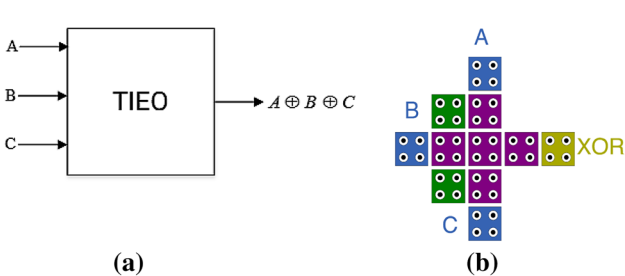
Fig. 8 TIEO gate **a** block diagram; **b** QCA layout

Fig. 9 2-Input XOR gate in QCA

Table 3 Truth table of the TIEO

A	B	C	Output
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 4 Truth table of proposed reversible odd parity generator circuit

A	B	C	GAR1	GAR2	Parity bit
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	1	0

Fig. 10 The proposed revers-
ible odd parity generator
circuit using the TIEO **a** block
diagram; **b** QCA layout

(a)

(b)

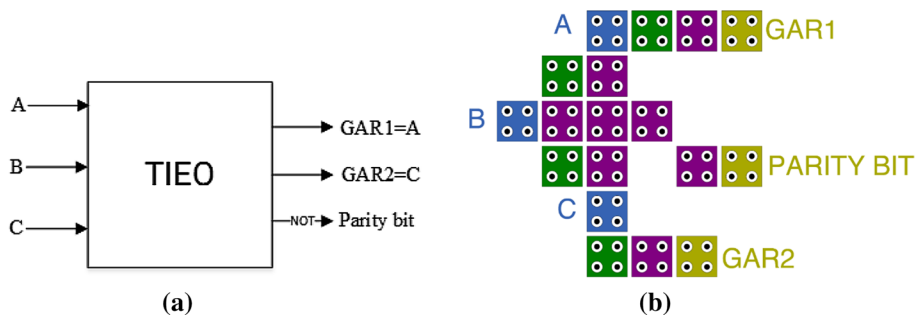**Table 5** Truth table of proposed reversible odd parity checker circuit

A	B	C	P_b	GAR1	GAR2	GAR3	Parity bit error check
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	1
0	1	0	0	0	0	1	0
0	1	0	1	0	0	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

through reversible NOT gate, and finally, the output of odd parity checker will be generated (Fig. 12).

3.3 Nano-communication system of the proposed reversible odd parity checker generating circuit

Architectural operation of the proposed nano-communication system is as follow.

The parity generator receives 3-bit message as input at the end of the transmitter and generates parity bit with 2 garbage values equal to values A, C. Then, 3-bit message and parity bit are transmitted to destination by communication media that these data move along with the parity checker circuit. At the end of receiver, the parity checker controls the validity of parity bit and input data which comes from transmitter.

Table 6 shows the truth table of proposed nano-communication system for the proposed reversible odd parity checker and generator circuit. According to this table, if the output of the 4-bit parity bit (3 bits message plus parity bit) is even, the error will be occurred. The truth table of nano-communication system is achieved considering

odd parity generator values in Table 4. Therefore, inputs of nano-communication system's transmitter are the same as shown in Table 4 which will cause all the outputs of odd parity checker bit in receiver be ended to zero. More precisely, according to the truth table shown in Table 6b, when a 3-bit message with odd parity generator bits become XNOR, all the outputs of odd parity checker will be zero.

4 Simulation results

The proposed circuits are studied and evaluated using QCADesigner 2.0.3 simulator. Then, they are compared with previous structures in terms of complexity, i.e., number of cells, area and delay by the results derived from this evaluation, and finally, it is applicable with QCAPro. Power dissipation of the circuits is analyzed. Instability of related simulator is estimated by parameters shown in Table 7.
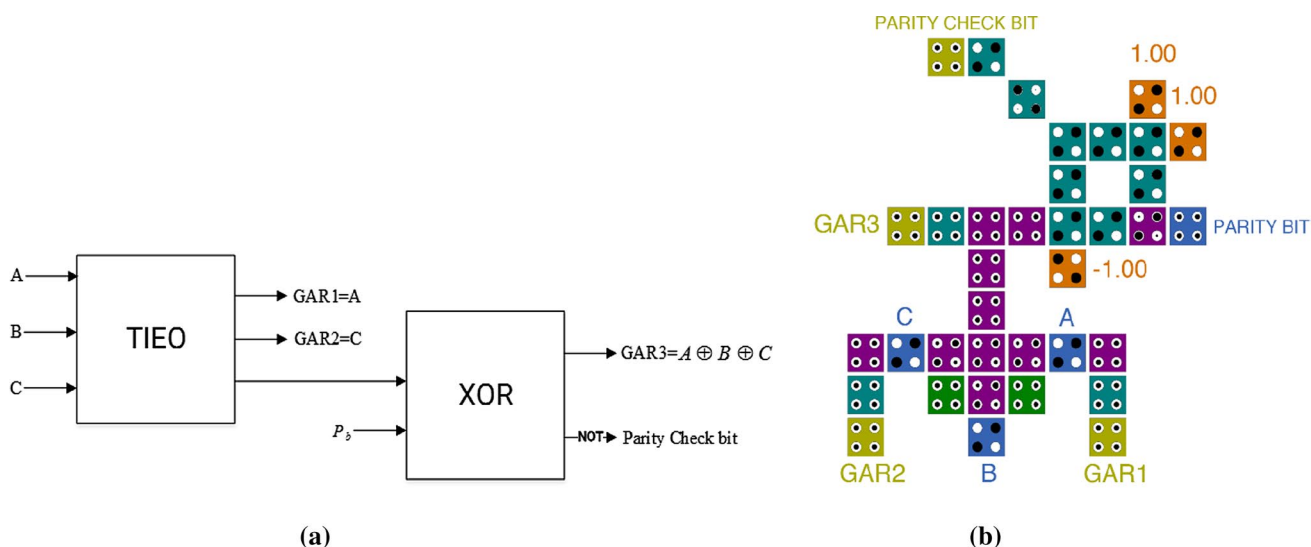
Fig. 11 The proposed reversible odd parity checker circuit using the TIEO **a** block diagram; **b** QCA layout

4.1 Simulation results of the proposed reversible odd parity generator

Figure 13a shows simulation results of the proposed reversible odd parity generator. According to Fig. 13a, if the inputs are $A = 1$, $B = 1$, $C = 1$, the outputs will be GAR2 = 1, GAR1 = 1 and parity bit = 0, and if $A = 1$, $B = 1$, $C = 1$, the outputs will be GAR2 = 0, GAR1 = 1 and parity bit = 0. So, the operation of the circuit according to Table 4 is correct. Simulation results are tested and approved by the values shown in Table 4. GAR1 and GAR2 are considered as garbage outputs.

4.2 Simulation results of the proposed reversible odd parity checker

Figure 13b shows simulation results of the proposed reversible odd parity checker. According to Fig. 13b, if the inputs are $A = 1$, $B = 1$, $C = 1$ and parity bit = 1, the output's values will be GAR1 = 1, GAR3 = 1, GAR2 = 1 and parity check bit = 1. Also other input modes are checked and tested according to Table 5. Thus, according to Table 5, the proposed reversible odd parity checker circuit operates properly. GAR1, GAR2 and GAR3 are garbage values.

4.3 Simulation results of nano-communication system for the proposed reversible odd parity checker and generator

Nano-communication system is composed of 2 parts of transmitter and receiver. In fact, transmitter side is the proposed reversible odd parity generator and the proposed reversible odd parity checker is placed in receiver side to control error. Simulation results of nano-communication system are described in both transmitter and receiver parts.

1. *Transmitter part* According to Fig. 13c, when inputs of parity generator are $A = 1$, $B = 1$, $C = 1$, the outputs will be GAR2 = 1, GAR1 = 1 and parity bit = 0 and when $A = 1$, $B = 1$, $C = 0$, outputs will be GAR2 = 0, GAR1 = 1 and parity bit = 1. Also other input and output compounds are tested and approved according to Table 6a. GAR1 and GAR2 are garbage values.
2. *Receiver part* In nano-communication circuit, since parity generator and checker are merged, it is necessary to apply a clocking cycle after parity generator circuit structure to prevent interference between receiver and transmitter parts. Then, parity checker circuit should be developed. Outputs of receiver part, i.e., the garbage values of GAR5, GAR4, GAR3 and parity checker, appeared with 2 delay clock cycles. Outputs of this part are tested and approved according to Table 6.

4.4 Complexity of designing proposed structures

Table 8 shows complexities of proposed design in number of cells, occupied area and delay. According to Table 8, the proposed reversible odd parity generator has 18 cells which are reduced by 74% compared with the structure of Chandra et al. [24]. Also the occupied area of the proposed parity generator structure is 0.03, that is, improved about 72% compared with [24] structure. Finally, delay of the proposed parity generator structure is 0.25 which is improved 90% compared with [24] structure.

Structure of the proposed reversible parity checker according to Table 8 has 36 cells, that is, improved about

Fig. 12 Proposed nano-communication system: **a** block diagram; **b** QCA layout

(a)

(b)
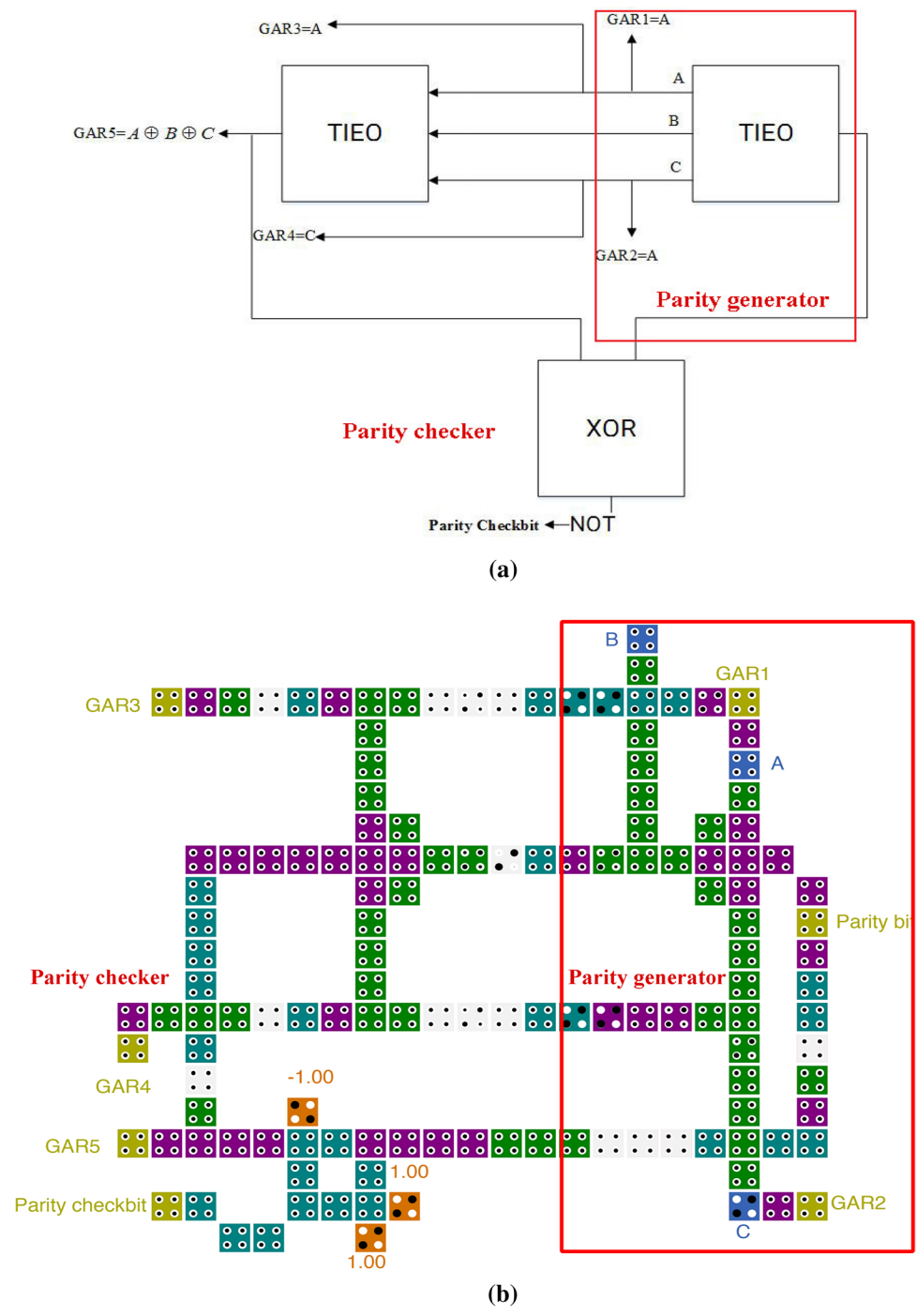
72% compared with [24] structure. The occupied area of the above-mentioned structure is 0.07, and its delay is 0.5 which is improved 60% and 75%, respectively, in comparison with [24] structure.

Structure of the proposed reversible nano-communication system has 137 cells that have about 65% cell reduction compared with [24] structure. In addition, with the occupied area of 0.28 and delay of 2.5 compared with the

structure of Chandra et al. [24], it is improved 62% and 37%, respectively.

According to Table 8, as explained, the proposed structures have made significant improvement compared with Chandra et al. structures. Improvement percentage is inserted in Table 9 completely.

Thus, with regard to Table 9, delay of the proposed structures of reversible odd parity checker and generator

Table 6 Truth table of proposed reversible odd parity generator and checker circuit

Parity generator (transmitter)

3-bit message			Garbage values		Generated parity bit
A	B	C	GAR1	GAR2	Parity bit
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	1	0

Parity checker (receiver)

4-bit message				Garbage values					Parity checker bit
A	B	C	P_b	GAR1	GAR2	GAR3	GAR4	GAR5	Parity check bit
0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	1	0	1	1	0
0	1	0	0	0	0	0	0	1	0
0	1	1	1	0	1	0	1	0	0
1	0	0	0	1	0	1	0	1	0
1	0	1	1	1	1	1	1	0	0
1	1	0	1	1	0	1	0	0	0
1	1	1	0	1	1	1	1	1	0

Table 7 Bistable parameters in QCADesigner 2.0.3

Parameter	Value
QCA cell width	18 nm
QCA cell height	18 nm
Quantum-dot diameter	5 nm
Amplitude factor	2.0000
Clock high	9.80000e−22 J
Clock low	3.80000e−23 J
Number of samples	12,800
Radius of effect	65.00 nm
Relative permittivity	12.900
Layer separation	11.50000 nm
Coverage tolerance	0.001000

be calculated through total power dissipation, majority and inverter gates and array of QCA cells [28].

Power dissipation computing software, QCAPro, is used to calculate power dissipation of the proposed circuits, which is applicable in Linux operating system. Power dissipation of the circuits is achieved in temperature $T = 2$ K and tunneling energies of 1.5 E_K, 1 E_K, 0.5 E_K.

Power dissipation of reversible parity checker and generator and nano-communication circuit structures is shown in Table 10a–c, respectively.

Table 11 shows improvement percentage of power dissipation of the proposed structures compared with Chandra et al. structures [24].

and nano-communication circuit is reduced 90%, 75% and 37.5%, respectively.

4.5 Power dissipation analysis

Power consumption of QCA circuit depends on logical gates used in circuit design [28]. Using logical gates such as majority gate and inverter gate will cause more power in the circuit. Thus, dissipated energy of QCA circuit will

5 Conclusion

In recent years, CMOS technologies would not be a suitable approach to design circuits in nano-scale due to their physical constraints. Because as mentioned earlier, this technology has problems such as leakage, noise and much power dissipation. Therefore, QCA technology is a suitable alternative to CMOS, since this technology could achieve less occupied area, less power dissipation and also less delay.

Fig. 13 Simulation results of QCA layout of the **a** odd parity generator, **b** odd parity checker, **c** nano-communication circuit

Table 8 Complexity of the proposed circuits

Circuits		Number of cells	Total area (μm²)	Latency (clock cycle)
Proposed circuits	Reversible odd parity generator	18	0.03	0.25
	Reversible odd parity checker	36	0.07	0.5
	Nano-communication circuit	137	0.28	2.5
Previous circuits [24]	Reversible odd parity generator	71	0.11	2.5
	Reversible odd parity checker	130	0.20	2
	Nano-communication circuit	397	0.74	4

Table 9 Improvements percentage of complexities of the proposed circuits compared with Chandra circuits

Proposed circuits	Number of cells (%)	Total area (%)	Latency (%)
Reversible odd parity generator	74.64	72.72	90
Reversible odd parity checker	72.30	60	75
Nano-communication circuit	65.49	62.19	37.5

In nano-communication systems, error detection in receiver message is a key factor to transmit information. Parity bit is considered as one of error detection approaches in data transmission. Reversible odd parity checker and generator are proposed using exclusive-OR gate or the same TIEO. In this study, the main goal is to optimize previous structures in terms of number of cells, area and delay. The proposed structure nearly reduces power dissipation due to its reversibility. In addition, the proposed structure reduces number of cells, area and delay significantly compared with the previous structure.

In the proposed structures unlike previous structures, no majority gate is used and circuits are designed by exclusive-OR gates. These structures are checked by QCADesigner 2.0.3 Simulator Software. Parity checker and generator have a wide application in nano-communication circuits. The proposed circuits can be used to design nano-communication architecture in nano-scale such as nano-transmitter and nano-receivers.

Table 10 Analysis of energy consumption of (a) reversible odd parity generator, (b) reversible odd parity checker, (c) nano-communication circuit

Structure	Avg. leakage energy dissipation (ev)			Avg. switching energy dissipation (ev)			Total energy dissipation (ev)		
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
(a)									
[24]	0.02368	0.06891	0.12046	0.08206	0.06982	0.05866	0.10574	0.13873	0.17912
Proposed	0.00616	0.01675	0.02817	0.0148	0.01204	0.00996	0.02096	0.02879	0.03813
(b)									
[24]	0.04121	0.12326	0.21855	0.18747	0.16033	0.13505	0.22868	0.28359	0.3536
Proposed	0.01282	0.03563	0.06036	0.03157	0.02544	0.02068	0.04439	0.06107	0.08104
(c)									
[24]	0.12256	0.37606	0.67476	0.47224	0.40462	0.34041	0.5948	0.78068	1.01517
Proposed	0.04691	0.13736	0.23987	0.16954	0.14262	0.11885	0.21645	0.27998	0.35872

Table 11 Improvements percentage of energy consumption of the proposed circuits compared with Chandra circuits

Structure	Avg. leakage energy dissipation (ev)			Avg. switching energy dissipation (ev)			Total energy dissipation (ev)		
	0.5 E_k (%)	1 E_k (%)	1.5 E_k (%)	0.5 E_k (%)	1 E_k (%)	1.5 E_k (%)	0.5 E_k (%)	1 E_k (%)	1.5 E_k (%)
Reversible odd parity generator	73.99	75.69	76.61	81.96	82.76	83.02	80.18	79.25	78.71
Reversible odd parity checker	68.89	71.09	72.38	83.16	84.13	84.69	80.59	78.46	77.08
Nano-communication circuit	61.72	63.47	64.45	64.1	64.75	65.09	63.61	64.14	64.66

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