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ORIGINAL PAPER

# Design of a loop-based random access memory based on the nanoscale quantum dot cellular automata

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**Abstract**
The use of modern quantum dot cellular automata (QCA) on the nanoscale gives better results than complementary metal–oxide–semiconductor (CMOS) technology such as diminution power consumption, augmentation clock frequency and device density enhancement. Thereupon, it becomes a substantial technology for forming whole varieties of memory. Random access memory (RAM) is an essential element of any computer set where the operating system, application programs and data can be kept to rapidly admonition via the main processor. The RAM is extremely swifter to read from and write into other kinds of the computer storages. There are some QCA cells for memory structures, wherein their specifications are used to design more optimized structures than CMOS. The offered techniques in the previous studies lead to extend in the consumption area, and the circuit complexity. So, in this paper a new single-bit QCA-based RAM is proposed to overcome these weaknesses. Ultimately, $4 \times 1$ RAM is designed by applying the single-bit memory. The operational authenticity of the offered layouts is demonstrated utilizing QCADesigner. Also, the QCAPro tool is utilized for calculating the dissipated energy of the circuit. The obtained results have indicated that the offered design has a smaller number of cells, low complexity and low wire crossing. Also, the wasted area has optimized based on the one-level loop-based structure. The suggested D-latch has 24 QCA cells, and the wasted area is 0.02 $\mu m^2$. Each memory structure in RAM layout has the wasted area of 0.06 $\mu m^2$ and 55 QCA cells. Finally, the obtained results have confirmed that the proposed design improves cell numbers and wasted area.

**Keywords** Quantum dot cellular automata · Random access memory · D-latch · Nanoscale · Energy consumption · Nanoelectronics

## 1 Introduction

By reducing the scalability of complementary metal–oxide–semiconductor (CMOS) technology, several obstacles in this technology such as high power consumption and leakage current prevent the reduction in size of the circuits' dimension. Therefore, the scholars endeavor to discover a solution or a superseded technology [1–3]. The quantum dot cellular automata (QCA) is the best alternative to CMOS technology using the Coulombic interactions between the cells [4–6]. The QCA is considered as one of the superior six technologies that have the ability to be used in computational circuits in designing future computers. The robust attributes of QCA are confirmed by modeling research and circuit design [7–10]. This technique is organized for smaller and more effectual circuits using the interposition of quantum physics and nanotechnology in electronics. The QCA is similar to the binary logic models of computer architecture [11, 12]. The incomparable feature is that logic states do not accumulate at the voltage level and they are demonstrated by a cell. A nanoscale cell consists of two electrons that can encode data. The cells must be aligned exactly on nanoscales to have better performance. The systems must be tested appropriately to identify defects and disorders. It is anticipated to realize low power consumption, high device density and very high clock frequency [7, 13, 14].

On the other hand, random access memory (RAM) is a method of data and information computer data storage preservation where their retrieval (read or write) is allowed. The RAM is formed in rows and columns to select the element of it, as well as writing and reading the data [15]. To retain the information and datum in the CMOS, a CMOS battery on the motherboard supplies stable power of chip. Whenever the

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battery is to be eliminated aboard the motherboard or picked up, the CMOS would erase the information which is stored in it [16–19]. Due to the weakness of CMOS-based RAM, the QCA-based RAM can be realized in two generic structures: line-based and loop-based layout. Storing in a line-based RAM cell is done by a QCA line as the primary element for the memory cell. The data in these structures move along a line forward and backward [20, 21]. Extra clock zones, which make the implementation complicated, are required for line-based RAM cells. In loop-based RAM cells, storage mechanism is prepared by circulating a bit in a closed QCA loop, which comprises of all four clocking zones that are explained. The loop-based RAM cells do not require the additional clock areas, and it causes the better performance of RAM [21].

Therefore, the main goal in this paper is designing a new loop-based single-layer RAM on the nanoscale using QCA. The level-sensitive D-latch model is offered for the main layer. Three AND gates, one OR gate, three NOT gates and one majority voter (MV) have been used in designing the proposed RAM. The significant role of the proposed RAM is synchronizing the writing and reading operation. Also, the $4 \times 1$ RAM has been designed to show the scalability of the design. Briefly, the main aims of this article are:

- Proposing a level-sensitive QCA-based D-latch.
- Presenting a mutual structure of loop-based RAM according to the proposed D-latch.
- Analyzing and evaluating speed, complexity, a number of cells, area consumption of the proposed and the state-of-the-art designs.
- Analyzing and calculating the dissipated energy of the circuit using QCAPro tool.
- Verifying the operation of the proposed design using QCADesigner tool.

The rest of this article is structured as follows: The state-of-the-art literature about QCA-based RAM layout is given in Sect. 2. The structure of loop-based RAM cells, a new style and layouts are offered in Sect. 3. Section 4 incorporates computing dissipated energy, power model of QCA technology and simulation outcomes. At last, the conclusions and future works are offered in Sect. 5.

## 2 Related work

In this section, the analysis of the literature for designing QCA-based RAM is considered and reviewed.

Walus and Vetteth [22] have described the layout of a QCA-based RAM and shown the layout of individual memory cells, as well as a layout for a $4 \times 1$ RAM. The designed RAM is based on a 2D grid of memory cells. The one-bit memory cells provide the layout of a simple Write/Read function that each of the memory cells in the RAM uses 158 QCA cells. Data in each memory cell are stored by means of a closed QCA wire loop (which is a partition by circa four clocking zones). Additionally, the clocking zones cannot be propagated between memory loops, and their dimensions are very small. Also, the memory cell entails a primary count of clocking zones, so the underlying CMOS layout for offering the necessary clocking signals is required. Assume that cells can be fabricated by 10 nm, causing memory capacities to reach over 1.6 Gbit/cm$^2$. There are more opportunities for its expansion that could lead to better capacitor density. Reducing the number of coplanar crossovers and possibly fault tolerant algorithms by increasing the fault tolerance. However, the speed and the wasted area of this RAM cell are not increased. Also, the long path between lines leads to increase the sensitivity of thermal variations and makes problem in its implementation. Also, it is difficult to measure the speed of the operation. Furthermore, the principal disadvantage of this approach is the same as [21].

Furthermore, Dehkordi and Shamsabadi [21] have offered two modified structures for a loop-based RAM cell. In the presented design, the inherent abilities of the QCA, such as the clocking mechanism and the programmability of majority gate, have been included. The first mentioned RAM based on SR-latch has two inputs and one output. A smaller number of cells are shared in this method, and the wasted area is contrasted to customary loop-based RAM cell. Each of the memory cells in the RAM uses 100 QCA structures. For the second structure, a new method has been offered to design D-latch and a RAM cell. Another memory cells in the RAM utilize 63 QCA structures. The executable time of memory has been replicated in attendance of a smaller count of cells. The irregular appointment of QCA cells in a QCA layout leads to have difficult realization. The drawback of this method is high area consumption and clocking cycle.

Also, Kianpour and Sabbaghi-Nadooshan [23] have provided a 16 bits RAM with three major goals such as optimized area, lower latency and improved Read/Write. The 2-to-4 decoder in the prime stage requires four 2-input AND gates. The input wire S1 is connected to required inverter gates, and the inputs of AND gates are connected to the input wire S0. Single column and single row are applied to run both decoders. Each memory cell in the decoder can be chosen with minimum delay. The importance of operational design stability is given by the maximum wire length in a clocking zone of 15 cells. The offered RAM cell will do the function by a minimum clock and can be applied in other circuits, such as FPGA, although the weakness of this method is a clocking cycle.

Furthermore, Hashemi and Navi [24] have offered a memory structure with set/reset capability and a powerful $2 \times 1$ multiplexer, efficacious edge-triggered and level-triggered

QCA-based D-flip flops. The input signal and the set/reset are two inputs of mux, and the select signal is applied to the select line of this element. Therefore, the output of the mux and the output signal of the circuit are two inputs of second mux, and the read/write signal is applied to choose the necessary value of it. The simulation outcomes have demonstrated that the offered layout has efficacious structures in the case of delay and complexity. The weakness of this style is high cell numbers and area consumption. Also, this method does not require any crossover wire.

Angizi and Sarmadi [25] have proposed a new robust five-input majority gate based on D-latch which is proper for implementation of simple and well-organized QCA layout in one layer. The majority gate takes every five input signals in the unique path at the prime clocking zone. This layout is formed by three 3-input majority gates and one 5-input majority gate. An offered RAM cell is organized by two separate set and reset signals. This layout has a simple and robust structure that supports minimal area, also reduces the hardware requests and clocking zone numbers. But, this design suffers from low speed.

At the end, Kianpour and Sabbaghi-Nadooshan [26] have implemented a $16 \times 32$-bit SRAM in QCA structure. 16-bit decoders and multiplexers in the QCA with low tallies of majority gates and cells also acts as a pipeline. The new SRAM, decoders and multiplexers are designed, executed and simulated applying a signal distribution network to avoid the coplanar problem of crossing wires. The offered SRAM has a reliable and mutable structure applying interconnections and programmable logic. In contradiction to other studies, the introduced memory cell acts as a pipeline then enhances the operating speed and reduction in the delay. Table 1 compares the reviewed related QCA-based RAM designs.

## 3 Proposed design

RAM structure is a fundamental component in several circuits; therefore, any optimization in its complexity and area is interesting. In this section, the layouts of the proposed QCA-based RAM are elaborated and other subsections suggest the main component of these layouts as a robust D-latch.

### 3.1 QCA design of D-latch

One of the important structures that are exerted in a RAM cell is D-latch, and the cell value is kept via a loop. Latches circuit can protect a binary state indefinitely directed by an input signal to switch states subject to the condition that as the power is delivered. Their outcomes are permanently affected by their inputs since the enable signal is confirmed. The enable signal usually controls the clock signal. The specification of D-latch utilizes one OR gate, one inverter and two AND gates for its designing. The offered D-latch instead of one OR gate and two AND gates used the majority gate and is illustrated in Fig. 1.

The QCA-based offered design needs one majority voter gate, and the design equation is $Q = M(IN, Q, \overline{Q}) = INQ + IN\overline{Q}$ as long as $IN\ \overline{IN} = 0$. The truth table of D-latch for amounts of $Q = 1$ and $Q = 0$ is explained in Table 2.

**Table 1** Summarization and comparison of the reviewed related works in the field of QCA-based RAM

| Paper | Advantages | Disadvantages |
|---|---|---|
| Walus [22] | Increasing the fault tolerance<br>Reducing the number of coplanar crossovers | Low speed<br>High area consumption |
| Dehkordi [21] | Reduced number of cells<br>Reduced area<br>High speed | High clocking cycle<br>High area consumption |
| Kianpour and Sabbaghi-Nadooshan [23] | Low area<br>Decreasing clock zone<br>Low cell numbers<br>Low delay | High power consumption |
| Hashemi and Navi [24] | Not need any crossover wire<br>Low delay<br>Decreasing complexity | High consumption area<br>High cell numbers |
| Angizi [25] | Low consumption area<br>Reduction in hardware requirements<br>Low delay | Low speed |
| Kianpour and Sabbaghi-Nadooshan [26] | Low delay<br>Low consumption area<br>High speed | High power consumption<br>Increasing complexity<br>High clocking cycle |

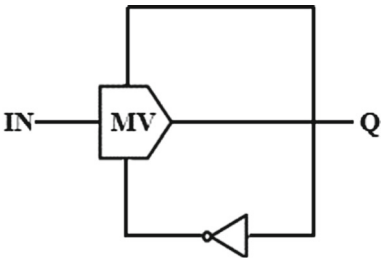


**Fig. 1** Circuit diagram of proposed D-latch

**Table 2** Truth table of D-latch with an initial value of Q = 1 and Q = 0

| IN | Q1 = $INQ'_{t-1} + INQ_{t-1}$ | Q2 = $INQ'_{t-1} + INQ_{t-1}$ |
|---|---|---|
| 0 | 1 (initial value) | 0 (initial value) |
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |

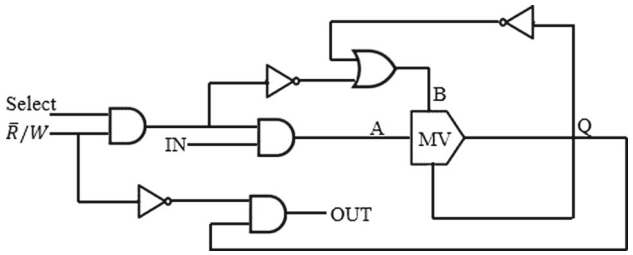


**Fig. 2** Circuit diagram of the proposed RAM cell

## 3.2 The proposed RAM cell structure

In this subsection, the D-latch-based RAM layout is offered. Each RAM structure has one output and two inputs. When $\bar{R}/W = 1$, the $\bar{R}/W$ is activated, and then the information is written to it. Therefore, if $\bar{R}/W = 0$, $\bar{R}/W$ input is deactivated, the output route opens, and the information can be read. A RAM cell has another input called *Select*. If the *Select* = '0', the output and the input amounts will be inactivated; accordingly, RAM cell will be deactivated. Three AND gates, one OR gate, three NOT gates and one majority voter have been added to the main cell structure, and the circuit diagram of the RAM cell is represented in Fig. 2.

The relating truth table of the offered RAM structure is expressed in Table 3. Three inputs of the majority voter are organized as Q, A and B, and the output of the majority voter (since S (Q, B, A) = Q($t$)) will be tantamount to Q($t$). When $\bar{R}/W$ is equivalent to '0' , the read function from a RAM cell is activated, the value of A is '0' (since '0' AND IN is

**Table 3** Truth table of the proposed RAM

| $\bar{R}/W$ | Input | Q | A | B | Q($t$) | Output |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | X |
| 1 | 0 | 1 | 0 | 0 | 0 | X |
| 1 | 1 | 0 | 1 | 1 | 1 | X |
| 1 | 1 | 1 | 1 | 0 | 1 | X |

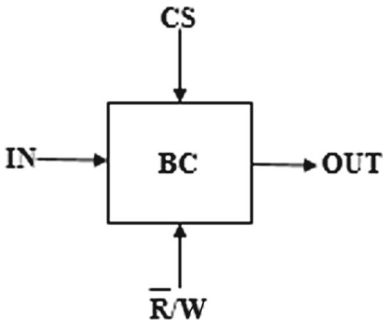


**Fig. 3** One-bit memory cell

equal to '0'), the value of B is '1' (since '1' OR Q is equal to '1'), then Q($t$) is equivalent to Q, the amount of output is equivalent to Q (since '1' AND Q($t$) is equal to Q), and then Q($t$) will be tantamount to Q as does output. Therefore, the write function from a RAM structure is evident as soon as $\bar{R}/W$ is tantamount to '1', the amount of A is equal to IN (since '1' AND IN is IN), and the value of B is equal to $\bar{Q}$ (since '0' OR Q is $\bar{Q}$), the amount of Output is '0', then output is '0', and Q($t$) is equivalent to input.

The basic cell (BC) is used to represent the memory structure. (The basic cell is applied in lieu of the memory structure.) Every cell subtends write and read operations, output, chip select and input as illustrated in Fig. 3.

The memory item cells are regular in 4 bits array to form a 1-bit memory as indicated in Fig. 4. The horizontal arrows are shorthand for the decoder rails (where outputs are displayed horizontally in OR chain), the data input rails, the $\bar{R}/W$ active rails and the OR chain rails. The clock cycle data on the arrows are used to decoder rails. The structure is founded on a simple 2D grid layout of memory cells. In an apparatus diagram for RAM, each memory cell in the RAM structure chooses one of two read or write functions. The word size of the RAM is specified via the number of memory cells in any of the rows and can be increased by simply memory cells. To increase the total valence of the RAM, the area address must be enhanced as well. The decoder uses two 2-input AND gates, the input wire S1 through inverter

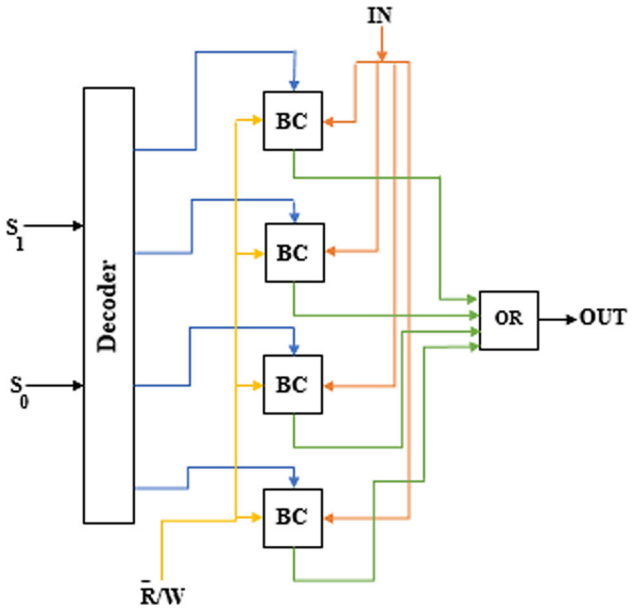


**Fig. 4** 4-bit RAM schematic

gates needed. The decoder can choose any unit of memory with minimum delay.

## 4 Simulation results

This section demonstrates the simulation environments in the prime subsection. The simulation parameters are determined in the next subsection. The QCA layout of offered designs, the comparison outcomes between the offered RAM cells architecture and previous designs and calculating the dissipated energy of the offered RAM applying QCA cells are defined in the following subsection.

### 4.1 Simulation environments

The QCADesigner is the results of determined investigation attempt via the Walus team at the University of British Columbia to organize a simulation and layout software for QCA cells [27]. This software is nevertheless under expansion and is free. The QCA is an extending significance in calculation nanotechnology to the perception of a computer utilizing arrays of nanoscale QCA layout [28, 29]. Its layouts are capable of performing any complicated computing functions which are necessary to make general calculations (inversion, fan-out and majority function). The QCADesigner software aids rapid attempt, layout and simulation of QCA structures by offering powerful CAD traits beneficial in more complex circuit layout tools [27].

On the other hand, the QCApro is a replacement package to the QCA package, via QCA 1.1.4 as its foundation [28, 30–33]. It implements the method of qualitative comparative analysis (QCA) techniques for analyzing configurationally data in accordance with the INUS theory of causation [34]. There are various technical and methodological problems in the QCA package, such as many new features and enhancements for applying QCA which provide multiple objective-built functions for experimenting attributes of QCA and QCA-related methods. Three common methods are used by QCApro, which are crisp-set QCA (csQCA) [35], multivalued QCA (mvQCA) [36] and fuzzy-set QCA (fsQCA) [37]. A sub-variant of csQCA called temporal QCA (tQCA) is also available [38]. Several datasets from different areas are united in QCApro so as to help familiarization with the package's functionality.

**Table 4** QCADesigner parameters model [25]

| Parameter | Value |
|---|---|
| Cell size | 18 nm |
| Number of samples | 50,000 |
| Convergence tolerance | 0.001000 |
| Radius of effect | 65.000000 nm |
| Relative permittivity | 12.900000 |
| Clock low | 3.800000e–023 J |
| Clock high | 9.800000e–022 J |
| Clock shift | 0 |
| Clock amplitude factor | 2.000000 |
| Layer separation | 11.500000 |
| Maximum iterations per sample | 100 |

### 4.2 Simulation parameters

The simulation outcomes of the offered layouts are confirmed applying the QCADesigner tool version 2.0.3 [25, 39, 43] with default parameters as illustrated in Table 4, and in this manner, the outcomes are obtained from both simulation engines (bistable approximation and coherence vector) of this tool. For D-latch, it is observed that the polarization at the output is $\pm 9.51e^{-001}$ (as to both $\bar{Q}$ and Q) through the bistable stability approximation and the selection of several coherence vectors via Euler manner. If instead of the temperature 1 °K, the assumption amount of 5 °K in coherence vector option preservation keeping the same manner, the corresponding amount of polarization is $\pm 9.\ 50e^{-001}$ (for $\bar{Q}$). However, the significant increase in the stage of 1 °K, for example, at 6 °K, the circuit cannot give the accurate result [25].

### 4.3 Layout of the proposed designs

The proposed level-sensitive D-latch is constructed from 24 cells, and the wasted area is 0.02 $\mu m^2$. The QCA-based

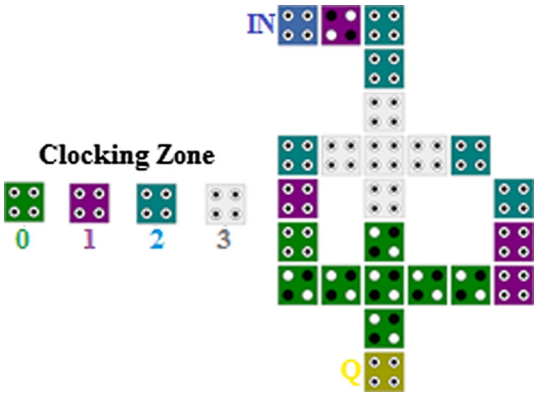


**Fig. 5** QCA layout of the offered D-latch

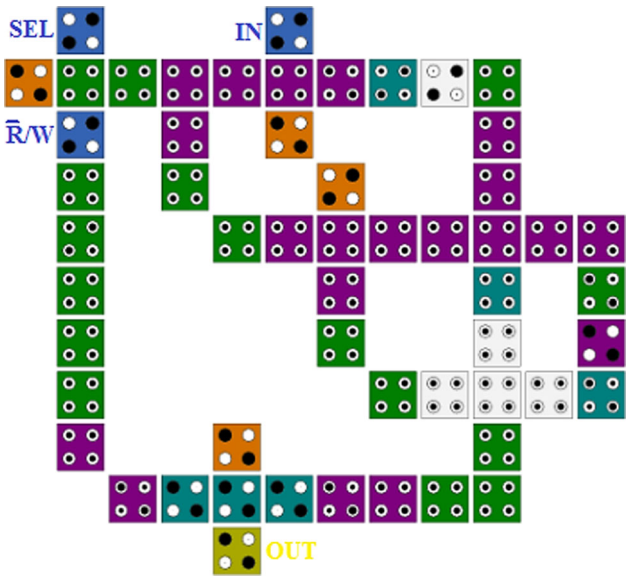


**Fig. 6** QCA layout of the offered RAM cell

D-latch design is illustrated in Fig. 5. The multi-phased clocking mechanism with appropriate information is required for designing. The several colors in the design indicate various clocking zones.

The QCA layout of the offered method is explained in Fig. 6. Single-layer RAM based on D-latch model over the conventional one is introduced its input–output delay which is composed of 2/5 clocking zones. One OR gate, three AND gates, three NOT gates and one majority voter have been applied in the offered RAM. The presented RAM layout applies 55 QCA cells, and the wasted area is 0.06 $\mu m^2$.

Addressing on any row of the QCA memory requires a decoder circuit which produces a ROW Select signal to allocate row in the memory based on a used address at the input. Applying the offered memory cell and the QCA decoder, a 2D addressable array can be created. In Fig. 7, a $4 \times 1$ QCA RAM is shown. The results of each cell are diffuse via a serial OR array. The usage of a serial OR array is obligatory because the equivalent of a tristate buffer does not exist in QCA technology. One of the inducements for applying this layout is larger sized memory is that the delay is proportional to the row length when the Row Select signal propagates to the output.

The outcomes of D-latch simulation for $Q=1$ (initial amount) are introduced in Fig. 8a and $Q=0$ (initial amount) in Fig. 8b that have been acquired via the simulator of QCA layout. Due to the simulation waveforms, the timing effect of D-latch for $Q=1$ and $Q=0$ is in accordance with the theoretical amounts as given in Table 2.

The simulation results of the introduced RAM scheme are reported in Fig. 9. When $\bar{R}$/W and the Select signals are activated by '+1' simultaneously, the output is demonstrated after 2.5 clock cycles delay and the result of waveform changes after 8 clock cycles. Whenever $\bar{R}$/W and Select signals are equal to '1' (enable), the write operation is written in the memory cell. In these figures, the inputs are blue, the yellow color represents the output, and the output delay of the proposed circuit is shown in red color. The output of the proposed RAM cell is shown as a single bit. The analysis of the output confirms the correctness of the offered circuit. The proposed RAM cell resolves the problem for prior structures with reducing cell number and area consumption. Also, the simulation of the offered $4 \times 1$ RAM scheme is specified in Fig. 10. As it is clear, if the *Input*=0, the value of output will be replaced at first BC and then, for *Input*=1, the value of output will be replaced at last BC. The proposed $4 \times 1$ RAM design uses 612 QCA cells, and the wasted area is 0.60 $\mu m^2$ that the offered RAM cell works accurately and correct output results are gained.

### 4.4 Comparisons

The offered D-latch cell improved the number of used cells and the occupation area compared to [40] explained in Table 5. The QCA designer is used to match the results betwixt the offered RAM cell structure and the prior designs as shown in Table 6. In the introduced RAM cell, the occupation area and the number of used cells are reduced compared to the state of the art in [21, 22, 24, 25]. Hence, the number of used gates can be a substantial criterion to decrease area consumption decomposition as explained in Table 6.

### 4.5 Power dissipation analysis

Hamiltonian matrix (H) is used to gauge the total power and energy of a QCA structure. The Hamiltonian uses Hartree–Fock approximation for an array of QCA cells,

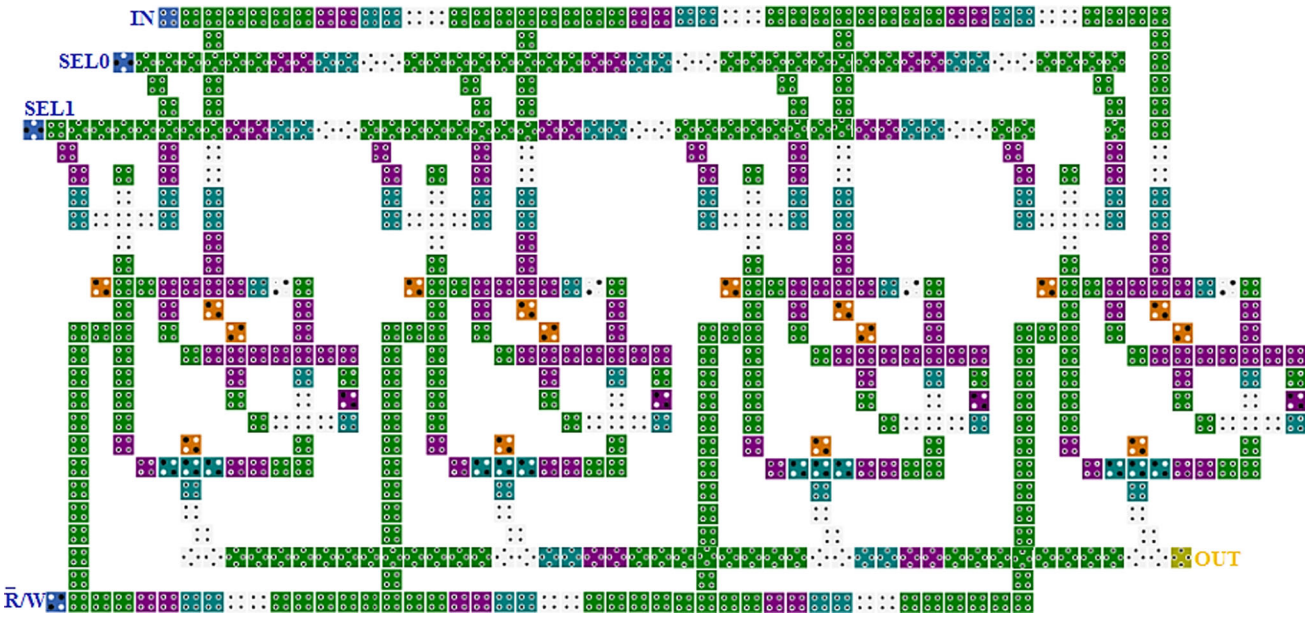


**Fig. 7** QCA layout of the proposed 4 × 1 RAM cell structure

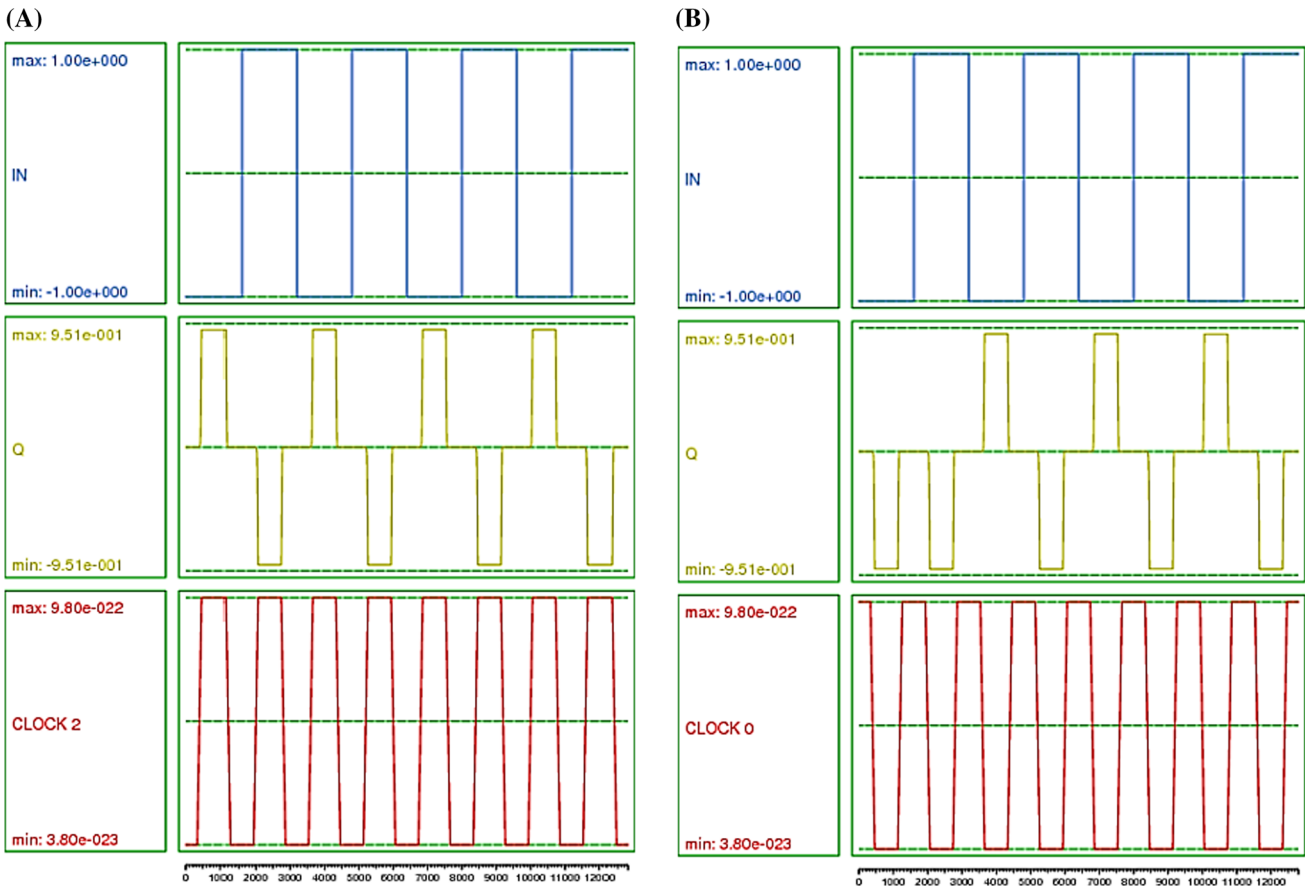


**Fig. 8** **a**. D-latch (cell response for Q = 1). **b**. D-latch (cell response for Q = 0)

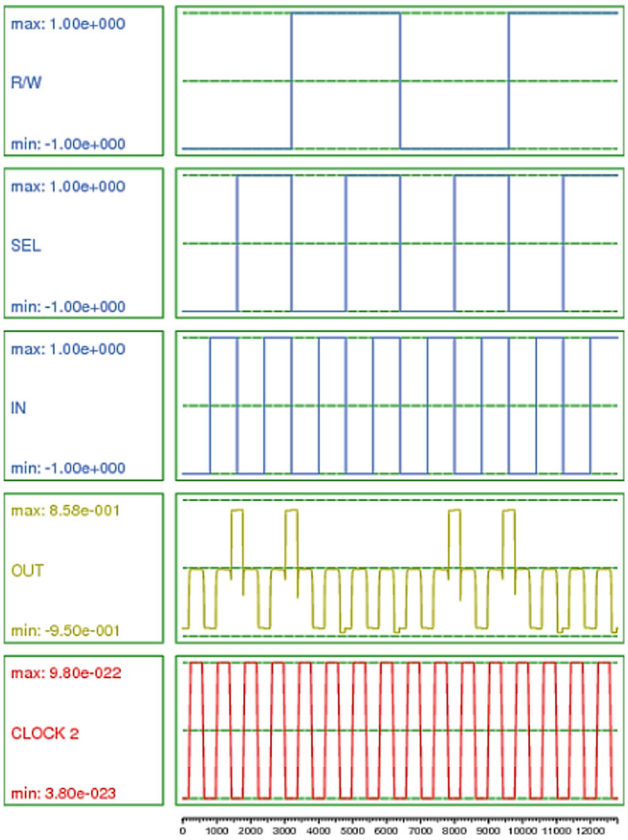


**Fig. 9** Proposed RAM cell


**Fig. 10** Proposed 4 × 1 RAM

and considering the Coulombic interaction between them [41–44]:

$$H = \begin{bmatrix} \frac{-E_k}{2}\sum_i C_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i C_i f_{i,j} \end{bmatrix} = \begin{bmatrix} \frac{-E_k}{2}\left(C_{j-1}+C_{j+1}\right) & -\gamma \\ -\gamma & \frac{E_k}{2}\left(C_{j-1}+C_{j+1}\right) \end{bmatrix} \quad (1)$$

where $C_i$ is the polarization of the $i$th and $f_{i,j}$ is the geometrical agent characterizing electrostatic interaction between cells ($i$ and $j$) due to the geometrical distance. In the case of equivalently spaced adjoining cells, agent $f_{i,j}$ is imbibing into the Kink energy description ($E_k$). This energy is pertained via the energy value of two QCA cells ($i$ and $j$) having inverse polarizations and can be evaluated as [45–47]:

$$E_{i,j} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_{i,n}q_{j,m}}{|r_{i,n}-r_{j,m}|} \quad (2)$$

where $\varepsilon_r$ is the dielectric constant, $q_{i,n}$ is the charge in $i$th point of cell $n$ and $r_{i,n}$ is the location of dot $i$ in cell $n$. The prognoses value of energy consumption of QCA structure at every clock cycle is appraised as [48]:

$$E = \langle H \rangle = \frac{h}{2}.\vec{\Gamma}.\vec{\lambda} \quad (3)$$

where $\vec{\Gamma}$ is the energy vector of the cell containing its neighbor's effects [$\vec{\Gamma}$ is evaluated by Eq. (4)], $h$ is reduced Planck constant and $\vec{\lambda}$ represents coherence vector.

$$\vec{\Gamma} = \frac{1}{h}\left[-2\gamma, 0, E_k\left(C_{j-1}+C_{j+1}\right)\right] \quad (4)$$

where $\left(C_{j-1}+C_{j+1}\right)$ is the sum of adjoining polarizations. As demonstrated in Fig. 11, the power stream of a QCA cell located in a binary wire is orderly within the four principal signal flows. As evidenced in [48], the horizontal signal powers are tantamount where $P_{\text{in}}$ is attained symptom power by the left neighboring cell and the released symptom power is obtained by the right neighboring cell $P_{\text{out}}$. As previously mentioned, in the switch phase, the inter-dot barriers that have arisen lead to transfer a significant amount of energy to the cell ($P_{\text{clock}}$) and in the release stage, these obstacles are declined; hence, the energy is comeback to the clocking

**Table 5** Comparison result of the proposed D-latch cell

| D-latch structure | Cell number | Occupation area ($\mu m^2$) | Gate count |
|---|---|---|---|
| Presented D-latch cell in [40] | 29 | 0.04 | 2 |
| Proposed D-latch cell | 24 | 0.02 | 2 |

**Table 6** Comparison result of offered RAM cell structures

| RAM structure | Coplanar wire crossing | Cell number | Occupation area ($\mu m^2$) | Gate count | Input to output delay(clocking cycle) |
|---|---|---|---|---|---|
| Presented RAM cell in [22] | Yes | 158 | 0.16 | 8 | 2 |
| Presented RAM cell in [21] | Yes | 100 | 0.11 | 8 | 3 |
| Presented RAM cell in [21] | No | 63 | 0.07 | 6 | 2 |
| Presented RAM cell in [24] | No | 109 | 0.13 | 8 | 1.75 |
| Presented RAM cell in [25] | No | 88 | 0.08 | 5 | 1.5 |
| Proposed RAM cell | Yes | 55 | 0.06 | 8 | 2.5 |

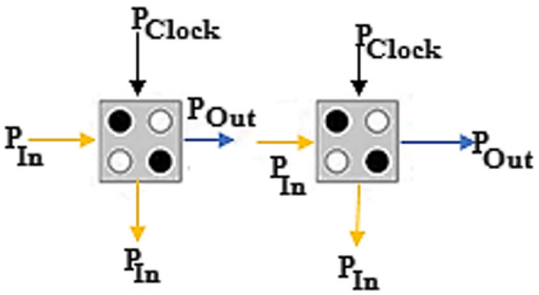


**Fig. 11** Power flows in a pair of neighbor cells [48]

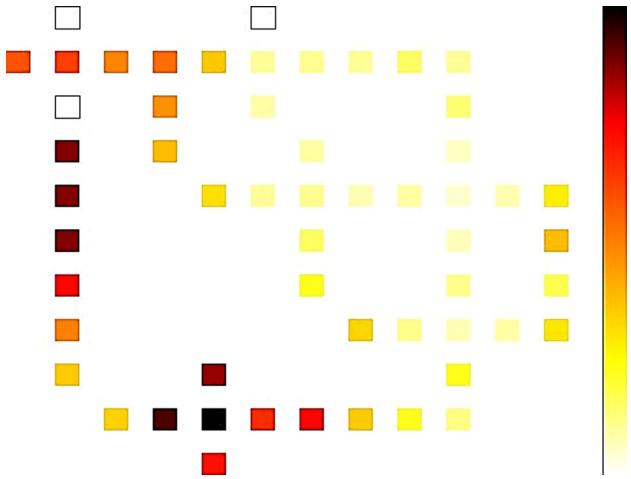

**Fig. 12** Power dissipation maps for the proposed RAM

circuit. The total power equation for a single QCA cell can be computed as [45, 46]:

$$P_1 = \frac{\mathrm{d}E}{\mathrm{d}t} = \frac{h}{2}\left[\frac{\mathrm{d}\vec{\Gamma}}{\mathrm{d}t}\cdot\vec{\lambda}\right] + \frac{h}{2}\left[\overrightarrow{r}\cdot\frac{\mathrm{d}\vec{r}}{\mathrm{d}t}\right] = P_1 + P_2 \tag{5}$$

In Eq. (5), $P_1$ contains two main sections: first, the power augment from input and output signal powers ($P_{\mathrm{in}} - P_{\mathrm{out}}$) and second, the transmitter clocking power of the cell ($P_{\mathrm{clock}}$) and $P_2$ symbolizes the dissipated power ($P_{\mathrm{diss}}$) [49]. According to [21], the energy dissipation is done via one clock cycle, $T_{cc} = [-T, T]$. The Hamiltonian and Coherence vectors are shown as:

$$E_{\mathrm{diss}} = \frac{h}{2}\int_{-T}^{T}\overrightarrow{r}\cdot\frac{\mathrm{d}\vec{r}}{\mathrm{d}t}\mathrm{d}t = \frac{h}{2}\left(\left[\vec{r}\vec{\lambda}\right]_{-T}^{T} - \int_{-T}^{T}\overrightarrow{\lambda}\cdot\frac{\mathrm{d}\vec{r}}{\mathrm{d}t}\mathrm{d}t\right) \tag{6}$$

It is notable that when the changing rate of $\vec{r}$ is maximum, the wasted energy is high. By expressing $r_+$ and $r_-$ as $\vec{r}(+T)$ and $\vec{r}(-T)$, the upper bound power dissipation model offered in [30, 46] is given as:

$$P_{\mathrm{diss}} = \frac{E_{\mathrm{diss}}}{T_{cc}} < \frac{h}{2T_{cc}}\vec{r}_+ * \left[\frac{\vec{r}_+}{|\vec{r}_+|}\tanh\left(\frac{h|\vec{r}_+|}{k_{\mathrm{B}}T}\right) + \frac{\vec{r}_-}{\vec{r}_-}\tanh\left(\frac{h|\vec{r}_-|}{k_{\mathrm{B}}T}\right)\right] \tag{7}$$

where $k_{\mathrm{B}}$ signifies the Boltzmann theorem and $T$ shows the temperature. In a presentation of QCA cells, the total dissipated power can be computed by surcharging the dissipated

**Table 7** Average energy consumption in diverse tunneling energy levels at $T = 2$ °K

| Power data | Avg leakage energy dissipation | Avg switching energy dissipation | Avg total energy dissipation |
|---|---|---|---|
| 0.50 $E_k$ | 0.01729 | 0.03059 | 0.04788 |
| 1.00 $E_k$ | 0.05110 | 0.02575 | 0.07685 |
| 1.50 $E_k$ | 0.09016 | 0.02158 | 0.11174 |

power of all cells since the offered layout for every QCA structure is similar.

### 4.6 Energy analysis

In this section, computing the wastage energy of the introduced layout is applying the QCAPro software [49]. The maximum, average and minimum power wastage in a QCA layout with no adiabatic switching is evaluated via this software [19]. Evaluation of the offered layout is done under three various tunneling energy levels (0.5 $E_k$, 1 $E_k$ and 1.5 $E_k$) at 2.0 °K temperature. The energy wastage of the offered layout by 0.5 $E_k$ is demonstrated in Fig. 12. High power wastage cells are demonstrated applying thermal hotspots and darker colors. Table 7 illustrates the total distributed energy divided into switching and leakage energies for the offered RAM structure.

## 5 Conclusion and future works

The reported layout based on a 2D grid of row addressing of memory layouts is proposed utilizing the level-sensitive D-latch. The layout of a simple Read/Write circuit is made possible by one-bit memory cells keeping only the single bit in the memory structure. The reported layouts have impressive structures in complexity, wastage area and cell count utilization. The input output delay of the proposed RAM are not optimized it is disadvantage of this manner. The simulations of the offered layouts of RAM cells are accomplished applying both bistable and coherence engines (by several operating temperatures) in QCADesigner, and computing the wasted energy of the offered layout is accomplished applying the QCAPro software. The logical structures are designed to be used as the basic building of nano-computers/general processors which cause to have technical advancement after the current researches. Therefore, the introduced layouts in addition to methods examined can help to improve energy consumption in future works.

Diminishing the usage gates in the offered memory, memory circuit layout based on magnetic QCA and fault-tolerant scheme of the memory circuits based on QCA can be discussed in the future works.

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