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An efficient XOR design based on NNI and five-input majority voter in quantum-dot cellular automata

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Abstract
As an emerging nanodevice, Quantum-dot cellular automata (QCA) is a hopeful candidate for conventional complementary metal oxide semiconductor devices. XOR, one of the most vital gates, occupies a significant positon in digital logic circuits. In order to improve the property performance of XOR, a novel five-input majority gate is put forward first. Then, an efficient XOR employing a NAND-NOR-Inverter (NNI) and the proposed five-input majority voter is realized in the paper. Compared with previous counterparts based on gates, the proposed design requires fewer cells, occupies less area, and consumes less average energy consumption. Specifically, it improves by 11.11% in cell count, 2.11% in area, and 9.51% ($1.5E_k$) in energy consumption when compared to the state-of-the-art design. The clock delay of the XOR in the article keeps the same with the minimum of them. Additionally, the proposed design has the lowest QCA cost, including area-delay cost, QCA-specific cost, and energy-delay cost. Moreover, the design is coplanar, without any crossing types. All these make it an outstanding design. To demonstrate its practicality, n-bit parity generators using the proposed XOR are implemented. The novel 4-bit parity generator excels in cell count, area, and average energy dissipation, achieving optimization of up to 10.6%, 6.0%, and 38.6% ($0.5E_k$), respectively, compared to previous optimum values. The significance of these optimization results becomes more pronounced as the bit of parity generators increases, indicating a promising future for constructing complex circuits.

Keywords QCA · NNI · Novel majority gate · XOR · Parity generator

1 Introduction

The feature size of traditional devices is scaling and the integration density is increasing with the rapid development of CMOS technologies, which leads to ever-growing problems, quantum effects, high leakage current and energy dissipation for instance (Sheikhfaal et al. 2015a). Searching for alternatives like novel nanodevices may be an efficient solution. Nanodevices include Carbon Nano Tube (CNT) (Bachtold et al. 2001), Single Electron Transistor (SET) (Kastner 1992), Tunneling-phase-logic (TPL) (Fahmy and Kiehl 1999),

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Quantum-dot Cellular Automaton (QCA) (Lent et al. 1993) and so on. Among them, QCA utilizing the Coulomb interaction between electrons doesn't have traditional transistors and possesses the characteristics of high switching rate (Seminario et al. 2004), high integration density (DeHon and Wilson 2004), low energy dissipation (Farazkish et al. 2008) etc., which makes it one of the most promising candidates (Henderson et al. 2004). In recent years, QCA has been intensively studied and achieves a rapid development.

XORs are considered as one of the important modules in digital circuit design since they are frequently used in full adders, parity generators, shifting registers, default detecting circuits etc. (Kumar et al. 2017). Thus, a XOR with high performance is of great importance in improving circuit efficiency. As a complicated gate, XOR can be constituted with elementary gates, majority gates, NOT and NNI gates for example. The proposed gate-based XORs are manifold and can be classified into five different constructions according to components: (1) using three three-input majority gates (M3) and NOT gates (Jagarlamudi et al. 2011; Shah et al. 2012; Roohi et al. 2011; Suresh and Ghosh 2014; Kianpour et al. 2014; Mohammadi et al. 2017; Khosroshahy et al. 2017; Chabi et al. 2014; Singh et al. 2016; Mustafa and Beigh 2013; De et al. 2016; Teja et al. 2008; Beigh et al. 2013); (2) consist of four three-input majority gates and NOT gates (Mustafa and Beigh 2013; Beigh et al. 2013; Poorhosseini and Hejazi 2018); (3) based on a three-input majority gate, a five-input majority gate (M5) and NOT gates (Chabi et al. 2014; Singh et al. 2016; Angizi et al. 2014; Sasamal et al. 2018; Sheikhfaal et al. 2015b; Mohammadi and Navi 2018); (4) realized using four NNIs (Poorhosseini and Hejazi 2018); (5) employing a five-input majority gate and NNI (Zhang et al. 2020). In the hard work of researchers to seek for more efficient circuits, the properties of XORs are obtained optimization continuously.

The main contributions of the work in the article are summarized as follows. (1) A novel five-input majority gate is proposed to construct an efficient XOR using the fifth structure mentioned above (a five-input majority gate and NNI); (2) Compared with the existing designs, XOR put forward in the paper shows superiority with respect to physical properties; (3)Also, n-bit parity generators implemented utilizing the state-of-the-art XOR describe a bright application prospect.

The paper proceeds as follows. Section 2 reviews the basics of QCA. In Sect. 3, previous XOR designs are categorized into five types according to the rule referred to in Sect. 1. The new scheme of XOR and one of its applications-parity generators are presented and discussed in Sect. 4. And Sect. 5 concludes the work.

2 QCA basics

The elementary unit of QCA is QCA cells. As shown in Fig. 1a, a standard cell comprises four quantum dots and two free electrons. The electrons can tunnel between these quantum dots and are liable to occupy the diagonal positions because of the Coulomb interaction.

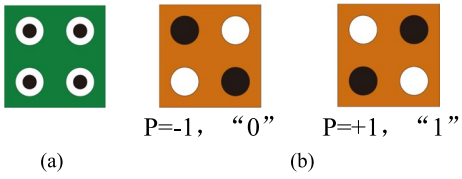


Fig. 1 QCA cell, **a** Standard QCA cell, **b** Polarized cells

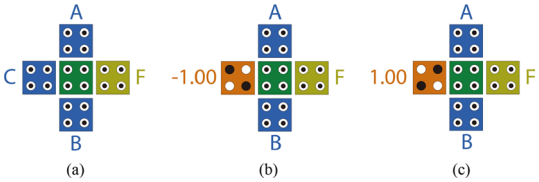


Fig. 2 Three-input majority voter, **a** QCA structure, **b** AND, **c** OR

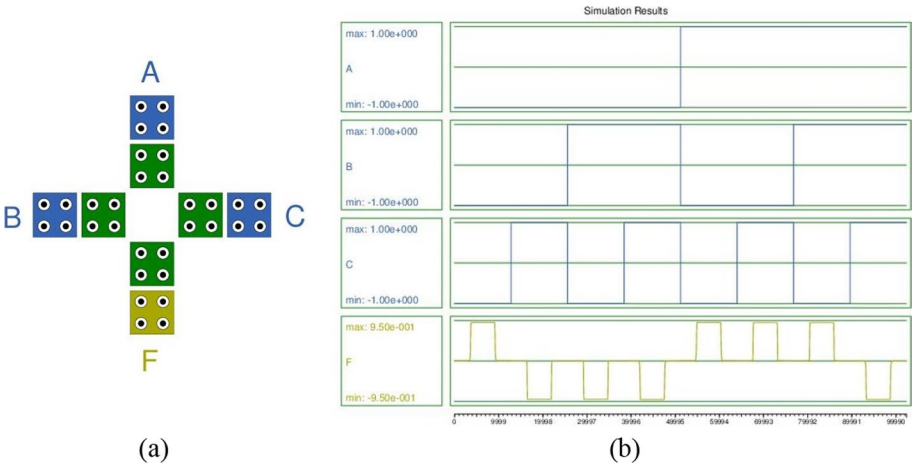


Fig. 3 NNI, **a** QCA structure, **b** Simulation results

Thus, the cell exists two steady states, namely polarization value $P = -1$ and $P = +1$, described in Fig. 1b, which is used to represent binary logic "0" and logic "1" respectively.

$$F = M(A, B, C) = AB + AC + BC \tag{1}$$

$$F = M(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \tag{2}$$

$$F = NNI(A, B, C) = A\overline{B} + A\overline{C} + \overline{BC} = M\left(A, \overline{B}, \overline{C}\right) \tag{3}$$

As the primary gates in QCA, the majority voter and NOT gate can be used to realize all the complicated circuits theoretically. The inputs of majority voters include three inputs and five inputs. Figure 2a is a three-input majority voter (M3), whose logic function is shown in Eq. (1). A AND logic will be achieved if fixing one of the three inputs to the polarity value $P = -1$, as presented in Fig. 2b. Similarly, if the fixed polarity value is replaced by $P = +1$, a OR function will be acquired, as illustrated in Fig. 2c. Equation (2) is the expression of the five-input majority gate (M5), and its QCA structures have numerous forms. NNI can also be regarded as an elementary gate, whose logic function is shown in Eq. (3) (Sen and Sikdar 2007). Figure 3a exhibits the QCA structure of NNI. The truth table of NNI is shown in Table 1, which is in accord with the simulation results shown in Fig. 3b using the simulation tool QCADesigner. The

Table 1 The truth table of NNI

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

bistable approximation simulation engine parameters of the tool is presented in Table 2. Based on these most basic gates above, any complicated circuits can be achieved in theory.

QCA clock is applied to control the direction of the information flow normally (Lent and Tougaw 1997). QCA clock employing the quasi-adiabatic switch clock scheme contains four phases, namely switch, hold, release and relax, as shown in Fig. 4. $\pi/2$ delay exists each of these adjacent phases. A complete clock cycle has four clock zones called clock 0, clock 1, clock 2 and clock 3. And the information transmits according to the direction of clock $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 0 \rightarrow 1 \rightarrow \cdots$. The QCA clock scheme guarantees that the data will be flow follow the scheduled path.

3 Classification of existing XORs

Existing XORs can be grouped into five types according to the components utilized, as presented in Table 3.

Table 2 Bistable approximation simulation engine parameters

Parameter	Value
Cell size	18.0 nm × 18.0 nm
Dot diameter	5.0 nm
Cell-to-cell spacing	2.0 nm
Number of samples	12,800
Convergence tolerance	0.001
Radius of effect	65 nm
Relative of permittivity	12.9
Clock high	9.8e−022 J
Clock low	3.8e−023 J
Clock shift	0.0e+000
Clock amplitude factor	2.0
Layer separation	11.5 nm
Maximum iterations per sample	100

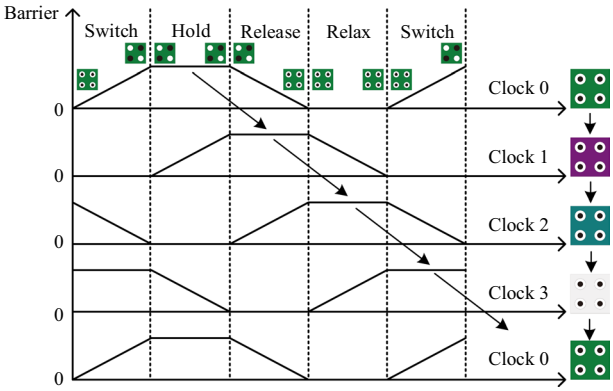


Fig. 4 QCA four-phase clock mechanism

4 New design schemes

4.1 Novel five-input majority voter

The novel XOR is designed using the fifth construction (a NNI and a five-input majority voter) in Table 3 with the logic function shown in Eq. (4). In order to achieve high-performance XOR, an excellent five-input majority voter is needed. Figure 5a exhibits the QCA structure of the five-input majority voter proposed in the paper. Since two inputs of the five-input majority voter are the same, as shown in Eq. (4), these two equal inputs are designed to share a common input called D. The other three inputs are A, B and C, and F is the output of the proposed five-input majority voter. Thus, the voter can gain the majority function among A, B, C, D and D, as is shown in Table 4. Figure 5b shows the simulation result of the proposed voter.

$$F = M5(A, B, 0, NNI(A, B, 1), NNI(A, B, 1)) \tag{4}$$

4.2 Novel XOR

A new XOR is designed based on the five-input majority voter proposed above and NNI, as shown in Fig. 6a. Figure 6b presents the simulation result, which demonstrates the correctness of the function. In order to illustrate the superiority of the design, XOR in the paper is compared with previous ones in terms of cell count, area, clock delay, cross structure and average energy dissipation, as shown in Tables 5, 6 and Figs. 7, 8, 9 and 10. Through the analysis of these figures, XOR in the article has the least cell count (24 cells), the least area (0.0186 μm^2), the least clock delay (0.75) and the least average energy dissipation. At the same time, the novel XOR design can easily be accessed with no crossover (Chaudhary et al. 2007). Figure 11 presents the power dissipation map for the proposed XOR gate at $0.5E_k$ tunneling energy level and 2.0 K temperature.

The cost of a QCA circuits is also an important parameter for performance analysis. Area-delay cost (ADC), QCA-specific cost (QSC) and Energy-delay cost (EDC) are calculated respectively according to the formulas presented in Khan and Arya (2022). The area delay cost can be obtained using (Area)×(latency)^2. The QCA-specific cost is $(MV^2+IN+CV^2)\times CK^2$, where MV, IN, CV and CK represent the number of utilized majority voters, inverters,

Table 3 Existing gated-based XORs

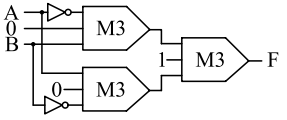
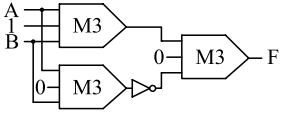
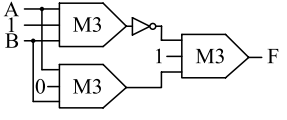
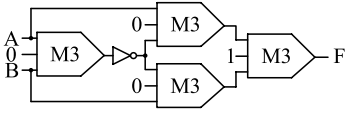
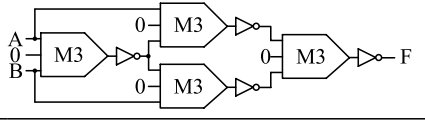
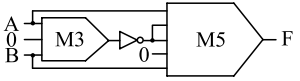
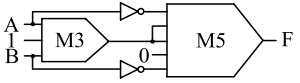
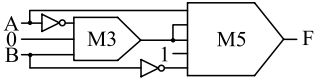
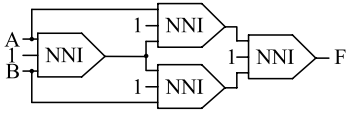
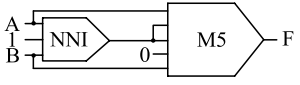
No	components	XOR schemes	XOR
1	three *M3s*	1–1 	1–1(1) Jagarlamudi et al. (2011),1–1(2)Shah et al. (2012), 1–1(3)Roohi et al. (2011), 1–1(4)Suresh and Ghosh (2014), 1–1(5)Kianpour et al. (2014), 1–1(6)(Mohammadi et al. 2017), 1–1(7)Khosroshahy et al. (2017), 1–1(8)Chabi et al. (2014), 1–1(9)Singh et al. (2016), 1–1(10) Mustafa and Beigh (2013), 1–1(11) De et al. (2016), 1–1(12) Chabi et al. (2014), 1–1(13) Teja et al. (2008)
		1–2 	1–2(1) Mustafa and Beigh (2013), 1–2(2)Beigh et al. (2013)
		1–3 	1–3 Singh et al. (2016)
2	four *M3s*	2–1 	2–1(1) Beigh et al. (2013), 2–1(2) Mustafa and Beigh (2013)
		2–2 	2–2(1) Mustafa and Beigh (2013), 2–2(2) Poorhosseini and Hejazi (2018)

Table 3 (continued)

No	components	XOR schemes	XOR
3	a *M3* and a *M5*	3–1 	3–1(1) Angizi et al. (2014), 3–1(2) Sasamal et al. (2018) 3–1(3) Sheikhfaal et al. (2015b), 3–1(4) Mohammadi and Navi (2018)
		3–2 	3–2 Singh et al. (2016)
		3–3 	3–3 Chabi et al. (2014)
4	four *NNIs*		4 Poorhosseini and Hejazi (2018)
5	a *NNI* and a *M5*		5 Zhang et al. (2020)

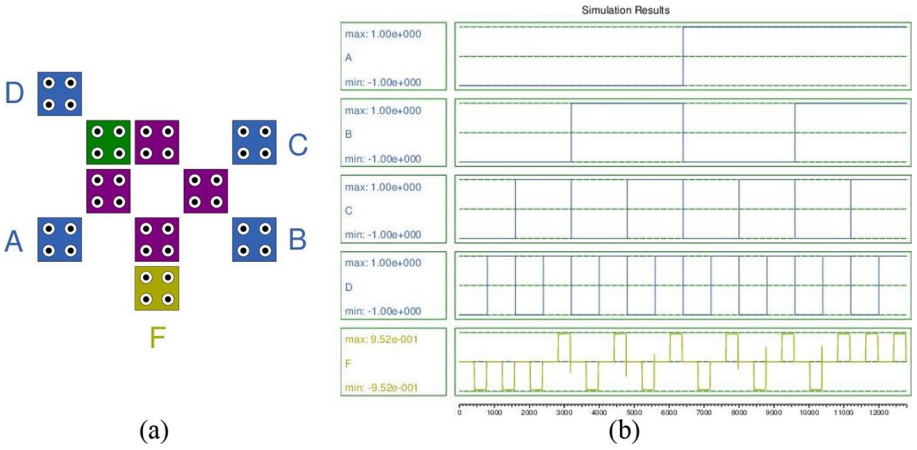


Fig. 5 The proposed five-input majority voter, **a** QCA structure, **b** Simulation results

Table 4 The truth table of the proposed five-input majority voter

A	B	C	D	E = D	F
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	1	1	1

crossovers and clocks, respectively. $E^2 \times D^2$ is used to calculate the energy-delay cost, where E is the dissipated energy and D is the latency. The cost calculation results of XORs are shown in Table 7 and the graphical view of comparisons are shown in Figs. 12, 13 and 14, respectively. Through these comparisons, Area-delay cost, QCA-specific cost and Energy-delay cost of the proposed XOR always keep the minimum.

All these comparisons certify that the proposed XOR possesses the excellent properties.

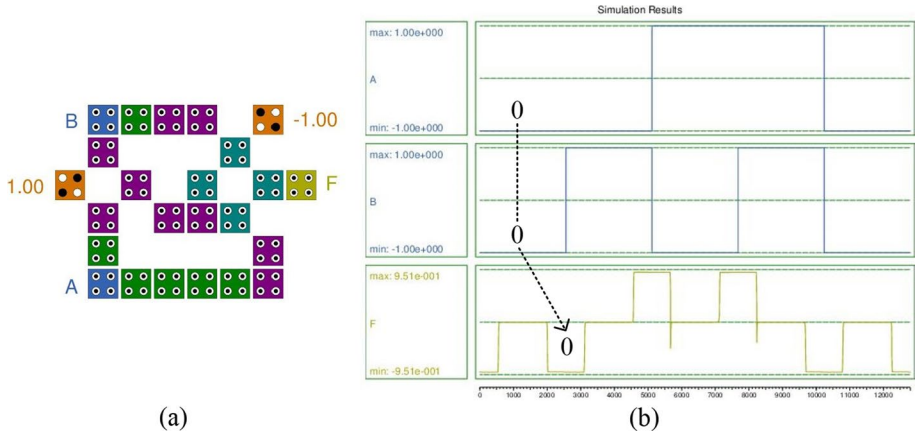


Fig. 6 The proposed XOR, **a** QCA structure, **b** Simulation results

4.3 Proposed parity generators

Utilizing the proposed XOR above, n-bit parity generators are implemented to illustrate the practicability. Figure 15a is the QCA circuit of 4-bit parity generator with 76 cells and 0.0820 μm^2. A 0.25 clock delay (clock 3) is added to the connection between adjacent XORs so as to hold the original clock design of the XOR, which provides convenience to construct high-bit parity generators. The simulation result of the proposed 4-bit parity generator is shown in Fig. 15b.

A comparison between the 4-bit parity generator in the paper and existing designs in cell count, area and average energy dissipation is needed to demonstrate the performance. Since the structure of the proposed circuit is coplanar with no rotated cells, the selected counterparts have the same characteristics, as shown in Fig. 16. The results can be seen from Table 8 and Figs. 17, 18 and 19. By contrasting the data, the novel 4-bit parity generator has the least values in term of cell count, area and average energy dissipation, up to 10.6%, 6.0% and 38.6% ($0.5E_k$) optimization compared to previous optimum values respectively. Therefore, the 4-bit parity generator based on XORs proposed in the paper has an excellent performance. Since the XOR is the elementary unit to construct the n-bit parity generators, the bit is higher, the optimization results are more significant. Figure 20 is the QCA design of the 32-bit parity generator.

5 Conclusion

XOR occupies a significant position in algorithmic logic. To improve the physical properties of XOR, an efficient five-input majority voter is designed. Based on the proposed five-input majority voter and NNI, a novel XOR is implemented. The proposed coplanar

Table 5 Performance figures of XORs

XOR	Cell count	Area um^2	Clock delay	Input/output accessibility	Type of crossover
1–1(1)	58	0.0614	0.75	No	No
1–1(2)	35	0.0281	1.00	No	No
1–1(3)	29	0.0317	1.00	No	No
1–1(4)	45	0.0388	0.75	No	No
1–1(5)	49	0.0606	1.00	Yes	Coplanar cross with rotated cells
1–1(6)	39	0.0313	0.75	Yes	Three-layer crossover
1–1(7)	55	0.0432	1.00	No	Coplanar cross with clock scheme
1–1(8)	59	0.0884	1.50	Yes	Coplanar cross with rotated cells
1–1(9)	32	0.0313	1.00	No	No
1–1(10)	83	0.0769	1.00	Yes	Three-layer crossover
1–1(11)	71	0.0769	1.00	Yes	Three-layer crossover
1–1(12)	54	0.0769	1.50	Yes	Coplanar cross with rotated cells
1–1(13)	121	0.1926	1.00	Yes	Coplanar cross with rotated cells
1–2(1)	41	0.0432	1.00	No	No
1–2(2)	54	0.0630	1.25	No	No
1–3	36	0.0352	0.75	No	No
2–1(1)	34	0.0313	1.25	Yes	No
2–1(2)	62	0.0693	1.50	Yes	No
2–2(1)	55	0.0737	2.00	Yes	No
2–2(2)	45	0.0519	1.00	Yes	No
3–1(1)	67	0.0606	1.25	Yes	Coplanar cross with clock scheme
3–1(2)	30	0.0210	0.75	Yes	No
3–1(3)	32	0.0246	1.00	Yes	No
3–1(4)	27	0.0218	0.75	Yes	No
3–2	28	0.0210	0.75	Yes	No
3–3	29	0.0281	0.75	Yes	No
4	38	0.0388	1.00	Yes	No
5	27	0.0190	0.75	Yes	No
P	24	0.0186	0.75	Yes	No

XOR has an excellent performance with less cell count, area, energy dissipation, and QCA cost. Moreover, the inputs and output of the design are easier to access without any crossovers since they locate on the outside of the structure. The 4-bit parity generator utilizing the novel XOR also presents outstanding physical property improvement in cell count, area and energy dissipation compared to its counterparts. Since the XOR is the elementary unit to construct the n-bit parity generators, the bit is higher, the optimization results will be more significant. Based on the proposed XOR and 5-input majority gate, high-efficiency full adders will be constructed in the future.

Table 6 Energy dissipation of XORs at 2.0 K

XOR	Average energy dissipation (meV)			Average Leakage energy dissipation (meV)			Average Switching energy dissipation (meV)		
	$0.50E_k$	$1.00E_k$	$1.50E_k$	$0.50E_k$	$1.00E_k$	$1.50E_k$	$0.50E_k$	$1.00E_k$	$1.50E_k$
1–1(1)	109.22	132.12	162.02	16.87	52.23	94.44	92.35	79.88	67.58
1–1(2)	57.85	72.65	91.32	11.10	33.01	58.16	46.75	39.64	33.16
1–1(3)	43.74	56.24	71.96	9.17	27.10	47.68	34.57	29.14	24.28
1–1(4)	75.54	94.57	118.82	13.60	41.27	73.76	61.94	53.30	45.06
1–1(5)	95.40	132.53	175.83	30.58	78.84	131.39	64.81	53.69	44.44
1–1(7)	97.23	120.18	149.53	16.33	49.90	89.64	80.90	70.28	59.88
1–1(8)	132.54	173.10	223.06	30.74	87.95	152.13	101.79	85.15	70.93
1–1(9)	49.81	63.49	80.83	9.73	29.77	52.78	40.08	33.73	28.05
1–1(12)	52.85	100.46	155.30	28.78	81.25	139.79	24.06	19.21	15.51
1–1(13)	273.85	359.64	462.41	72.39	193.60	324.76	201.47	166.04	137.65
1–2(1)	69.54	86.53	108.36	12.08	37.49	67.28	57.47	49.04	41.07
1–2(2)	97.11	118.51	146.79	14.72	47.84	87.41	82.39	70.67	59.38
1–3	63.32	78.53	97.47	11.35	33.48	58.93	51.97	45.04	38.54
2–1(1)	49.42	64.86	84.03	11.18	33.42	58.34	38.23	31.43	25.70
2–1(2)	100.15	127.21	161.69	18.61	57.56	103.05	81.54	69.65	58.64
2–2(1)	83.13	108.34	139.78	18.11	54.40	95.40	65.02	53.94	44.37
2–2(2)	63.30	84.98	111.26	15.98	46.19	79.59	47.32	38.80	31.68
3–1(1)	146.44	171.57	204.47	19.65	46.19	79.59	47.32	38.80	31.68
3–1(2)	37.77	52.63	70.29	11.86	32.33	54.20	25.92	20.30	16.09
3–1(3)	47.28	62.39	80.34	11.51	31.91	54.69	35.78	30.48	25.66
3–1(4)	34.06	47.65	63.44	10.37	28.30	47.64	23.69	19.35	15.80
3–2	36.43	50.47	66.73	11.03	28.79	48.32	25.40	21.68	18.40
3–3	49.89	62.23	77.34	9.94	27.30	47.17	39.96	34.93	30.16
4	46.99	66.54	89.51	14.82	40.32	68.10	32.17	26.23	21.41
5	30.92	44.78	61.01	10.10	27.92	47.34	20.82	16.86	13.67
P	29.33	41.24	55.21	9.64	25.71	42.82	19.69	15.53	12.39

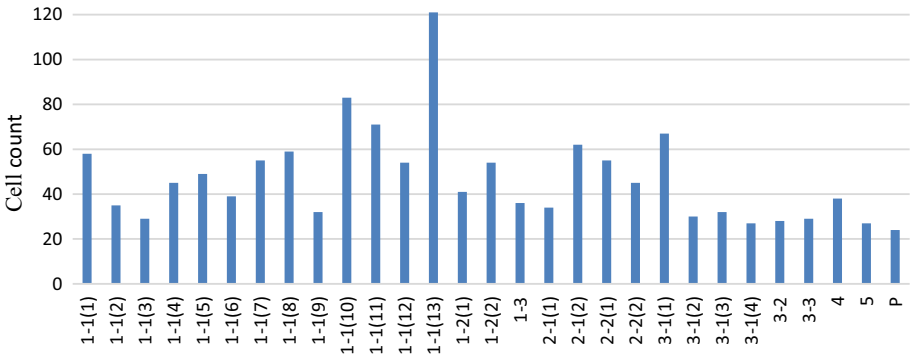


Fig. 7 Cell counts for XORs

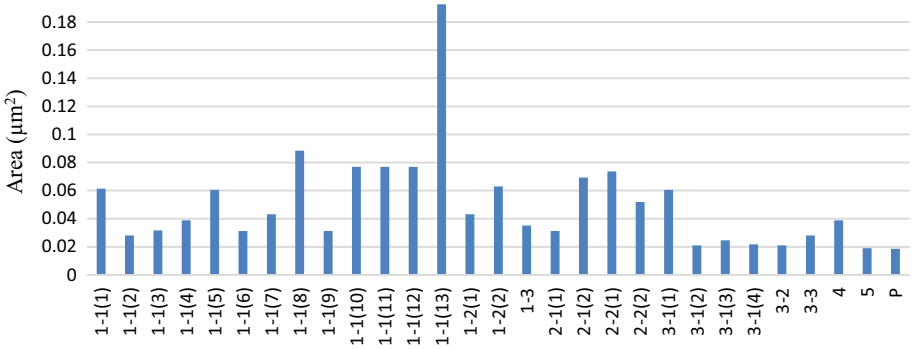


Fig. 8 Areas for XORs

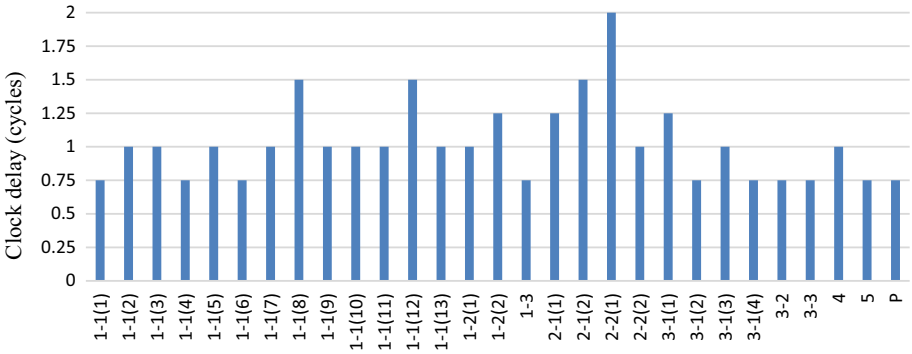


Fig. 9 Clock delay for XORs

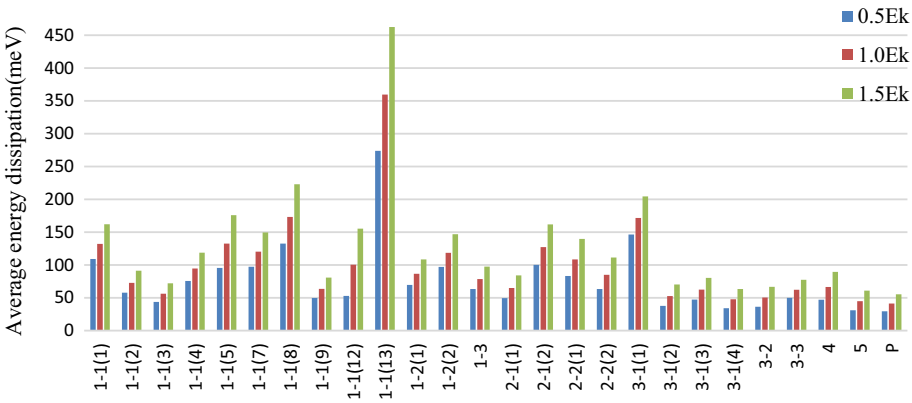


Fig. 10 Average energy dissipation for XORs

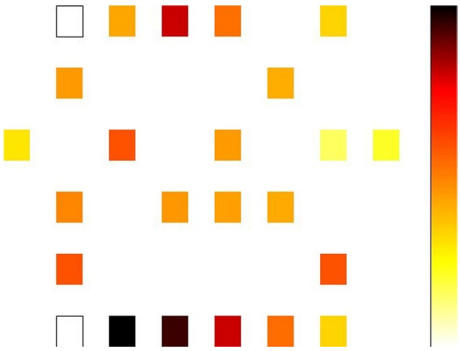


Fig. 11 Power dissipation map for the proposed XOR gate at $0.5E_k$ tunneling energy level and 2.0 K temperature

Table 7 The cost of XORs

XOR	ADC (m^2·cc)$\times 10^{12}$	QSC (scp)	EDC(seV-scc)$\times 10^3$		
			$0.5E_k$	$1.0E_k$	$1.5E_k$
1–1(1)	0.0345	99	11.930	17.456	26.251
1–1(2)	0.0281	176	3.348	5.279	8.340
1–1(3)	0.0317	176	1.914	3.164	5.179
1–1(4)	0.0218	99	5.707	8.944	14.119
1–1(5)	0.0606	240	9.102	17.565	30.917
1–1(6)	0.0176	108	–	–	–
1–1(7)	0.0432	192	9.455	14.444	22.360
1–1(8)	0.1989	432	17.569	29.966	49.758
1–1(9)	0.0313	176	2.482	4.032	6.534
1–1(10)	0.0769	240	–	–	–
1–1(11)	0.0769	192	–	–	–
1–1(12)	0.1730	432	2.795	10.094	24.120
1–1(13)	0.1926	240	74.995	129.342	213.824
1–2(1)	0.0432	160	4.837	7.488	11.743
1–2(2)	0.0984	250	9.432	14.046	21.549
1–3	0.0198	90	4.010	6.168	9.501
2–1(1)	0.0489	425	2.444	4.208	7.063
2–1(2)	0.1559	612	10.032	16.185	26.146
2–2(1)	0.2948	1280	6.915	11.742	19.542
2–2(2)	0.0519	320	4.008	7.223	12.380
3–1(1)	0.0947	150	21.446	29.438	41.810
3–1(2)	0.0118	45	1.427	2.770	4.941
3–1(3)	0.0246	80	2.236	3.894	6.456
3–1(4)	0.0123	45	1.161	2.271	4.025
3–2	0.0118	54	1.328	2.548	4.453
3–3	0.0158	54	2.490	3.873	5.982
4	0.0388	256	2.209	4.429	8.013
5	0.0107	36	0.957	2.006	3.723
P	0.0105	36	0.861	1.701	3.049

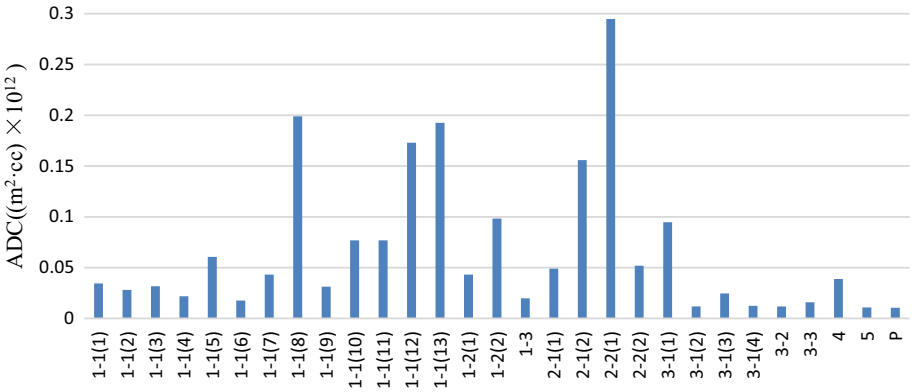


Fig. 12 Area-delay cost for XORs

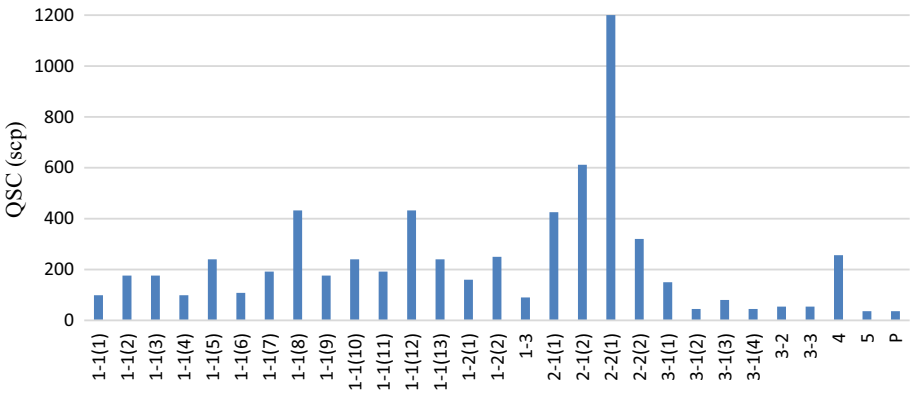


Fig. 13 QCA-specific cost for XORs

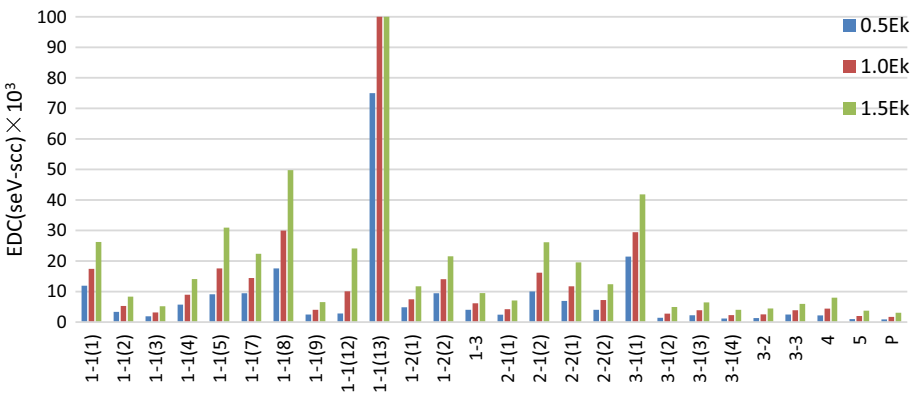


Fig. 14 Energy-delay cost for XORs

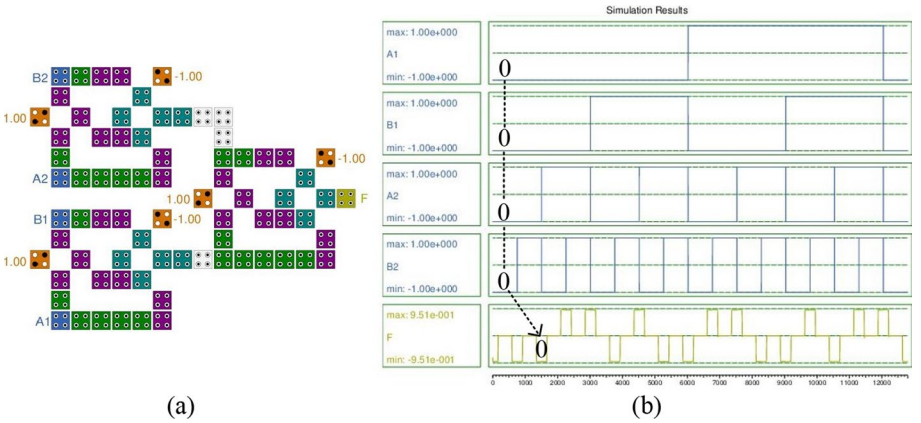


Fig. 15 The proposed 4-bit parity generator, **a** QCA structure, **b** Simulation results

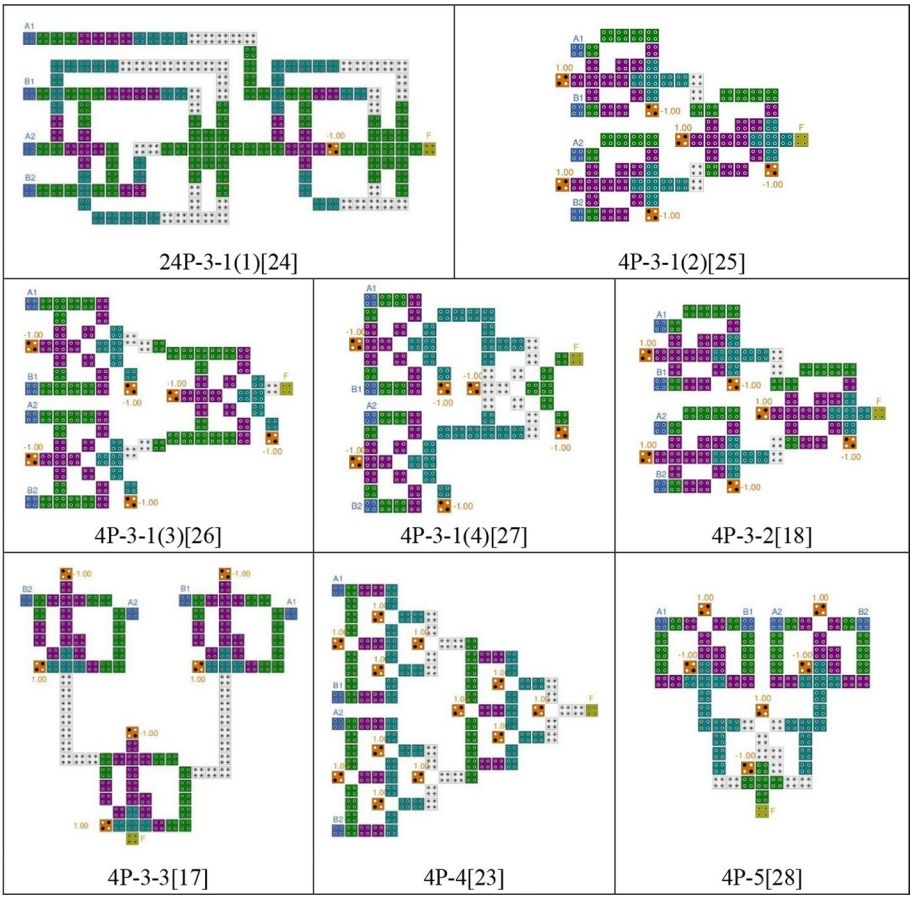


Fig. 16 Existing 4-bit parity generators

Table 8 Performance figures of 4-bit parity generators

4-bit parity generator	Cell count	Area μm^2	Average energy dissipation (meV)		
			0.50E_k	1.00E_k	1.50E_k
4P-3–1(1)	179	0.1662	348.44	420.56	513.82
4P-3–1(2)	97	0.0975	126.92	175.62	233.94
4P-3–1(3)	98	0.1126	140.28	189.45	246.96
4P-3–1(4)	85	0.0947	120.51	162.58	212.18
4P-3–2	87	0.0872	115.87	160.16	212.01
4P-3–3	111	0.1747	201.70	248.14	306.82
4P-4	112	0.1504	137.82	197.42	266.90
4P-5	86	0.0880	121.86	162.38	211.73
4P-P	76	0.0820	71.10	115.12	164.81

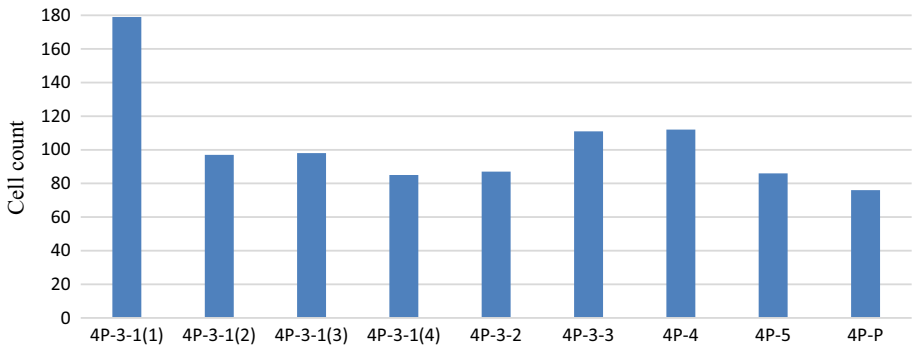


Fig. 17 Cell counts for 4-bit parity generators

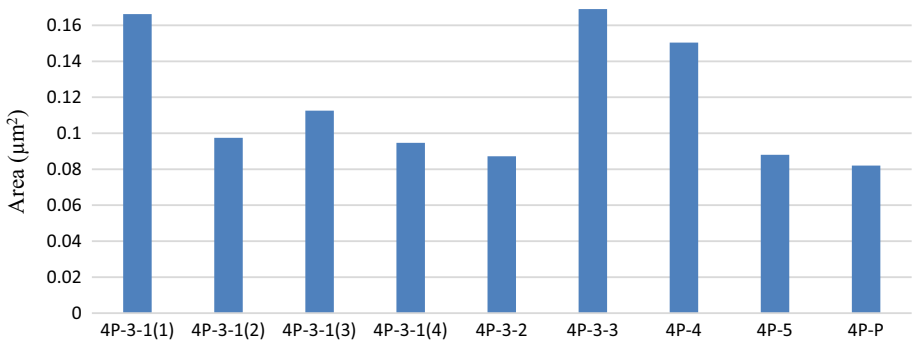


Fig. 18 Areas for 4-bit parity generators

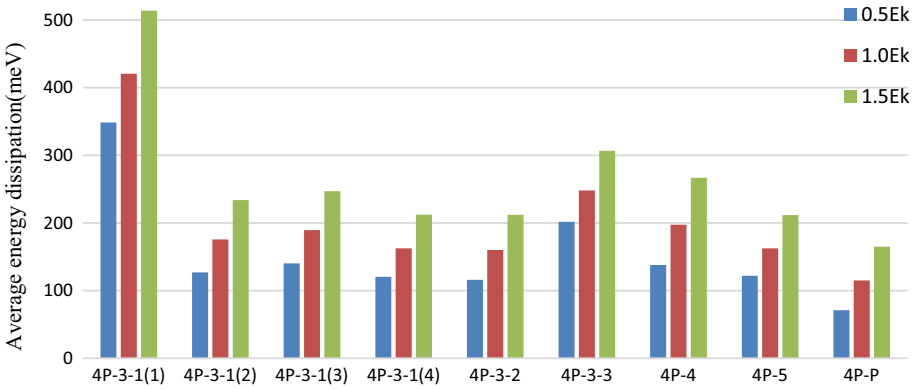


Fig. 19 Average energy dissipation for 4-bit parity generators

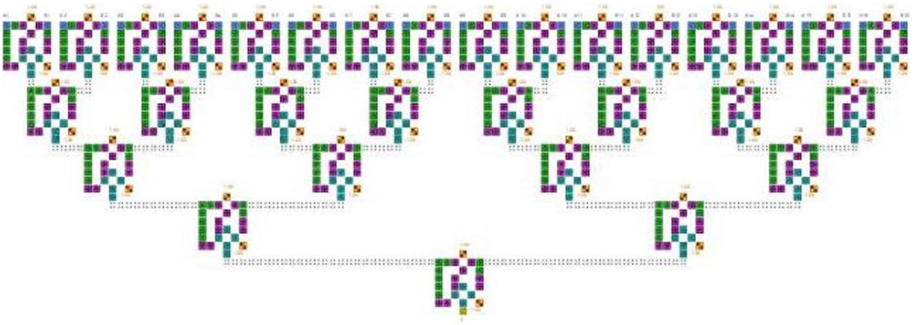


Fig. 20 The proposed 32-bit parity generator

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Declarations

Conflict of interest The author declares no conflict of interests.

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