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A full adder structure with a unique XNOR gate based on Coulomb interaction in QCA nanotechnology

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Abstract
Quantum-dot cellular automata (QCA) is a new and considerable technology for implementing nanoscale electronic circuits. QCA technology is considerable in terms of high speed, area and low power consumption compared to CMOS technology and can significantly improve the design of various logic circuits. The XOR/XNOR gate is one of the basic components in a full adder circuit, and improving its performance can lead to an improved full adder. To this end, the purpose of this paper is to provide a new and efficient design for the XNOR circuit based on QCA technology in order to realize the implementation of the new full adder structure. In order to evaluate the efficiency of designed structures, their operation has been studied by QCADesigner software. The simulation results show the superiority of the proposed full adder structure in terms of cell reduction about 5 %, 33 % in latency (clock zones) and 25 % in area reduction compared to the previous structure.

Keywords Quantum-dot cellular automata (QCA) · Full adder (FA) · Unique XNOR gate · Nanotechnology

1 Introduction

Quantum-dot Cellular Automata is a technology for presenting data and performing calculations based on the quantum property of charged particles and follows the principle of electrostatic interaction (Lent et al. 1993a). Increasing the density of circuits in QCA technology will be several times higher than conventional CMOS circuits, and the high switching speed and low power consumption have led to this technology being at the forefront of research (Salimzadeh and Heikalabad 2019; Heikalabad 2015). So far, many circuits have been designed based on QCA, and various implementations have been proposed in the construction of QCA cellular structures and their performance has been studied.

Full adder has been widely used as one of the basic components in computing circuits (Barughi and Heikalabad 2017; Ahmadpour et al. 2019; Heikalabad 2018; Shalamzari et al. 2020; Fouad and Radwan 2019; Mousavi et al. 2020; Mosleh 2019;

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Ahmadpour and Mosleh 2019; Babaie et al. 2019; Asadi et al. 2020). Designing an optimal full adder circuit will have a significant impact on computational circuits (Salimzadeh and Heikalabad 2019; Mohammadi and Mohammadi 2014). Therefore, in this paper, a new and efficient design for the three-input XNOR circuit is presented in order to realize the implementation of the optimal structure for the full adder circuit in QCA technology.

Other sections are organized as follows: An overview of the basic topics related to QCA and related work is presented in Sect. 2. In Sect. 3, a new structure for full adder is introduced by proposing a unique QCA-based XNOR gate. Section 4 simulates the presented structures and investigates their operations. Summarizing the results and proposing future work are described in Sect. 5.

2 Background and related work

In this section, we introduce the basic components and widely used gates in QCA. Next, we review XOR gate and full adder structures presented in previous work.

One of the important features that distinguish QCA from other technologies is the method of applying logic 0 and 1. QCA uses a quantum state of the cell to display these values. A binary QCA cell is a set of four dots where electrons can be stored. These dots are located side by side in a square-like structure. The QCA cell has two additional electrons, which can move freely between the dots. In QCA technology, cells are responsible for communicating and transmitting binary values between circuit components. In this technology, when a polarized cell is placed next to another cell in a line, the force between them causes the second cell to be in the same state as the first cell to minimize electrostatic energy in the cell configuration (Lent et al. 1993a; Lent et al. b; Norouzi et al. 2020; Mohammadi and Eshghi 2008; Norouzi and Heikalabad 2019; Heikalabad and Kamrani 2019; Salimzadeh et al. 2020).

There are two stable and possible arrangements in a cell, which are introduced as cell polarizations $P = -1$ and $P = +1$. The binary values "0" and "1" are mapped to polarizations -1 and $+1$, respectively (Lent et al. 1993a; Ahmadpour et al. 2020a; Sadoghifar and Heikalabad 2018; Teodósio and Sousa 2007).

Wire is one of the most important elements needed to design circuits in QCA technology. It can be easily made by placing cells in a linear arrangement (Hosseinzadeh et al. 2018; Karkaj and Heikalabad 2017a; Heikalabad and Gadim 2018; Heikalabad and Heikalabad 2021; Kamrani and Heikalabad 2020; Afrooz and Navimipour 2017; Fam and Navimipour 2019; Ahmadpour et al. 2021; Rad and Heikalabad 2017).

Like other technologies, the first widely used gate in QCA is the inverter gate. The function of this gate is easily obtained by diagonally placing a cell to the previous cell (Salimzadeh and Heikalabad 2019; Karkaj and Heikalabad 2017b; Heikalabad et al. 2016; Asfestani and Heikalabad 2017; Abbasizadeh and Mosleh 2020; Ahmadpour and Mosleh 2020; Rahmani et al. 2021).

The majority gate, as a widely used gate, has three inputs and one output. In this gate, the polarization of the output cell is determined by the status of the majority of inputs. Its logical function is as Eq. (1). Using the majority gate, AND and OR gates can be designed. If one of the inputs is fixed and its value is "-1" or "$+1$", the two-input AND gate or

OR gate is constructed, respectively (Salimzadeh end Heikalabad 2019; Ahmadpour et al. 2020b; Chaharlang et al. 2020; Heikalabad 2016; Raj et al. 2020; Majeed 2020).

$$\mathrm{Maj}(A, B, C) = AB + BC + AC \tag{1}$$

The full adder as the basic component in the design of computational circuits has attracted the attention of researchers, so that several different structures have been proposed for it (Salimzadeh and Heikalabad 2019; Barughi and Heikalabad 2017; Ahmadpour et al. 2018, 2019; Heikalabad 2018, 2020; Norouzi et al. 2020; Gadim and Navimipour 2018; Hasani et al. 2021).

Safoev and Jeon (2020) have proposed a new structure for the three-input XOR gate in the form of a unique QCA gate. They then used this XOR gate to design a single-bit full adder. The full adder is single-layer.

Ahmadpour et al. (2018) have proposed a new three-input XOR gate based on interactions among cells. They then used that to design a single-bit full adder. The full adder is single-layer.

3 Proposed structures

In this section, first a new structure for the three-input XNOR gate is presented as a unique gate in QCA, and then a new structure is presented using the proposed XNOR gate for the full adder.

3.1 QCA XNOR

The XNOR Gate is one of the most widely used gates in designing logical structures. The operation of the XNOR gate is to act as an even-count gate. This means that if the even number of inputs has a value of 1, the output is equal to 1. The logical function of three-input XNOR is as Eq. (2).

$$\mathrm{XNOR} = (A \oplus B \oplus C)' \tag{2}$$

In order to design this structure, a unique gate has been provided based on cellular interaction. Inputs A, B, and C enter the circuit simultaneously in the clock zone 0. Finally, in order to obtain the XNOR output, the output of this gate is created in the clock zone 1. The proposed cellular structure for XNOR, which can be seen in Fig. 1, has been implemented with 9 quantum cells. All the cells used in its design are 90° cell type. This structure is implemented as a single layer and the whole operation related to output production took 0.5 clock zones.

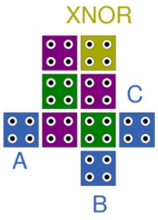

Fig. 1 Cellular design of proposed XNOR gate

Table 1 Truth table of a full adder

A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

3.2 QCA full adder

Full adder, as one of the basic components in computing, is an important structure in QCA. A full adder is a combination circuit that performs a three-bit arithmetic sum. The circuit has three inputs called A, B and C and two outputs called Sum and Carry.

Table 1 shows the truth table to design a new full adder with 3 inputs A, B and C and two outputs Sum and Carry. The input A is most significant bit of full adder, and the third input C is the carry obtained from the previous less valuable location. The Sum output achieves a lower value of the sum, and the Carry output represents the carry of the sum. The values of outputs are determined from the arithmetic sum of the input bits. When all input bits are 0, the output is 0. The Sum output becomes one when only one input is 1 or all three inputs are 1. Carry output is equal to 1 when two or three inputs are equal to 1. The logical function of a full adder is as Eq. (3).

$$\text{Sum} = \text{A} \oplus \text{B} \oplus \text{C} \tag{3}$$

$$\text{Carry} = \text{AB} + \text{BC} + \text{AC} = \text{MG}(\text{A}, \text{B}, \text{C})$$

Based on the logical function, a proposed unique XNOR gate and a majority gate were used to implement the full adder structure. Inputs A, B, and C enter the circuit simultaneously in clock zone 0. The inputs are applied simultaneously to the three-input XNOR gate and the three-input majority gate to obtain Sum and Carry outputs.

The inverse of the XNOR gate output, which is produced in clock zone 1, is the Sum output. The output of the majority gate, which is produced in clock zone 1, is the Carry output. The proposed cellular structure for full adder can be seen in Fig. 2.

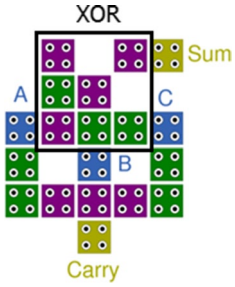

Fig. 2 Proposed design for full adder

Table 2 QCADesigner parameters (Walus et al. 2004)

Parameter value	Value
Cell size	18 nm *18 nm
Relaxation time	1.0e−015
Time step	1.0e−016
Radius of effect	80.0
Relative permittivity	12.90
Clock high	9.80e−022
Clock low	3.80e−023
Clock amplitude factor	2.0
Layer separation	11.5
Clock shift	0.0e+000
Total simulation time	7.000000e−011

Table 3 Implementation result for XNOR gates

Structure	Cell count	Area (μm^2)	Latency (clock cycle)
Safoev and Jeon (2020)	17	0.02	0.5
Ahmadpour et al. (2018)	10	0.008	0.5
Our design	9	0.006	0.5
Improvement	10 %	25 %	–

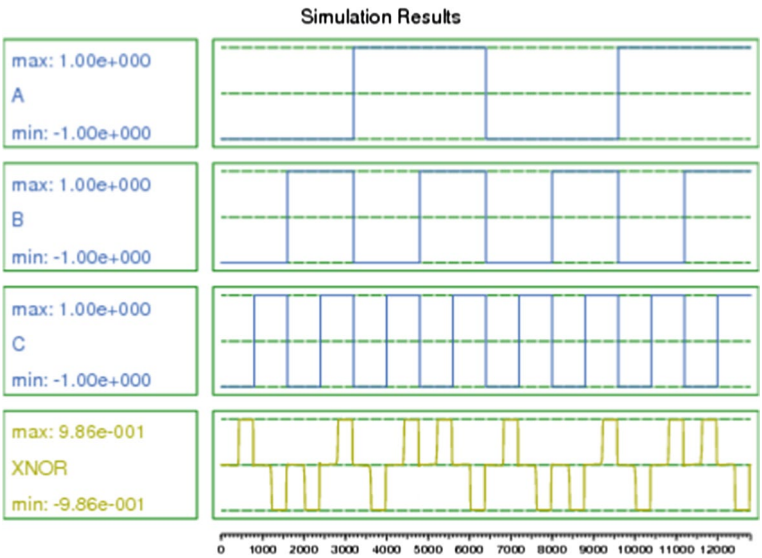

Fig. 3 Simulation result of the proposed XNOR gate

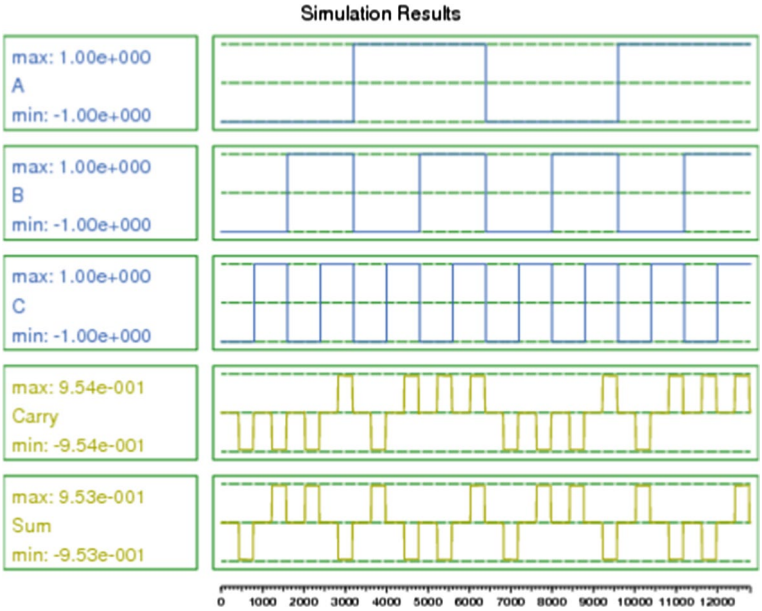

Fig. 4 Simulation result of the proposed full adder

Table 4 Implementation for Full adder gates

Structure	Cell count	Area (μm^2)	Latency (clock cycle)
Safoev and Jeon (2020)	49	0.05	1
Ahmadpour et al. (2018)	20	0.016	0.75
Our design	19	0.012	0.5
Improvement	5%	25%	33%

4 Simulation results and comparison

In this section, in order to evaluate the performance of the proposed structures, we investigate their operation based on parameters such as the amount of occupied area and the number of cells.

QCADesigner 2.0.3 software is used to simulate the proposed structures in QCA. The simulation is performed with Bistable Approximation engine. Table 2provides a brief description of the parameters used for simulation (Walus et al. 2004).

Figure 3 shows the result of the proposed structure for the three-input XNOR gate. According to the operation table, the XNOR output of the three inputs is 1 when the number of inputs with value 1 is even. This operation can be seen in Fig. 3 with a half-cycle delay.

The implementation result of the proposed structure for the XNOR gate compared to the previous XOR gates is given in Table 3. In order to evaluate the proposed structure, the

proposed design is compared with the previous structures in terms of the number of cells and occupied area. The proposed structure shows an improvement of about 10 % in terms of cell count and about 25 % in terms of occupied area compared to the previous best XOR gate.

Figure 4 shows the result of the proposed structure for full adder. The Sum and Carry outputs are obtained with a half-cycle delay in accordance with what is provided in the operation table.

In order to evaluate the improvement of the proposed structure for full adder in QCA compared to the previous design, the values of the parameters related to the implementation of the structures are presented in Table 4. As the values of the implementation results, the proposed structure shows an improvement of about 5 % in terms of the number of cells, about 25 % in terms of occupied area, and about 33 % in terms of latency compared to the previous design.

5 Conclusions

QCA introduces a new method of computing and transmitting information in nanoscale. This technology is suitable for designing computational circuits due to its high operational speed. As a basic computation component, full adder is widely used in computational combination circuits. The XOR/XNOR gate is one of the main building blocks of a full adder circuit whose performance improvement can lead to an improved full adder. To this end, in this paper, a new and efficient design for the XNOR gate based on QCA technology was presented in order to realize the implementation of the new full adder circuit structure. In order to evaluate the efficiency of designed structures, their performance has been studied by QCADesigner software. The obtained results prove the efficiency of the structures presented in this paper.

References

Abbasizadeh, A., Mosleh, M.: Ultradense 2-to-4 decoder in quantum-dot cellular automata technology based on MV32 gate. ETRI J. **42**(6), 912–921 (2020). https://doi.org/10.4218/etrij.2019-0068

Afrooz, S., Navimipour, N. J.: Memory designing using quantum-dot cellular automata: Systematic literature review classification and current trends. J. Circuit. Syst. Comput. *26*(12), 1730004 (2017). https://doi.org/10.1142/S0218126617300045

Ahmadpour, S.-S., Mosleh, M.: New designs of fault-tolerant adders in quantum-dot cellular automata. Nano Commu. Netw. **19**, 10–25 (2019). https://doi.org/10.1016/j.nancom.2018.11.001

Ahmadpour, S.-S., Mosleh, M.: A novel ultra-dense and low-power structure for fault-tolerant three-input majority gate in QCA technology. Concurr. Comput.: Prac. Exp. **32**(5) (2020). https://doi.org/10.1002/cpe.5548

Ahmadpour, S.-S., Mosleh, M., Heikalabad, S.R.: A revolution in nanostructure designs by proposing a novel QCA full-adder based on optimized 3-input XOR. Physica B **550**, 383–392 (2018)

Ahmadpour, S.S., Mosleh, M., Rasouli Heikalabad, S.: Robust QCA full-adders using an efficient fault-tolerant five-input majority gate. Int. J. Circuit Theory Appl. **47**(7), 1037–1056 (2019)

Ahmadpour, S.-S., Mosleh, M., Heikalabad, S.R.: The design and implementation of a robust single-layer qca alu using a novel fault-tolerant three-input majority gate. J. Supercomput. **76**, 1–31 (2020a)

Ahmadpour, S.-S., Mosleh, M., Heikalabad, S.R.: An efficient fault-tolerant arithmetic logic unit using a novel fault-tolerant 5-input majority gate in quantum-dot cellular automata. Comput. Electr. Eng. **82**, 106548 (2020b)

Ahmadpour, S. -S., Mosleh, M., Asadi, M. A..: The development of an efficient 2-to-4 decoder in quantum-dot cellular automata. Iranian J. Sci. Technol. Trans. Elect. Eng. **45**(2), 391–405 (2021). https://doi.org/10.1007/s40998-020-00375-9

Asadi, M.-A., Mosleh, M., Haghparast, M.: A novel reversible ternary coded decimal adder/subtractor. J. Ambient Intell. Hum. Comput. **12**, 1–19 (2020)

Asfestani, M.N., Heikalabad, S.R.: A novel multiplexer-based structure for random access memory cell in quantum-dot cellular automata. Physica B **521**, 162–167 (2017)

Babaie, S., Sadoghifar, A., Bahar, A. N.: Design of an efficient multilayer arithmetic logic unit in quantum-dot cellular automata (QCA). IEEE Trans. Circuits Syst. II: Express Briefs **66**(6), 963–967 (2019). https://doi.org/10.1109/TCSII.2018.2873797

Barughi, Y.Z., Heikalabad, S.R.: A three-layer full adder/subtractor structure in quantum-dot cellular automata. Int. J. Theor. Phys. **56**(9), 2848–2858 (2017)

Chaharlang, J., Mosleh, M., Rasouli-Heikalabad, S.: A novel quantum steganography-Steganalysis system for audio signals. Multim. Tools Appl. **79**, 1–27 (2020)

Fam, S. R., Navimipour, N. J.: Design of a loop-based random access memory based on the nanoscale quantum dot cellular automata. Photon. Netw. Comm. **37**(1), 120–130 (2019). https://doi.org/10.1007/s11107-018-0801-9

Fouad, A.H., Radwan, A.G.: Memristor-based quinary half adder. AEU-Int. J. Electron. Commun. **98**, 123–130 (2019)

Gadim, M.R., Navimipour, N.J.: A new three-level fault tolerance arithmetic and logic unit based on quantum dot cellular automata. Microsyst. Technol. **24**(2), 1295–1305 (2018)

Hasani, B., Navimipour, N.J.: A new design of a carry-save adder based on quantum-dot cellular automata. Iran. J. Sci. Technol. Trans. Electr. Eng. 1–7 (2021)

Heikalabad, S.R., et al.: Midpoint memory: a special memory structure for data-oriented models implementation. J. Circuits Syst. Comput. **24**(05), 1550063 (2015)

Heikalabad, S.R., et al.: Erratum:“ Midpoint Memory: A Special Memory Structure for Data-Oriented Models Implementation". J. Circuits Syst. Comput. **25**(02), 1692001 (2016)

Heikalabad, S.R.: Non-coplanar counter in quantum-dot cellular automata. Eur. Phys. J. Plus **136**(2), 1–16 (2021)

Heikalabad, S.R., Gadim, M.R.: Design of improved arithmetic logic unit in quantum-dot cellular automata. Int. J. Theor. Phys. **57**(6), 1733–1747 (2018)

Heikalabad, S.R., Kamrani, H.: Design and implementation of circuit-switched network based on nanoscale quantum-dot cellular automata. Photon Netw. Commun. **38**(3), 356–377 (2019)

Heikalabad, S.R., Asfestani, M.N., Hosseinzadeh, M.: A full adder structure without cross-wiring in quantum-dot cellular automata with energy dissipation analysis. J. Supercomput. **74**(5), 1994–2005 (2018)

Heikalabad, S.R., Navin, A.H., Hosseinzadeh, M.: Content addressable memory cell in quantum-dot cellular automata. Microelectron. Eng. **163**, 140–150 (2016)

Heikalabad, S.R., Salimzadeh, F., Barughi, Y.Z.: A unique three-layer full adder in quantum-dot cellular automata. Comput. Electr. Eng. **86**, 106735 (2020)

Hosseinzadeh, H., Heikalabad, S.R.: A novel fault tolerant majority gate in quantum-dot cellular automata to create a revolution in design of fault tolerant nanostructures, with physical verification. Microelectron. Eng. **192**, 52–60 (2018)

Kamrani, H., Heikalabad, S.R.: Design and implementation of multiplication algorithm in quantum-dot cellular automata with energy dissipation analysis. J. Supercomput. **77**, 1–27 (2020)

Karkaj, E.T., Heikalabad, S.R.: Binary to gray and gray to binary converter in quantum-dot cellular automata. Optik **130**, 981–989 (2017a)

Karkaj, E.T., Heikalabad, S.R.: A testable parity conservative gate in quantum-dot cellular automata. Superlatt. Microstruct. **101**, 625–632 (2017b)

Lent, C.S., et al.: Quantum cellular automata. Nanotechnology **4**(1), 49 (1993a)

Lent, C.S., Tougaw, P.D., Porod, W.: Bistable saturation in coupled quantum dots for quantum cellular automata. Appl. Phys. Lett. **62**(7), 714–716 (1993b)

Majeed, A.H., et al.: Full adder circuit design with novel lower complexity XOR gate in QCA technology. Trans. Electr. Electron. Mater. **21**, 1–10 (2020)

Mohammadi, M., Eshghi, M.: Heuristic methods to use don’t cares in automated design of reversible and quantum logic circuits. Quantum Inf. Process. **7**(4), 175–192 (2008)

Mohammadi, Z., Mohammadi, M.: Implementing a one-bit reversible full adder using quantum-dot cellular automata. Quantum Inf. Process. **13**(9), 2127–2147 (2014)

Mosleh, M.: A novel full adder/subtractor in quantum-dot cellular automata. Int. J. Theoret. Physics **58**(1), 221–246 (2019). https://doi.org/10.1007/s10773-018-3925-x

Mousavi, H.A., Keshavarzian, P., Molahosseini, A.S.: A novel fast and small XOR-base full-adder in quantum-dot cellular automata. Appl. Nanosci. **10**, 1–12 (2020)
Norouzi, A., Heikalabad, S.R.: Design of reversible parity generator and checker for the implementation of nano-communication systems in quantum-dot cellular automata. Photon Netw. Commun. **38**(2), 231–243 (2019)
Norouzi, M., Heikalabad, S.R., Salimzadeh, F.: A reversible ALU using HNG and Ferdkin gates in QCA nanotechnology. Int. J. Circuit Theory Appl. **48**, 1291–1303 (2020)
Rad, S.K., Heikalabad, S.R.: Reversible flip-flops in quantum-dot cellular automata. Int. J. Theor. Phys. **56**(9), 2990–3004 (2017)
Rahmani, Y., Heikalabad, S.R., Mosleh, M.: Efficient structures for fault-tolerant majority gate in quantum-dot cellular automata. Opt. Quant. Electron. **53**(1), 1–18 (2021)
Raj, M., Gopalakrishnan, L., Ko, S.-B.: Design and analysis of novel QCA full adder-subtractor. Int. J. Electron. Lett. 1–14 (2020)
Sadoghifar, A., Heikalabad, S.R.: A content-addressable memory structure using quantum cells in nanotechnology with energy dissipation analysis. Physica B **537**, 202–206 (2018)
Safoev, N., Jeon, J.-C.: A novel controllable inverter and adder/subtractor in quantum-dot cellular automata using cell interaction based XOR gate. Microelectron. Eng. **222**, 111197 (2020)
Salimzadeh, F., Heikalabad, S.R.: Design of a novel reversible structure for full adder/subtractor in quantum-dot cellular automata. Physica B **556**, 163–169 (2019)
Salimzadeh, F., Heikalabad, S.R., Gharehchopogh, F.S.: Design of a reversible structure for memory in quantum-dot cellular automata. Int. J. Circuit Theory Appl. **48**(12), 2257–2265 (2020)
Shalamzari, Z.D., Zarandi, A.D., Reshadinezhad, M.R.: Newly multiplexer-based quaternary half-adder and multiplier using CNTFETs. AEU-Int. J. Electron. Commun. **117**, 153128 (2020)
Teodósio, T., Sousa, L.: QCA-LG: a tool for the automatic layout generation of QCA combinational circuits. In: Norchip 2007. IEEE (2007)
Walus, K., et al.: QCADesigner: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans. Nanotechnol. **3**(1), 26–31 (2004)