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Investigation of electrical and dielectric properties of epitaxially grown Au/n-GaAs/p-Si/Al heterojunction

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Abstract
We aimed in our paper to construct of Au/n-GaAs/p-Si/Al structure as a Schottky barrier diode by liquid phase epitaxial growth, and study it's electrical and dielectrically properties by Current–Voltage (I–V) and capacitance–voltage (C–V) measurements. The novelty in this article is investigation of dielectric properties of Au/n-GaAs/p-Si/Al that researchers had not studied before, which encouraged us to study these properties. From investigation of dielectric parameters such as impedance, we can tune the values of real part of impedance (Z′) and imaginary (Z″). By the variation of temperature, we found that the values of Z′ and Z″ reached maximum value at 30 °C and were reduced with temperature increasing, Z″ takes positive and negative values depending on temperature. The Z′ and Z″ have been verified by of The Cole–Cole diagrams. Also, the dielectric parameters such as capacitance (C), conductance (G) and tan(δ) could be controlled by variation of voltage, temperature and frequency. Electric parameters such as Ideality factors (n), series resistance (R_s), shunt resistance (R_{sh}), barrier height (Φ_b), rectification ratio (RR) were investigated from I–V measurement. To prove the diode behavior of Au/n-GaAs/p-Si/Al architecture, the electrical parameters using thermionic emission theory. The ideality alongside barrier height decrease with the rise of temperature and the device show intermediate rectifying ratio. Investigation of conduction mechanism asserts that space-charge-limited current prevailing in the forward bias, where schottky and pool frenkel control the transport in the reverse bias. Besides, trapping concentration factor and level were estimated in terms of Mott–Gurney law.

Keywords Epitaxial growth · Heterojunction · XRD · Dielectrics · I–V

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1 Introduction

Gallium arsenide (GaAs) is one of the beneficial semiconductors that meet the interest of many researchers on the account of their feasibility to involve in plenty of applications that finally integrated into industry (Arpapay et al. 2020; Saha et al. 2020). Yet, GaAs based-devices with metal semiconductor or metal insulator-semiconductor used in several application including field effect transistors, Schottky barrier diodes, and heterostructure bipolar transistors (Sze and Ng 2006; Ghosh et al. 1984; Ng and Card 1980; Hackam and Harrop 1972; Ashok et al. 1979; Altındal et al. 2006; Singh et al. 1990). Particularly, Gallium arsenide found special interest in application relaying on interface defect density (N_{ss}), series resistance (R_s), applied bias voltage and temperature (Chattopadhyay and Daw 1986; Card and Rhoderick 1971; Nielsen 1983; Hattori and Torii 1991; Biber 2003; Akkal et al. 2000; Akkal et al. 1999; Cova and Singh 1990; Mönch 1999; Chand and Kumar 1996; Chand and Kumar 1997).

It is recognized from theoretical work thermionic emission (TE) theory that the barrier height of GaAs (Φ_b) is unrelated to temperature. However, lately it has been found that it highly relied on temperature (Ghosh et al. 1984; Hackam and Harrop 1972; Ashok et al. 1979). In addition, the inhomogeneity of the barrier height (BH) has been suggested as a description for nonlinearity (Karataş et al. 2003; Özden et al. 2016). This feature qualifies GaAs to incorporate in various types of diodes (Karataş et al. 2005; Tung 1992; Song et al. 1986; Werner and Güttler 1991). The detailed review of the literature demonstrated contradictory results about the temperature dependence of both ideality factor (n) and barrier height (Φ_b) in GaAs diodes (Sze and Ng 2006; Ghosh et al. 1984; Ng and Card 1980). For example, Padovani (1968) found that ideality factors values (n's) of diode based on GaAs reduces with increasing which disagree with the theoretical predication finally asserted that barrier height must reduce linearly with temperature. Hackam and Harrop (1972) suggested ideality factor (n) must connected to the reverse current (I_0) which also conflict with theoretical outcomes. The proposed data of Harrop et. al make the values of barrier height obtained from both I–V and C–V are highly harmonious. On the other hand, Hudait et al. (2001) and Bengi and Bülbül (2013) elucidated that barrier height (Φ_b) exhibits abnormal rise, while ideality factors (n's) decrease at lower temperature for schottky barrier diode employed GaAs as n-type layer. Such unusual trend at low temperature on account of the existence of inhomogeneity of barrier height at the metal-semiconductor interface (M/S), which interpreted by gaussian distribution of barrier height (GD of BH).

In this article, we interested in the manufacture of Au/n-GaAs/p-Si/Al as a schottky barrier diode by liquid phase epitaxial growth and study it's electrical and dielectrically properties by I–V and C–V measurement. The novelty of this article is to study the dielectric properties of Au/n-GaAs/p-Si/Al that researchers had not studied before, which encouraged us to study these properties. From investigation of dielectric parameters such as Z' and Z'', we can tune these parameters by variation of temperature. Likewise, we can tailor the dielectric parameters such as C, G and tan (δ) by variation of voltage, temperature and frequency. For the first time, the conduction mechanism in both forward and reverse bias has been examined extensively and rapping concentration and trapping level was computed on the basis of Mott–Gurney law. Finally, transport mechanism in reverse direction were analyzed and Schottky and Poole–Frenkel (PF) field-lowering coefficients were studied as a function of temperature.

2 Experimental procedures

2.1 Synthesis

GaAs thin films were manufactured using liquid phase epitaxy (LPE) method (Farag et al. 2004). The LPE growth was carried out by the supercooling method. GaAs was fabricated on p-Si wafer of 300 μm thickness, and 20 Ω cm resistivity. Silicon wafer cleaned by standard method for removing all oxide layers and all contamination. Indium metal and monocrystalline n-GaAs of high purity were used as source materials. Next, the slipping boat in which the source materials and the Si substrate were charged, was heated up to the temperature with the pre-baking procedure of In, the growing dissolve was transported into connection with the substrate at 845 °C for 20 min. The LPE system was cool fast at a cooling rate of 0.7 °C/min to evade thermal harm. Purified Ar gas was flow through at 100 cm^3/min during the LPE growing period. The upper (Au) and lower electrode (Al) were deposited by thermal evaporation (Edward 306A). Schematic illustrated of Au/n-GaAs/p-Si/Al heterojunction is visualized in Fig. 1.

2.2 Characterization

X-ray scan of GaAs/Si were achieved by X-ray diffractometer equipped with filtered CuK_α a radiation (1.540 Å). Dielectric measurements were done in frequency range 0.1 Hz–20 MHz and at a temperature range from 30 to 150 °C using a Novocontrol high resolution alpha analyzer. It was reinforced by Quatro temperature controller via clean nitrogen as heating agent and pledging temperature steadiness best than 0.2 K.

3 Results and discussion

3.1 XRD investigation

The X-ray profile of GaAs synthesized by liquid phase epitaxy (LPE) on silicon substrate (Si) is demonstrated in Fig. 2a. As can be seen, the presence of well-defined peaks disclosed the highly crystalline GaAs phase. Except for the Diffraction lines of silicon substrate Si (400), all other reflection positions (2θ) and almost relative intensities are in accord with standard JCPDS# 79-0614, which are indexed and labelled as referred in the figure. Also, there is no lines for impurities or extra phases are noticed asserting

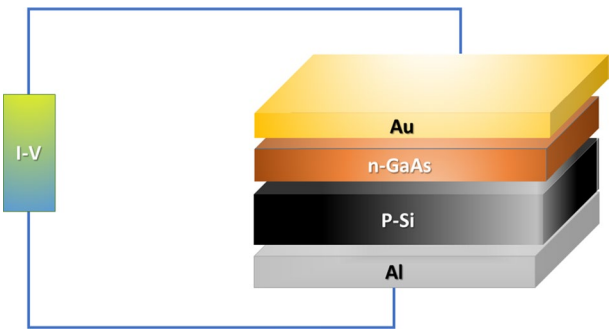

Fig. 1 Schematic diagram of Au/GaAs/n-Si/Al architecture

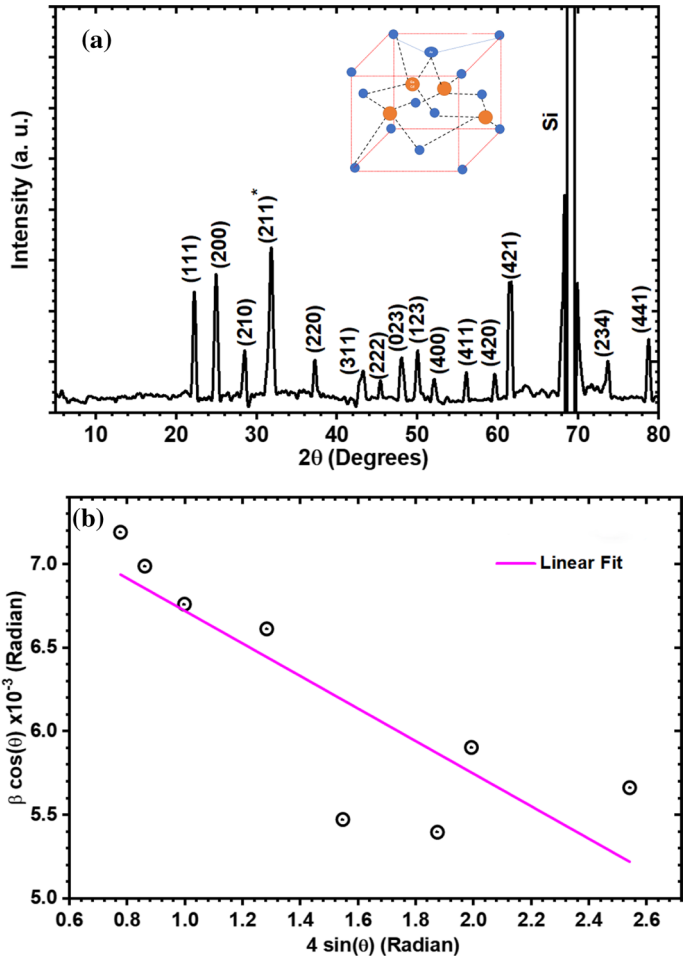

Fig. 2 **a** X-ray diffraction pattern of Au/GaAs/n-Si/Al and **b** Williamson–Hall plot of GaAs deposited on p-Si

the purity and prepared GaAs films. considering this consistence with standard file, the thin films are formed in cubic structure and space group Pa3(205). It is apparent that the GaAs films exhibits a preferred orientation along the diffraction line (211), marked with asterisks on figure, which also agree with standard file.

The lattice constant (a) studied film were estimated in terms miller indices (hkl) by the following equation (El Radaf et al. 2018):

$$d_{hkl} = \frac{a}{\sqrt[2]{h^2 + k^2 + l^2}} \tag{1}$$

It has been found that the value of length of cubic cell is 6.90 which differ slightly than the standard JCPDS (6.922) which may be assigned to internal stress due to the preparational high temperature.

For the purpose of confirmation, the grain size (D) is determined by both Williamson-Hall and Sherrer's method according to the following equations (Mansour et al. 2018; Hameed et al. 2020a):

$$\beta \cos\theta = k\lambda/D + 4\varepsilon \sin\theta \tag{2}$$

$$\mathrm{D} = 0.94\ \lambda/\beta \cos\theta \tag{3}$$

where λ (1.540 Å) referee to wavelength of X-ray, β donates to the full width at half maximum of the peak (in radian) and θ is diffraction angle at the reflection line. Figure 2b illustrates Williamson–Hall plots GaAs films. The data points were fitted to straight line and the slope and intercept used for calculating the grain size and microstrain. It has been found that the grain size determined by Williamson-Hall and Sherrer's method are 30 and 32 nm whereas the microstrain are 2.3×10^{-3}. The Dislocations and the number of crystallites (N) were calculated (Hameed et al. 2020b) and equal to 3.8×10^{11} line/cm^3 and 2.4×10^{14} cm^3, respectively.

3.2 Dielectric properties of Au/n-GaAs/p-Si/Al

As revealed in Fig. 3(a), each capacitance–voltage(C–V) curve of Au/n-GaAs/p-Si/Al has three regions; inversion, depletion and accumulation. DC bias has a significant effect on the accumulation region and a lesser one on the inversion and saturation regions due to the effect of dc bias on the interface states. The capacitance rises with reduction in

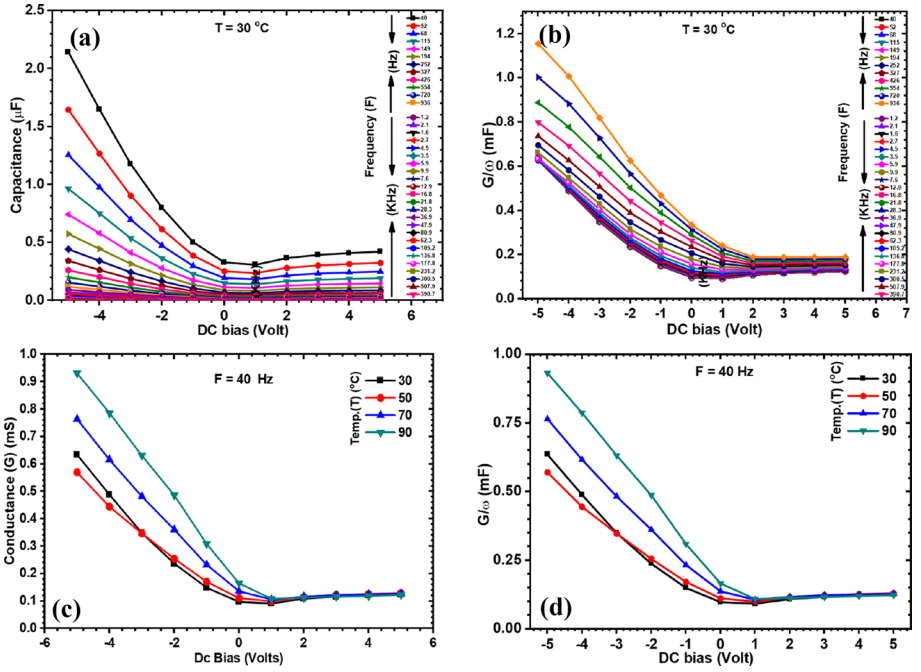

Fig. 3 **a** Capacitance (C) versus voltage (V) at different frequencies and T = 30 °C, **b** conductance versus voltage at different frequencies at T = 30 °C, **c** capacitance versus V at different temperatures and f = 40 Hz, **d** conductance versus voltage (V) at different temperatures and f = 40 Hz of Au/Ga As/n-Si/Al

frequency and it is worth mentioning that the capacitance originates from an irregularity layer between the GaAs/Si interface. It is the interface layer, where the metals meet semiconductor. This is irregular due to itching with HF and the high temperature used to make the device using LPE, which causing liquid metals to make nano dendrites like filaments within the oxide, if present, or semiconductor in the manufactured device. This happens at lower frequencies, where the interface states can track the ac signal and produce an extra capacitance, which depends on frequency. In the high frequency region, the interface states cannot track the ac signal. This weakens the influence of interface state capacitance to the entire capacitance negligibly small (Akkal et al. 2000). As revealed in Fig. 3(a and b), capacitance and conductance are sensitive to frequency. After the overhead discussion, it can be decided that under bias (V), the interface states are responsible for the detected frequency spreading in C(V) and G/ω (V) curvatures. Reliant on the relaxation time of the interface states and the frequency of the ac signal, capacitance here may be a due to interface states and depletion layer. Figure 3(c, d) display the measured capacitance and G/ω features of the Au/n-GaAs/p-Si/Al assembly as a function of forward and reverse voltage inside the temperature range of 30–90, respectively. As revealed in Fig. 3(c and d), the capacitance-voltage and conductance-voltage plots depend on temperature. The C–V features were measured in − 5 to 5 V range at assigned temperatures, in Fig. 3(d), there is a slight increase in G/ω in the reverse bias from 0.0 to 5 V. Meanwhile, the charge neutrality situations at the interface state must be fulfilled, narrowing of the depletion width in the forward bias. The acceptance–voltage C–V characteristic is a consequence from the increase of the ionized donor concentration (Özden et al. 2016). The capacitance (C) values increase with increasing temperature at a bias voltage (0.0 to − 6 V). This outcome can be credited to the fact that the interface states peruse the AC signal at little frequencies and consequently an extra capacitance happens in adding to the space charges capacitance as of the influence of interface charges (Karabulut et al. 2017; Yakuphanoglu et al. 2012; Zhang et al. 2017; Karataş and Türüt 2004; Mohammad et al. 2001). Also, as revealed in Fig. 3(c and d) the G/ω features of Au/n-GaAs/p-Si/Al assembly raised with temperature rely on the voltage in the forward bias, while the values of capacitance and G/ω remain almost constant with temperature in the reverse bias. Such a manner is ascribed to rearrangement of the series resistance and interface state densities. Moreover, this exact G/ω manner might be credited to a specific delivery of the interface states between GaAs/Si layers (Tataroğlu 2006; Chattopadhyay and RayChaudhuri 1993; Karataş and Kara 2011). Therefore, it can be thought that the C and G/ω plots relay on voltage and temperature. A conduct of C and G/ω is mainly ascribed to specific spreading of surface states at the n-GaAs/p-Si interface. The variations of C and G/ω characteristics with temperature at high frequency at which merely the free carriers in the common bands were capable of responding to the small excitation ac signal, shown in Fig. 3c and d for Au/n-GaAs/p-Si structures, respectively (Karataş and Kara 2011). Furthermore, as displayed in Fig. 3c and d, the values of both capacitance and G/ω increase with temperature.

Figure 4(a-b) display the difference of the C and G of the Au/n-GaAs/p-Si/Al assemblies as functions of frequency in the voltage range of − 5 to 5 V with steps of 1-V and temperature range of (30–90 °C). The frequency dependency of R_s can be obtained from the C–V–f and G–V–f data. The capacitance versus frequency at different voltage bias (V = − 5 to 5 V) at (T = 30 °C) respectively, were shown in Fig. 4(c–d). The capacitance (C) values do not change at high and mid frequency, but at low frequency dispersed and increase with temperatures and negative voltages from 0 to − 5 V as displayed in plot 4(a and d). The conductance (G) values in Fig. 4(b and c) raise with temperature and negative voltages (1–5 V) and its raise was small in low and mid frequency, but a rapid raise occurs in high

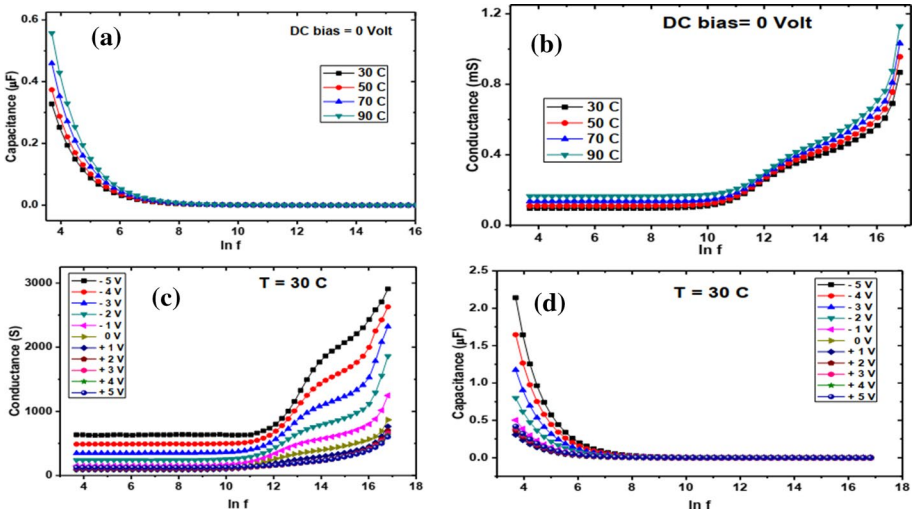

Fig. 4 **a** Capacitance versus ln(f) at different temperatures and V = 0 V, **b** conductance versus ln(f) at different temperatures and V = 0 V, **c** conductance versus ln(f) at different voltages and T = 30 C, **d** capacitance versus ln(f) at different voltages and T = 30 °C of Au/GaAs/n-Si/Al heterojunction

frequency region. The capacitance tends in high frequencies to approach its minimum values; meanwhile carrier transfer procedure is freezing at the higher frequencies (Perera et al. 1999) (Figs. 4, 5 and 6).

Figure 5(a) demonstrate the variation of impedance Z′ with frequency at different temperature. The values of Z′ reduce with temperature and raise with reducing voltage

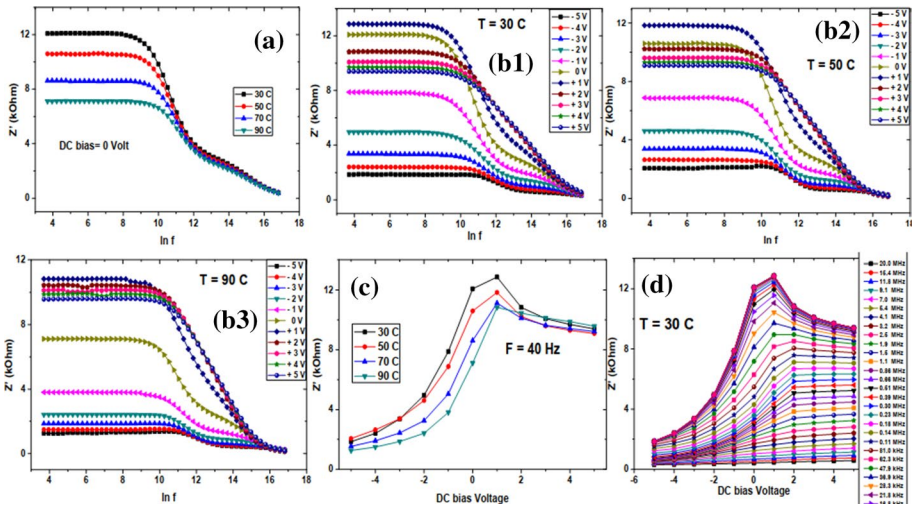

Fig. 5 **a** Z′ versus ln(f) at different temperatures at V = 0 V, **b1–b3** Z′ versus ln(f) at different voltages at T = 30, 50, 90 °C respectively, **c** Z′ versus V at different temperatures and f = 40 Hz and **d** Z′ versus V at different frequencies and T = 30 °C of Au/Ga As/n-Si/Al heterojunction

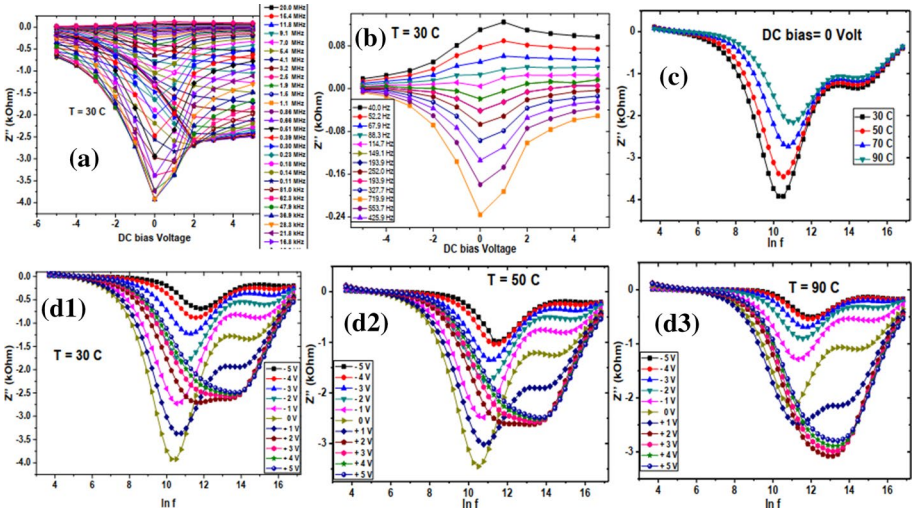

Fig. 6 **a** Z" versus ln(f)at different temperatures and V = 0 V, **b** Z" versus ln (f) at different voltages T = 30 °C, **c** Z" versus voltage at different frequencies and T = 30 °C, **d**1–**d**3 Z" versus frequency at different voltages and T = 30 50, 90 °C, respectively, of Au/Ga As/n-Si/Al heterojunction

in the range of (− 5 to 0 V), but increase with reducing voltage in the range of (5–1 V) in the low and high frequencies, but at higher frequencies Z′ values reached to minimum values. Figure 5(b1–b3) show the variation of temperature we can tune the values of impedance as displayed Z′ reached to maximum values at 30 °C and decrease with temperature. The impedance (Z′) was starting powerfully relying on temperature and voltage as displayed in plot 5(c). Also, The Z′ decrease with temperature, and voltage in negative region bias, but raise and caused peaks in the depletion and inversion region. It is noticed that Z′ has a peak moving to positive voltage regime for all curves. The impedance (Z′) dependence on voltage bias at different frequencies and constant T = 30 °C is shown in Fig. 5(d). It has been found that it decreases with frequency and raise in the depletion and inversion regime in the positive bias and decrease in the accumulation region. The temperature and frequency reliance are believed to start at interface states (Teffahi et al. 2016).

Figure 6(a, b) displays measured impedance–voltage (Z″–V) features of Au/n GaAs/p-Si/Al construction as function of frequency and voltage at T = 30 °C. The impedance (Z″) takes positive values at low frequency, but in high frequencies its values are negative and caused peaks in negative and positive region at about value 0 V as displayed in Fig. 6(a and b). Thus, the impedance transition voltage and the ratios of the impedances drop after transition are very similar (Kim et al. 2011; Wu et al. 2012; Doğan et al. 2015). The Imaginary impedance (Z″) takes positive values and reach to zero at low frequencies and reduce with reducing temperature taking negative values created peaks in the mid frequencies as displayed in Fig. 6(c). However, its values with different voltages created two peaks in mid and high frequencies and raise from (− 5 to 0 V) causing first peak and decrease form (2–5 V) forming second curve as demonstrated in Fig. 6(d1). We can tune the values of Z″ by variation of constant applied temperature as demonstrates of Fig. 6(d–d3), at 30 C. Z″ reached to maximum negative values and with raise temperature its negative values reduce as shown in Fig. 6(d2, d3).

The Cole-Cole diagrams of Z′ versus Z″, measured in a widespread range of frequency at dissimilar bias is revealed in Fig. 7a. The performance of impedance spectra is characterized by the existence of two semicircular curves whose radii are reliant on the bias voltage, demonstrating the presence of two relaxation mechanisms at entirely applied voltage. The semicircles radii enlarge with increasing the positive bias approving the altering of the electrical conductivity of the device. The size of the semicircle labels the electrical charge transmission or the recombination advances at the interface (Wang et al. 2016). This is because the interface is the location where two different materials having different permittivities meet. Moreover, it is where the charge carriers jump and pass to the other side once they have enough energy. The existing Cole–Cole diagram of the device can be established by the equal circuit, displayed in Fig. 7b. The circuit of the measured device can be signified by resistance, R_s and capacitance in series with a leak resistor, R_p resistance shaped from the electrode resistance, linked wires (Wei et al. 2013). parallel resistance, Rp and the capacitance, C are equivalent to the GaAs/Si interface.

The differences of tan(δ) versus voltage at different temperatures and frequencies at f = 40 Hz, T = 30 °C are displayed in Fig. 8(a and b), respectively. Tan(δ) values raise with temperatures taking negative values making a down spike 0 V and increase more in inversion than accumulation region as revealed in Fig. 8(a). the dielectric loss (tan(δ)) values raise with reducing frequencies and in negative bias voltage in the accumulation region as revealed in Fig. 8(b). This behavior resembles that reported in previous studies (Bengi and Bülbül 2013; Arslan et al. 2010). In the case of high frequency, the interfacial dipoles must fewer times to orientate themselves in the way of the irregular field (Sattar and Rahman

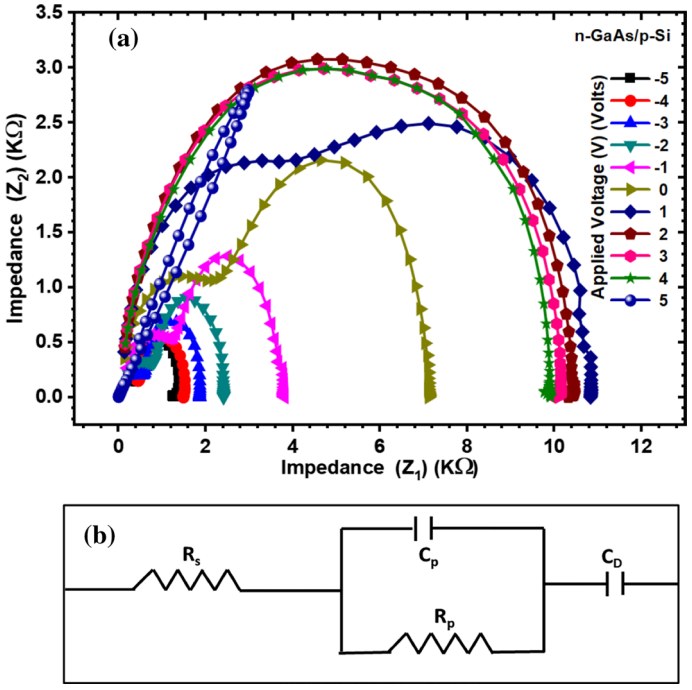

Fig. 7 **a** Cole–Cole plot at different bias voltages of Au/GaAs/n-Si/Al structure; **b** schematic diagram of the equivalent circuit of Au/GaAs/Si/Al junction

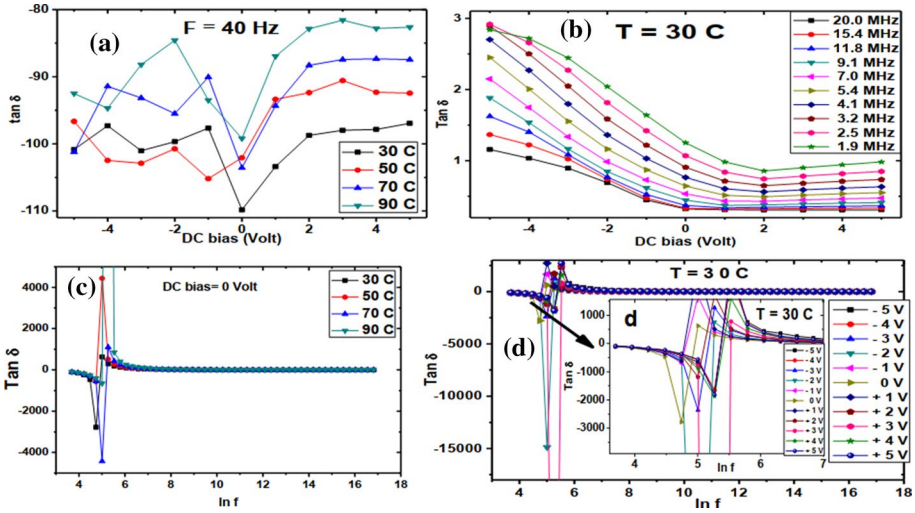

Fig. 8 **a** tan(δ) versus v at different temperatures and f = 40 Hz, **b** tan(δ) versus v at different frequencies and T = 30 C, **c** tan(V) versus ln (f) at different temperatures and V = 0 V, **d** tan(δ) versus lnf at different temperatures and T = 30 C of Au/Ga As/n-Si/Al

2003; Prabakar et al. 2003). The variation of tan(δ) with frequency at different temperatures and voltages at constant V = 0, T = 30 C respectively, Fig. 8 (c, d). Tan(δ) at low frequencies move from negative to positive values as shown in the inset of Fig. 8d. But in mid and high frequencies its values do not change.

3.3 I–V Characterization of Au/n-GaAs/p-Si/Al

Investigation of I–V characteristics is impactful tool for determination various parameters of diode including barrier height, series and shunt resistance as well as rectification ratio (RR)and ideality factor. Figure 9a demonstrated the temperature-dependent of the current–voltage (I–V) characteristic of Au/GaAs/p-Si/Al heterojunction underneath both the forward and reverse bias. A non-uniform I–V shape is noticed under forward and reverse bias reflecting diode-like characteristics. Figure 9b displays the high magnified reverse current-voltage scale to visualize the alteration of the current below reverse bias, which clearly show that the values of reverse current lies in micro ampere range, while forward current extended in milliampere rang. As can be seen in Fig. 9c, Our studied junction possesses a high apparent rectification varied from 200 to 1200 as the voltage change from 0.5 to 1.2 V. As expected, the rectification values decrease with temperature owing to the increase of reverse current as illustrated in Fig. 9d. The vital factors of the Au/GaAs/p-Si/Al structure that regulate the structure performance and significant for several applications are the shunt resistance (R_{sh}) and series resistance (R_s). Figure 9e is a demonstration of the variation of junction resistance (R_j) with a bias voltage (V). This Fig. is used for extracting the values of both series resistance (R_s) and Shunt resistance (R_{sh}) at high enough bias voltage forward and reverse voltages, respectively (Farag 2011). The values of series resistance were plotted as a function temperature in Fig. 2f. It is conspicuous that R_s and R_{sh} exhibits decrement with

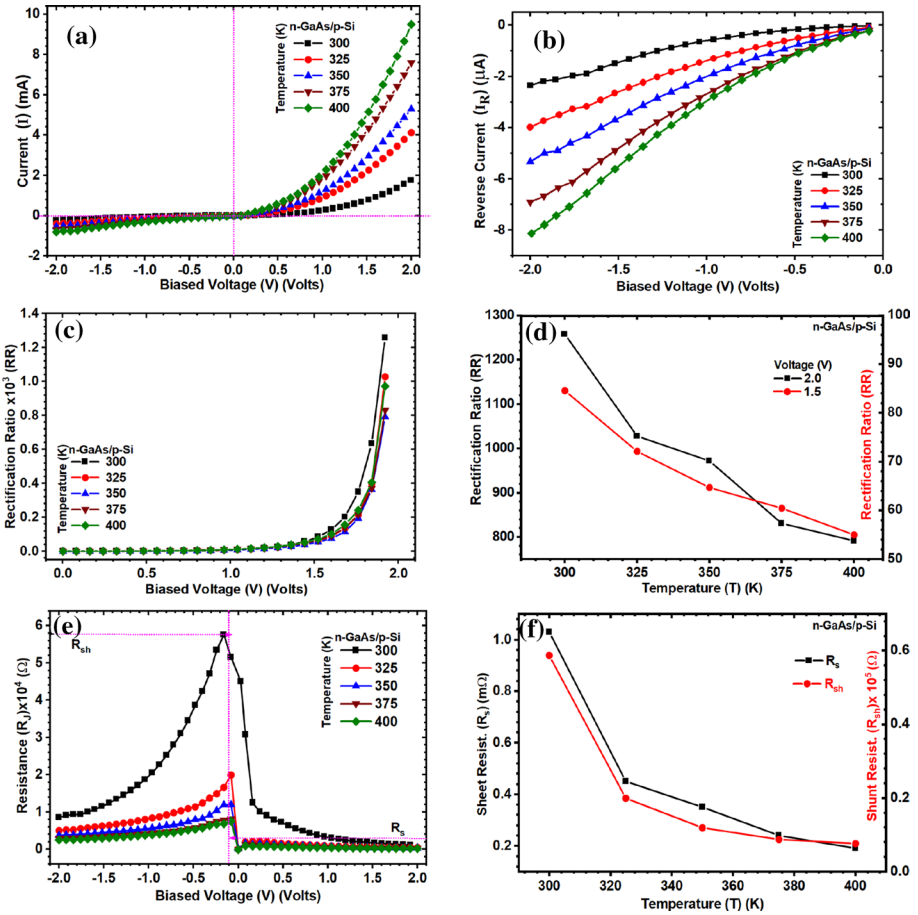

Fig. 9 **a** Current–voltage (I–V) characteristics; **b** enlargement of reverse current versus voltage over temperature range (300–400 K); **c** the bias voltage dependence of RR at different temperatures; **d** rectification ratio versus temperature at fixed voltage (1.5 and 2 V) to clarify the high rectification ratio; **e** junction resistance (R_J) versus voltage; and **f** the variation of sheet resistance and shunt resistance with temperature

growing temperature which ascribed to existence of the amount of free carriers' density, either by the mechanism of detrapping or bond breaking (Farag 2011). Additional reason behind the reduction of the R_s is the decrement of the ideality factor as the temperature rise (Demircioglu et al. 2011).

Figure 10a depicted the measured semi-logarithmic current–voltage (I–V) of the Au/GaAs/Si/Al structure measured in the temperature range from 300 to 400 K and scanned from −2 to 2 V. Apparently, a diode-like feature is noticed with rectification trend. Moreover, the created current is thermally started and can be defined by the thermionic emission mechanism (Ashery et al. 2010). In order to compute the various parameters of Au/GaA/Si/Al diode, the thermionic emission (TE) theory is applied by which the current and the voltage is connected by Özerli et al. (2017):

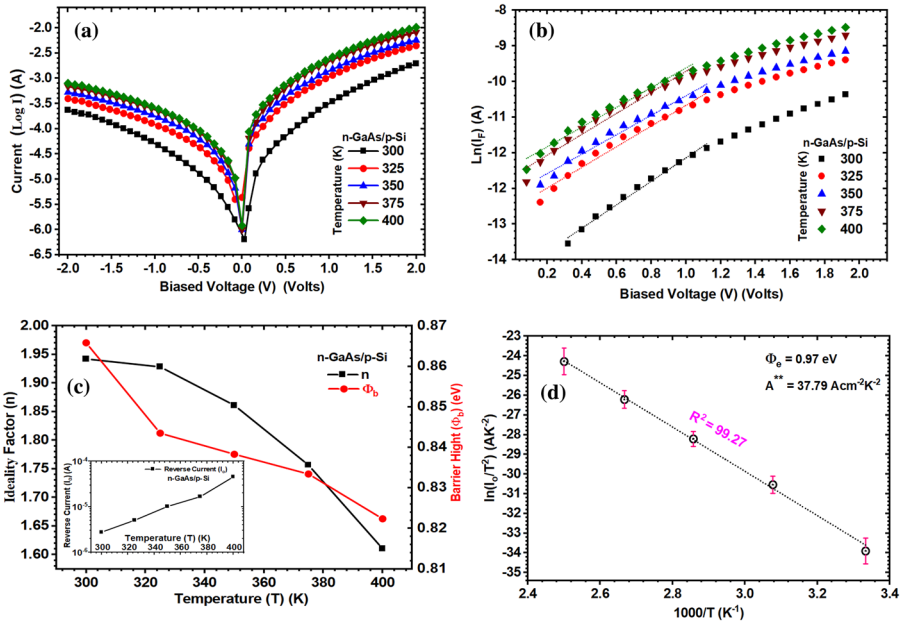

Fig. 10 For Au/GaAs/n-Si/Al diode: **a** log (I)-V characteristic of at different temperature range of 300–400 K; **b** Forward semi-logarithmic I–V relation for the diode at different temperatures, **c** the change of ideality factor and barrier height with temperature (T) and the inset figure represented the change of saturation current with temperature; and **d** the relation between logarithm of I0/T^2 and 1000/T showing thermionic conduction

$$I = I_0 \exp\left[\frac{q(V - IR_s)}{nk_B t}\right]\left[1 - \exp\left[\frac{-q(V - IR_s)}{k_B T}\right]\right] \tag{4}$$

where e denotes to electronic charge, V refers to the applied voltage, R_s is series resistance, n express the ideality factor, k_B is the Boltzmann constant (1.38×10^{-23} J/K), T refer to the absolute temperature and I_s is the reverse saturation current express by Sze and Ng (2006):

$$I_s = AA^* T^2 \exp\left[-\frac{e\varphi_b}{k_B T}\right] \tag{5}$$

where A express the area of diode, A* is Richardson constant equal to as 32 A cm^{-1} K^{-2} for p-Si, and φ_b is the barrier height. By employed Eqs. 4 and 5.

The ideality factor and barrier height can calculate by Rhoderick and Rhoderick (1978), Orak et al. (2014):

$$n(V) = \frac{qV}{K_B T \ln\left(I/I_0\right)} \Rightarrow n = \frac{q}{k_B T}\left(\frac{dv}{d\ln I}\right) \tag{6}$$

$$\varphi_b = \frac{kT}{q} \ln\left(\frac{AA^* T^2}{I_0}\right) \tag{7}$$

The semilogarithmic forward I–V Relation for Au/GaA/Si/Al was plotted for evaluation of ideality factors by using the slope and saturation current from the y-intercept as visualized in Fig. 10c. The forward current displays a strong exponential dependence with the applied voltage in the intermediate region and then deviate significantly from linearity at the high voltage region (V > 0.8 eV) owing to the influence of series resistance. The values of ideality factor saturation current and barrier height were calculated and listed in Table 1. Figure 10d manifests the variation of ideality factors (n) and values of barrier height (φ_b) with temperature which reduces by the rise of temperature. On the other hand, the saturation show strong increase with growing temperature as can be observed in inset of Fig. 10c. Figure 10d that connect between logarithm of I_0/T^2 versus 1000/T exhibits a strong linearity which asserts that major conduction mechanism is thermionic emission which is agreeable with other reported works.

3.4 Conduction mechanism

The profound examination of conduction mechanism in heterojunction is powerful tool to the know-in-depth the path and how the charges transport, which accordingly assisting us in knowing the limitations of conduction process in the junction. For that purpose, the I–V data is re-plotted, as presented in Fig. 9a, in terms of ln(I)–ln(V.), as illustrated in Fig. 11a. Apparently, two regions can be distinguished on the plot with different slopes, which can be examined by $I = AV^m$ power law. Here m expresses the slope of ln(I) versus ln(V) in each region whose values determine the type of conduction mechanism. The curves of the lower and higher voltage regions were fitted and the slopes were determined and tabulated in Table 2. The slopes of the high-voltage region ($m \approx 2$) suggesting that dominant mechanism might be assigned to space charge limited current (SCLC) dominated by single trap of distribution. This means that the majority kept trapped and the output arise from junction region and hence the current is low till all the trap level are filled. The current density of SCLC is described by Mott–Gurney law (Röhr et al. 2017):

$$J = \frac{9}{8}\varepsilon_0\varepsilon_r\mu\theta\frac{V^2}{d^3} \tag{8}$$

where ε_0 denotes the permittivity of free space(8.85×10^{-14} F/cm), ε_r infer the permittivity of GaAs (12), μ implies the mobility of GaAs, d is the layer thickness of GaAs (500 nm), V express the applied voltage and θ is the trapping factor described by El-Menyawy and Ashery (2014):

Table 1 Electrical parameters of Au/GaAs/n-Si/Al heterojunction

Temperature (K)	Conventional method			
	$\ln I_s$–V		dV/dI	
	n	Φ_b (eV)	$R_s \times 10^3$ (Ω)	$R_{sh} \times 10^4$ (Ω)
300	1.94	0.865	1.03	5.87
325	1.92	0.843	0.45	1.99
350	1.86	0.838	0.35	1.19
375	1.75	0.833	0.24	0.87
400	1.61	0.822	0.19	0.76

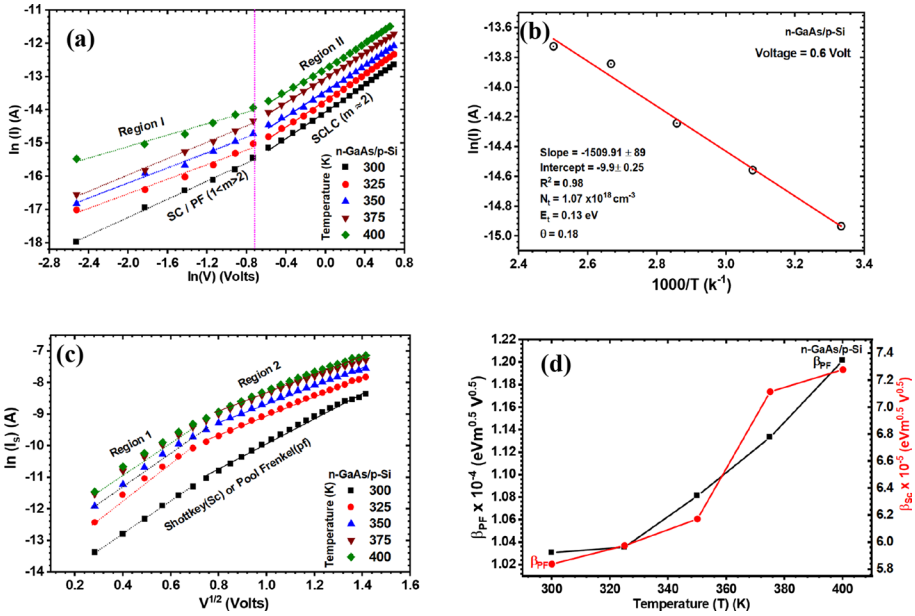

Fig. 11 For Au/GaAs/n-Si/Al diode, the variation between **a** ln(I) with ln(V); **b** The natural logarithm of the current and inverse temperature in SCLC region (V = 0.80 V); **c** ln(I) and $V^{1/2}$ in reverse bias, and **d** Schottky and Poole–Frenkel (PF) field-lowering coefficients with temperature

Table 2 The values of slope (m) in region 1 and 2 of the plot ln(I) versus ln(V) and values of β_{sc} and β_{PF} coefficients

Temperature (K)	Conduction mechanism			
	Forward (lnI–lnV)		Reverse (lnI_s–$V^{1/2}$)	
	Region I $1 < m < 2$	Region II $m \approx 2$	$\beta_{PF} \times 10^{-4}$ (eV $m^{1/2}$ $V^{1/2}$)	$B_{SC} \times 10^{-5}$ (eV $m^{1/2}$ $V^{1/2}$)
300	1.31	1.8	1.03	7.27
325	1.42	1.98	1.04	7.11
350	1.12	2.03	1.08	6.17
375	1.32	2.02	1.13	5.97
400	1.30	2.01	1.20	5.83

$$\theta = \frac{N_c}{N_t} \exp\left(-\frac{E_t}{k_B T}\right) \tag{9}$$

where N_c denotes to the effective density of states in the conduction band (9.5×10^{19} cm^{-3}) and N_t is the trap concentration located at energy level E_t underneath conduction band (CB). By combining the Eqs. 7 and 8 and plot the relation between $ln(I_S)$ and 1000/T at fixed voltage (0.8 V), as demonstrated in Fig. 5b, the N_t and E_t were found to be 1.07×10^{-18} cm^{-3} and 0.13 eV, respectively. Then the trapping factor can be determined by

substituting these parameters in Eq. 9, which found to be 0.17. in the law voltage region, the value of slopes $1 < m < 2$, which means that the Schottky or Poole–Frenkel is the prevailing mechanism.

For more detailed analysis about the dominant transport mechanism in the revers bias, the graphical representation of natural logarithm of the reverse current ($\ln I_s$) versus square root of applied voltage ($V^{1/2}$) all over the temperature range is pictured in Fig. 11c. The presence of two distinct regions exhibiting linear trend for each temperature is a strong proof for two different mechanisms. Such trend in reverse bias can be explained with reference to Schottky (Sc) or Poole–Frenkel (PF) effect. Therefore, the function that describe the link between reverse saturation current and applied voltage at fixed temperature can be expressed by Eqs. 1 and 2 for Schottky (Sc) or Poole–Frenkel (PF) mechanism (Gould 1996).

$$I_s = AA^* \exp\left[\frac{-q\varphi_{sc}}{k_B T}\right] \exp\left[\left(\frac{\beta_s}{k_B T}\right)\left(\frac{V}{d}\right)^{1/2}\right] \tag{10}$$

$$I_s = I_s \exp\left[\left(\frac{\beta_{PF}}{k_B T}\right)\left(\frac{V}{d}\right)^{1/2}\right] \tag{11}$$

where φ_{sc} is the barrier height for Schottky mechanism, d is the film thickness β_{sc} and β_{PF} are the Schottky and Poole–Frenkel (PF) field-lowering coefficients which corelate by the below expression (Ashery et al. 2017):

$$\beta_{PF} = 2\beta_{SC} = \sqrt{\left(\frac{q^3}{\pi\varepsilon_0\varepsilon_r}\right)} \tag{12}$$

ε_0 is the permittivity of vacuum, ε_r is the relative permittivity GaAs and q charge of electron. The slope of the linear portion of region 1 and region 2 for all temperature is determined and used for estimation of β_1 and β_2, respectively. The obtained values of β1 (Region 1-low voltage) and β2 (Region II-high voltage) are tabulated in Table 2 and plotted against temperate as depicted in Fig. 11d, which show that they increase with the rise of temperate. By comparison, it has been found that values of experimental β1 is close to that theoretical value of β_{PF} whereas $\beta_{2\,is}$ related to that of β_{sc}.

3.5 Band diagram

The energy band diagram of the Au/n-GaAs/p-Si/Al heterojunction at room temperature (300 K) is represented in Fig. 12. clearly the work function of n-GaAs is 4.65 and that of p-Si is 5.1, that is, the electrons will move from GaAs to the Si which allow the accumulation of charge at the interface. As a result, the band valance band and conduction band will show an upward curvature to keep the position of fermi level at the balance, as manifested in Fig. 12. therefore, a barrier is formed at the interface forming a good diode like behavior exhibiting a high rectification ratio as clarified in Fig. 9d.

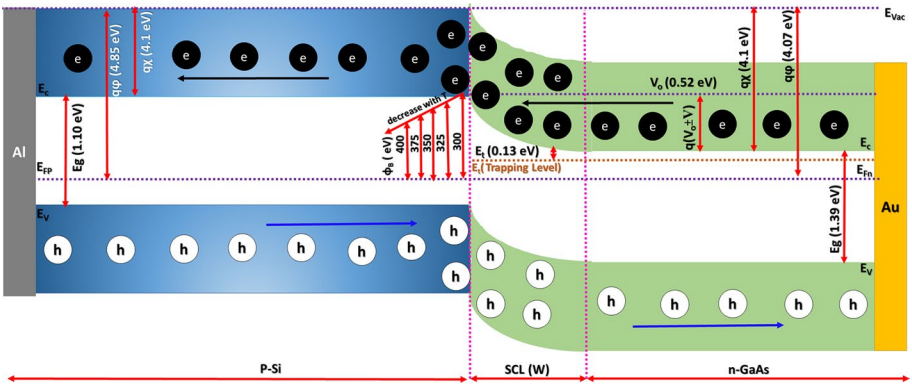

Fig. 12 Simplified representation of energy band diagram of Au/GaAs/n-Si/Al heterojunction

4 Conclusion

In this contribution, the main goal is manufacture of Au/n-GaAs/p-Si/Al structure as a schottky barrier diode by liquid phase epitaxial growth, and investigation it's electrical and dielectrically properties by C–V and I–V measurements. The novelty in this article is investigation of dielectric properties of Au/n-GaAs/p-Si/Al that investigators had not deliberate before, which stimulated us to study these properties. From examination of dielectric parameters such as Z′ and Z″, we can tuned the values of Z′, Z″ by difference of constant temperature, the values of Z′ and Z″ reached to maximum value at 30 °C and decrease with temperature increasing, Z″ takes positive and negative values depending on temperature. Z′ and Z″ are verification of the Cole–Cole diagrams. Also, can be tailoring the dielectric parameters such as C, G and tan(δ) by difference of voltage, temperature and frequency. Electric parameters such as Ideality factors, series resistance, shunt resistance, barrier height, rectification ratio was investigated from I–V measurement. The exploring of I–V features displayed that Au/n-GaAs/p-Si/Al have a noteworthy rectifying values ranged from 200 to 1200 as the bias voltage varied from 0.5 to 1.2 eV. with rising of temperature, the sheet (R_s) and shunt resistance (R_{sh}) exhibits decrement with temperate. Moreover, the values of ideality factors (n) and barrier height (φ_b) also reduce with temperature. The conduction mechanism has been extensively studied in both forward and reverse scan. It has been found at high voltage region that managed by space charge limited current dominated (SCLC) by single trap distribution. Also, the trap concentration and trap level were found to be 1.07×10^{-18} cm^{-3} and 0.13 eV, which placed directly below the bottom of conduction band as pictured by the band diagram of Au/n-GaAs/p-Si/Al architecture.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest. This research was not funded by any authority, entity or individual other than the authors themselves. They bear all the costs of the work.

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