

Influences of electrode material and design on the reliability of IRFPAs detector under thermal shock

Liwen $\mathrm{Zhang}^1 \cdot \mathrm{Na}$ Li $^1 \cdot$ Lu Song¹ • Qingduan Meng¹ • Meiyu Xu¹ • Zhen Lei¹

Received: 7 November 2016 / Accepted: 16 January 2017 / Published online: 23 January 2017 - Springer Science+Business Media New York 2017

Abstract Under thermal shock, high fracture probability in indium antimonide (InSb) infrared focal plane arrays (IRFPAs) limits its applicability. Typical fracture photographs under thermal shock shows that the cracks originating from the area above public electrode are dominant. In order to learn the influences of electrode material parameter and design on the reliability in InSb IRFPAs detector, the proposed improved equivalent modeling method is employed to build three dimensional InSb IRFPAs structure analysis model. Simulated results show that different electrode materials greatly influence the maximal thermal stress appearing in InSb chip and public electrode, and among the electrode material parameters, the coefficient of thermal expansion is the main affecting factor on thermal stress. With the increasing electrode thickness, the maximum thermal stresses in InSb chip and public electrode both decrease, which means the smaller electrode thickness leads to larger thermal stress in InSb chip and electrode. Besides, it is also found that adjusting the electrode layout to avoid the overlap between indium bumps and the embedded part of electrode can effectively reduce the stress concentration in the area of InSb chip above public electrode. All these are beneficial to optimize the structure of InSb IRFPAs and reduce the fracture probability.

Keywords Thermal shock · Reliability · Thermal stress · Finite element · Infrared detector

1 Introduction

In recent years, infrared focal plane arrays (IRFPAs) detector is a critical component in infrared imaging system, especially indium antimonide (InSb) IRFPAs detector with cutoff wavelength $5.5 \mu m$ at 77 K, is widely used in many military guiding system and civil

 \boxtimes Liwen Zhang lyzhangliwen@163.com

¹ School of Electrical Engineering, Henan University of Science and Technology, Luoyang 471023, China

applications (Benson et al. [2000](#page-8-0); Hoffman et al. [2004\)](#page-8-0). With the development of technology, there is a growing need for very large format IRFPAs to achieve simultaneously high resolution and wide field of view image data. A 4 \times 4 mosaic of 2 k \times 2 k HgCdTe SCAs with 67 million pixels were assembled for the VISTA telescope to survey the entire sky by Raytheon (Hoffman et al. [2006](#page-8-0)), and the Gigapixel IRFPAs for UVOIR Space Telescopes has been developed by the Space Telescope Science Institute, which has been up to 32 K \times 32 K elements in size, and consists of sixteen fully independent 8 K \times 8 K focal plane arrays (Ebbets et al. [2009](#page-8-0)). For InSb arrays, the large arrays with formats of 2 K \times 2 K pixels have also been built (Hoffman et al. [2004](#page-8-0)), and 4 K \times 4 K, 8 K \times 8 K devices presently have being developed (Davis and Greiner [2011\)](#page-8-0). But, due to the special structure of InSb IRFPAs, a very low yield limits its applicability, especially for large format. InSb IRFPAs is usually fabricated by flip chip bonding technology, typical hybrid FPA structure is showed as Fig. 1 (Rogalski [2004](#page-8-0)). That is, indium bumps are deposited on both detector array and Si ROIC dies, which are then hybridized together using a flip-chip bonder. Then the gap between bumps is backfilled with underfill. The electric contacts to the p-type layer in each pixel are made by indium bumps, and the electric connection to n-type layer is completed by the common negative electrode at the edge of the array (not shown in Fig. 1) (Zhang et al. [2013;](#page-8-0) Gektin et al. [1997](#page-8-0)). To reduce crosstalk, InSb chip is usually thinned to about 10 μ m. Besides, InSb IRFPAs needs to be mounted and stored in room temperature (300 K), and operate at liquid nitrogen temperature (77 K). The temperature fluctuation is over 200 K, fracture usually occurs due to the mismatch of the coefficients of thermal expansion (CTE) of neighboring components, which has been a main problem, especially in large format InSb IRFPAs.

Fig. 1 Hybrid FPA with independently optimized signal detection and readout (Rogalski [2004\)](#page-8-0)

The thermo-mechanical reliability of flip chip assemblies is usually assessed by numerical simulation technique in conjunction with experimental verification (Guo et al. [2013;](#page-8-0) Hegde et al. [2008](#page-8-0); Bai et al. [2014\)](#page-8-0). The finite element method is a powerful tool in optimization design of packaging. However, the simulations on traditional three dimensional (3-D) model of large format IRFPAs are very difficult, due to the complicated structure of IRFPAs detector and huge meshing number of large format IRFPAs. To solve the problem, the improved equivalent modeling method of ''first split, then equivalently replace'' is put forward in our previous paper (Zhang et al. [2013](#page-8-0)). The simulation results show the discontinuous stress extreme value appears in the area above the public negative electrode, which are consistent with the fracture photographs in experiment (Zhang et al. [2013,](#page-8-0) [2014](#page-8-0); Meng et al. [2014](#page-8-0)), these results also indicate that most of the cracks in InSb IRFPAs originate in the area above the public negative electrode.

To study the reliability and reduce the thermal stress in the crack originating area above the public electrode, basing on the improved equivalent modeling method, a 32×32 array is adopted to replace the real 128×128 array, a 3-D structural model of large format hybrid InSb IRFPAs is established in this article. We investigated the influences of electrode materials, electrode structure size and layout on the thermal stress and its distribution in large format InSb IRFPAs. All these lay a good foundation for structural design and optimization for large format InSb IRFPAs detector.

2 Modeling of InSb IRFPAs and material characterization

2.1 Finite element model

The commercial FEA software ANSYS is used for both finite element modeling and analysis. Basing on the proposed improve equivalent modeling method of ''first split, then equivalent" (Zhang et al. [2013\)](#page-8-0), a 128 \times 128 format IRFPAs is equivalent replaced with a small 32×32 format IRFPAs, and three dimensional (3-D) InSb IRFPAs model is shown in Fig. [2.](#page-3-0) Using the geometrical symmetry, only one-eighth of the actual structure is modeled here. The model is divided into two parts along the plane $S-P-Q$: the inner part is photosensitive element arrays, and the outer part includes public negative electrode and several rows/columns photosensitive elements array for testing or protecting. The structure of InSb IRFPAs comprises of five different materials, which are InSb chip, public negative electrode, indium bump arrays, underfill and Si ROIC from top to bottom. The enlarge side view along the $O'-P-O$ plane near the electrode and the division is shown in Fig. [2b](#page-3-0).

In this model, the thicknesses of InSb chip and Si ROIC substrate are 10 and 300 μ m, respectively. The indium bump diameter is 20 with 50 μ m pitch, the indium bump arrays and underfill has the interlacing distribution, with the same thickness of $10 \mu m$. And the public negative electrode has thickness range of $2-6 \mu m$. Since InSb IRFPAs flip chip process is completed at 370 K, the materials in IRFPAs are assumed to be stress free at this temperature. The assembly is uniformly cooled down from 370 to 77 K, and no thermal gradient and no transient heat transfer are considered in simulation. Due to the one-eighth of the actual structure, the symmetry boundary conditions are used on the symmetric O' - $P-O$ and $O'-Q-O$ planes, and single node constraint on the bottom surface center point of the package is also applied for avoiding movement. Meshing the whole model free, and a locally refine mesh pattern is maintained for accurate results.

Fig. 2 a Finite element model of InSb IRFPAs detector, and **b** Enlarge side view along the $O'-P-O$ plane near the electrode and the division

2.2 Material parameters

Indium (In) is commonly used as an attachment material in packaging structures intended for operation at extreme cold-temperature environment applications. For its high homologous temperatures, e.g., 0.70 Tm (in K) at room temperature (300 K), when the thermally activated strains impose on the attachment of indium, due to CTE mismatch between packaging materials, it gives rise to a complex deformation behavior. This deformation behavior is associated with the irreversible, temperature and rate (or time) dependent inelastic characteristics, are known to be viscoplastic, which is described with Anand model (Chang and McCluskey [2009\)](#page-8-0). Based on the compression test data, the material parameters of indium bump in Anand's model were acquired to simulate the steady-state viscoplastic behavior and stress/strain responses by Chang research group in 2009 (Chang and McCluskey [2009](#page-8-0)). Here, indium bump is built using VISCO107 element type, and the other materials are built using SOLID95 element type.

Underfill is usually described as classical constant elastic material, or described as viscoelastic material around glass transition temperature, once completely cured, it shows obvious temperature dependent elasticity, the temperature dependent CTEs of underfill were measured using a thermal mechanical analyzer (TMA) operated in expansion mode by He research group (He et al. [2000](#page-8-0)). For InSb IRFPAs, the service conditions require functions at cryogenic temperatures, even below the temperature of liquid nitrogen (77 K). The hybrid detector often undergoes a wide temperatures range from room temperature to cryogenic temperature. During this wide temperature change, not only the mechanical properties of underfill shows obvious temperature dependent elasticity, but the CTEs of other materials are not constant values. So, the temperature-dependent properties of the materials have to be employed, which are given in Table [1](#page-5-0) (Chang and McCluskey [2009;](#page-8-0) He et al. [2000](#page-8-0); Cheng et al. [2012;](#page-8-0) Hahn [1970](#page-8-0); White and Collins [1972\)](#page-8-0). All the other employed parameters are listed in Table [2](#page-6-0), where μ is the Poisson's ratio, α is the linear CTEs of underfill.

3 Results and discussion

3.1 Effects of different electrode materials on thermal stress

Copper (Cu) and Gold (Au) have excellent conductivity, widely used as the electrode materials in many flip-chip devices. Indium (In) is often used as an electrical connection material in packaging structures, due to its greater ductility and excellent conductivity at extreme cold-temperature environment. To learn the influences of electrode material parameters on the reliability in detector, three different materials Cu, Au and In are respectively adopted as the public negative electrode, the thermal stresses appearing in detector are studied. Under thermal shock, the Von Mises stress maximal values of all materials at three different electrode materials Cu, Au and indium are depicted in Fig. 3, here the electrode thickness keeps 4 μ m.

From these results, it is clear that the stresses in underfill, indium bump arrays and Si ROIC are approximately constant or have very little difference at three different electrode materials. However, the stresses appearing in InSb chip and public negative electrode don't keep unchanged, but have significant difference, especially between indium and the other two materials as the electrode. Specifically, when selecting respectively Au and Cu as the electrode, the maximal stresses in InSb chip are 503 and 512 Mpa; while selecting indium as the electrode, the maximal stress in InSb chip is up to 918 MPa, which increases nearly 81%. Conversely, selecting In as the electrode, the maximal stress in public negative electrode is 2.82 MPa, which much smaller than 242 and 323 MPa respectively for Au and Cu as the electrode. Apparently, the three materials have different material parameters in Tables [1](#page-5-0) and [2,](#page-6-0) but the similar stress change trend appears for Au and Cu electrode, the

opposite stress change trend for indium as the electrode. Through comparing and analysis, it can be found that Au and Cu have similar CTEs in Table 1, however In has much larger CTEs than the other two electrode materials. These results show that the CTEs are the main electrode material parameter to influence the thermal stress appearing in InSb chip and the electrode. Considering the cracks usually happen in thinner InSb Chip, although In has excellent malleability, ductility at extreme cold-temperature environment, it is not a good selection for the public electrode material. Due to its larger CTEs, the accumulated thermal stress in indium electrode is shifted to InSb chip through indium electrode distortion, which makes the stress in indium electrode become smaller and the stress in InSb chip become larger, the stress concentration in InSb chip makes it easier to fracture. Although there are similar stress change trends for Au and Cu electrode due to their similar CTEs, considering that copper is easily to be oxidized and Au has better ductility, malleability than Cu in extreme cold-temperature environment. To improve the stability and reliability of IRFPAs, Au is usually adopted to be the public electrode material in InSb IRFPAs.

3.2 Effects of different electrode thickness on thermal stress

To learn the effects of the electrode structure size on the reliability of InSb detector, the thermal stress in detector are simulated through changing the electrode thickness from 2 to 6 lm for a fixed electrode width. Considering its better ductility and stability, Au material is used as electrode in the following simulation. The simulated stress change rules are given in Fig. [4.](#page-6-0) To compare the simulation results, the model meshing, constraints and loading in any model are same. Apparently, as the electrode thickness increases from 2 to 6 lm, the stress maximum in Si ROIC, underfill and indium bump almost keeps at 350, 280, 2.8 MPa respectively, and almost does not vary with increasing electrode thickness. However, the maximal Von Mises stresses appearing in InSb chip and the electrode both decline gradually with the increasing electrode thickness, which have the similar varying tendency. The only difference is that the maximal stress in electrode reduces more quickly, when the electrode thickness changes from 3 to 4 μ m. It is worth noticing that the maximal Von Mises stress appearing in InSb chip is always much larger than that in other materials at different electrode thickness. This phenomenon is also consisted with that in Fig. [3](#page-4-0), which originates from stress concentration in thinned thickness $(10 \mu m)$ Insb chip. Even though underfill has the same $10 \mu m$ thickness, the maximal stress in underfill is also smaller than that in InSb chip because underfill has larger CTEs than InSb chip. From Fig. [4,](#page-6-0) it can be included that the thermal stress in InSb chip and the electrode are obviously affected by the electrode structure thickness. The larger electrode thickness, the stresses in InSb and electrode are smaller. From Fig. [2,](#page-3-0) it can been seen that the public

Materials	50 K	100K	150 K	200 K	250 K	300 K	350 K	400K
InSb chip	-0.2	2.38	3.91	4.38	4.75	5.1	5.53	5.82
Underfill	11.22	13.74	16.26	18.78	21.30	24.06	26.10	28.86
Indium (In) bump	23	27	27.5	28.5	29.5	31	32.4	33.5
Gold (Au)	7	10.41	11.53	12.86	13.38	14.1	14.15	14.2
Copper (Cu)	3.9	10.33	14.09	15.18	15.98	16.61	17.09	17.58
Si ROIC	-0.28	-0.33	0.5	1.41	2.1	2.62	2.98	3.25

Table 1 The CTEs of all the employed materials (10^{-6} K^{-1})

electrode locates in top of underfill between InSb chip and Si, and indium bumps are designed under the electrode to obtain electrical interconnections. Increasing the electrode thickness, accordingly the height of indium bumps under the electrode need to be decreased, but too small indium bumps will also bring the reliability and technology problems of solder joints. Considering the stress in electrode reduces more quickly during the electrode thickness changing from 3 to $4 \mu m$, the electrode thickness is selected to be 4 lm in the following discussion.

3.3 Effects of the electrode layout design on thermal stress

In InSb IRFPAs, the common negative electrode is arranged at the edge of the detector, which is attached to bottom surface of InSb chip. To obtain better electrical connection and bondability between p-type layer of InSb chip and the common electrode, one small part are often designed to insert into active p-type layer of InSb, as shown in Fig. [2b](#page-3-0). The stress distribution appearing in InSb chip is illustrated in Fig. [5a](#page-7-0). Apparently, the stress above the electrode area is much larger than other outer regions, especially above the overlap region of indium bumps and the embedded part of common electrode, there are discontinuous distribution of stress concentration. The position layout between the electrode and indium bumps below is given detailedly in Fig. [5](#page-7-0)b, it can be seen that the left column indium bumps have overlapped the embedded part of public electrode.

It can be deduced that the discontinuous distribution of stress concentration is attributed to two aspects, one is the area of InSb chip above the embedded part of Au electrode is much thinner, its anti-deformation intensity in the overlap region changes smaller, another

Fig. 5 a Stress distribution in InSb chip with electrode layout (b); c Stress distribution in InSb chip with electrode layout (d)

is that the indium bumps has larger CTEs and greater ductility than underfill, the accumulated thermal stress in indium electrode is shifted to InSb chip through indium electrode distortion. When the inserted part of common electrode is moved to the position between two columns indium bumps, as shown in Fig. 5d, the stress distribution of InSb chip is given in Fig. 5c. Comparing two stress simulation results, it can be found that the maximum Von Mises stress of InSb almost have no change, but the stress distribution above the electrode area is obvious different. In Fig. 5c, the stress concentration phenomenon above the electrode area become much smaller, and no obvious discontinuous distribution of extreme values. Obviously, avoiding the overlap between indium bumps and the inseted part of electrode is good to decrease the stress of InSb chip above the embedded part of electrode area and reduce the fracture originating from the electrode area.

4 Conclusions

Basing on improved finite element equivalent modeling method, a 128×128 format IRFPAs is equivalent replaced with a small 32×32 format IRFPAs, three dimensional InSb IRFPAs structure model is built. At the same time, taking account of the temperature dependence of coefficient of thermal expansion, the effects of electrode materials, structure size and layout on the thermal stress and its distribution in large format InSb IRFPAs are analyzed. Simulation results show that the coefficient of thermal expansion and structure size of common electrode material obviously influence the thermal stress appearing in InSb chip and common electrode. Combining with material and structure parameters, these simulation results are beneficial to optimize the design of InSb IRFPAs. And adjusting the electrode layout and avoiding the overlap between indium bumps and the inserted part of common electrode can effectively reduce the stress concentration in the electrode region. These simulation results are favorable to more comprehensive understanding of the influences of electrode material, structure size and layout on the reliability of InSb IRFPAs, and improving the production ratio.

Acknowledgements This research has been supported by National Natural Science Foundation of China (Nos. 61205090, 61107083), Education Bureau of Henan Province for the Young Core Teacher of University (No. 2014GGJS054), Foundation of Educational Commission of Henan Province (Nos. 14A510003, 15A470012) and Youth Foundation of Henan Science and Technology University (No. 2014QN027).

References

- Bai, J., Hu, W.D., Guo, N., Lei, W., Lv, Y.Q., Zhang, X.L., Si, J.J., Chen, X.S., Lu, W.: Performance optimization of InSb infrared focal-plane arrays with diffractive microlenses. J. Electron. Mater. 43(8), 2795–2801 (2014)
- Benson, R.G., Forrest, W.J., Pipher, J.L., Glaccum, W.J., Solomon, S.L.: Spatial distributions of hole traps and image latency in InSb focal plane arrays. In: Proceedings of SPIE, vol. 4131, pp. 171–184 (2000)
- Chang, R.W., McCluskey, F.P.: Constitutive relations of indium in extreme-temperature electronic packaging based on Anand model. J. Electron. Mater. 38(9), 1855–1859 (2009)
- Cheng, X., Liu, C., Silberschmidt, V.V.: Numerical analysis of thermo-mechanical behavior of indium micro-joint at cryogenic temperatures. Comput. Mater. Sci. 52(1), 274–281 (2012)
- Davis, M., Greiner, M.: Indium antimonide large-format detector arrays. Opt. Eng. 50(6), 061016 (2011)
- Ebbets, D., Blouke, M., Freymiller, E., McArthur, S., Warren, P.: Gigapixel Focal Plane Arrays for UVOIR Space Telescopes. <http://www.stsci.edu/institute/atlast/atlast-documents-articles> (2009)
- Gektin, V., Bar-Cohen, B., Ames, J.: Coffin-Manson fatigue model of underfilled flip-chips. IEEE Trans. Compon. Pack. Manuf. Technol. 20(3), 317–326 (1997)
- Guo, N., Hu, W.D., Chen, X.S., Lei, W., Lv, Y.Q., Zhang, X.L., Si, J.J., Lu, W.: Optimization for midwavelength InSb infrared focal plane arrays under front-side illumination. Opt. Quantum Electron. 45(7), 673–679 (2013)
- Hahn, T.A.: Thermal expansion of copper from 20 to 800 K—Standard Reference Material 736. J. Appl. Phys. 41(13), 5096–5101 (1970)
- He, Y., Moreira, B., Overson, A., Naka, S., Bider, C., Briscoe, J.: Thermal characterization of an epoxybased underfill material for flip chip packaging. Thermochim. Acta 357–358(14), 1–8 (2000)
- Hegde, P., Ochana, A.R., Whalley, D.C., Silberschmidt, V.V.: Finite element analysis of lead-free surface mount devices. Comput. Mater. Sci. 43(1), 212–220 (2008)
- Hoffman, A.: Semiconductor processing technology improves resolution of infrared arrays. Laser focus world, 81–84 (2006)
- Hoffman, A.W., Corrales, E., Love, P.J., Rosbeck, J.P., Merrill, M., Fowler, A., McMurtry, C.: 2K x 2K InSb for astronomy. In: Proceedings of SPIE, vol. 5499, pp. 59–67 (2004)
- Meng, Q.D., Gui, L., Zhang, X.L., Zhang, L.W., Geng, D.F., Lv, Y.Q.: Delamination study of InSb infrared focal plane arrays using a cohesive zone model. Acta Phys. Sin. Ch Ed 63(11), 118503 (2014)
- Rogalski, A.: Optical detectors for focal plane arrays. Opto Electron. Rev. 12(2), 221–245 (2004)
- White, G.K., Collins, J.G.: Thermal expansion of copper, silver, and gold at low temperatures. J. Low Temp. Phys. 7(1–2), 43–75 (1972)
- Zhang, L.W., Shao, M., Zhang, X.L., Meng, Q.D., Wang, J.C., Lv, Y.Q.: Three-dimensional modeling and simulation of large-format hybrid indium antimonide detector arrays. Opt. Eng. 52(10), 103110 (2013)
- Zhang, X.L., Meng, Q.D., Zhang, L.W., Lv, Y.Q.: Negative electrode structure design in InSb focal plane array detector for deformation reduction. J. Mech. Sci. Technol. 28(6), 2281–2285 (2014)