

# Electrical and spectral characterization of CdS/Si heterojunction prepared by plasma-induced bonding

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**Abstract** In this work, the characteristics of the CdS/Si structure produced by plasma-induced bonding technique were studied. The produced structure was an asymmetric heterojunction consisting of n-type CdS on a p-type silicon substrate. The Si substrate and CdS sample were bonded by subjecting them to the plasma formed between two electrodes. The measurements included the structural and electrical characteristics. The typical spectral responsivity within the range 400–800 nm and the maximum value is at 577 nm. With dark current of 6  $\mu\text{A}$ , maximum reverse bias current of 670  $\mu\text{A}$  and ideality factor of 3.5, the results explained better characteristics than those of the same heterojunction produced by other deposition techniques.

**Keywords** CdS/Si structure · Heterojunction · Plasma-induced bonding · Low-dimensional structures

## 1 Introduction

Direct bonding means the joining of two smooth and clean surfaces at room temperature (Zhou et al. 2000). No constraint on lattice matching exists and after joining the two surfaces, the bonded pairs are annealed at a high temperature to ensure the formation of strong bonding (Mathine 1997). With proper procedure the bonded interface can achieve bulk strength (Stengl et al. 1988).

If two solids with clean and flat surfaces are brought into close proximity at room temperature, attractive forces pulls the two bodies together into intimate contact so that bonds can form across the interface (Widdershoven et al. 1990). The phenomenon was

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given rather little attention until in the last decades when semiconductors bonding found several applications in micromechanics, microelectronics and optoelectronics (Gösele et al. 1995).

There are many factors governing the bonding behavior of two surfaces. First, the surfaces must be flat and smooth (Takagi et al. 1996). Usually it is argued that surfaces can make contact only at some asperities. However, the success of bonding technique has followed the development of modern semiconductor chemical–mechanical polishing (CMP) technology (Gösele et al. 1995). The semiconductor polishing technology has reached such a level of maturity that, nowadays, commercial silicon wafers have surface roughness in the order of  $10^{-10}$  m. The second parameter governing the ability for bonding is the surface chemical state and surface termination (Berthold et al. 1998). For most semiconductors, surface preparation and cleaning techniques are well-developed and characterized. However, in silicon technology the surface chemical treatments are more standardized and established processes, as compared to, for example, compound semiconductors (Tong et al. 1998).

One of the great potentials of the bonding approach is the integration of dissimilar materials (Krauter et al. 1997). Integration of dissimilar semiconductor by heteroepitaxial growth is hampered by the difference in lattice constants. Particularly, combining compounds semiconductors with highly developed silicon circuits has been pursued in recent years with the goal to incorporate photonic and high-speed devices with advanced silicon technology (Levine et al. 1999).

When the solids are bonded together at room temperature, usually the interaction, or bonding energy, is relatively weak (Black et al. 1997). Therefore, a heat treatment is performed to increase the bond-strength. The annealing enhances out-diffusion of interface trapped molecules and desorption of chemisorbed surface atoms, such as hydrogen (Wada et al. 1999). At the same time the annealing activates formation of covalent bonds between the bonded surfaces, like solid-to-solid bonding in the case of hydrophobic bonding. The thermal treatment used to increase the bond-strength can, unfortunately, also cause severe problems in bonding technique. For instance, when bonding dissimilar materials, the thermal mismatch induced high stresses in the material (Kikuchi and Adachi 2000). High temperature annealing also restricts the use of metal patterns and can cause diffusion of dopants (Zazzera and Moulder 1989).

Chemically reactive plasma discharges are widely used to modify the surface properties. The relative importance of a specific discharge depends on input power, gases, reactor volume and geometry, gas flows, etc. For instance, plasma discharges are employed for etching, deposition or surface cleaning (Kish et al. 1995). The gas-chemistry and the plasma parameters (effect, applied voltage, pressure, plasma density, etc.) that are being used govern the plasma/surface interactions (Gösele et al. 1995). A variety of gases are such as Ar, O<sub>2</sub>, SF<sub>6</sub>, Cl<sub>2</sub> and CHF<sub>3</sub> are used for this purpose.

Wafer bonded p-n heterojunction characteristics are heavily affected by the non-ideal interface. However, a substantial improvement of wafer bonded p-n heterojunctions characteristics is usually obtained by shifting the p-n transition away from the bonded interface, either by high temperature annealing or by implantation (Kopperschmidt et al. 1997; Hawkins et al. 1996).

In this work, the use of plasma activation of the surfaces before bonding has been examined to achieve a low-temperature bonding of cadmium sulfide and silicon samples to form a heterojunction for photodetection applications.

## 2 Experimental work

High purity (99.999) (100)-oriented p-type silicon wafers of 500  $\mu\text{m}$  thickness and 3  $\Omega\text{ cm}$  resistivity were used in this work. Also, high purity (99.999) cadmium sulfide (CdS) was used to form 350  $\mu\text{m}$ -thick samples. Both samples, Si and CdS, were washed with distilled water then rinsed in ethanol and subjected to ultrasonic waves for 10 min, then dried by hot air. The silicon samples were then cleaned with HF for 5 min to remove any residual oxides which have existed on their surfaces. Both samples were softly grinded and polished to obtain flat surfaces. Then, these samples were rinsed in ethanol to remove acids then dried to be ready for processing. More details can be found in previous works of the author (Hamadi 2007, 2008).

The Si and CdS samples were mounted inside the homemade plasma system, which is working under vacuum of ( $10^{-10}$  mbar) at room temperature. The silicon substrate was mounted on a holder made of stainless steel at a specified distance from the anode and the CdS sample was placed on the Si substrate. The samples were placed at a position that the plasma is entirely surrounding the sample. Discharge voltage and current are 15 kV<sub>DC</sub> and 3 A, respectively. Argon gas at a pressure of (1 mbar) was used to generate the discharge plasma. The sample was maintained inside the operated system for 10 min before being removed and tested.

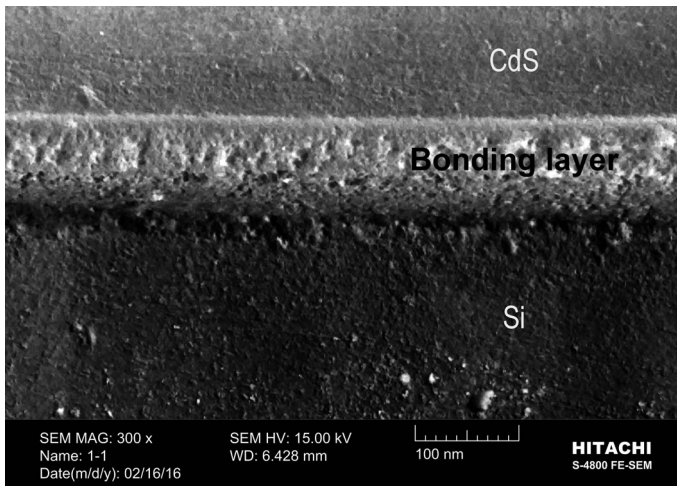
Before bonding, the native oxide is removed from the surfaces to have a solid-to-solid bonding (Kikuchi and Adachi 2000). However, the bonding is very weak at room temperature and after low-temperature annealing because of the hydrogen-terminated surface. A high-temperature annealing above 520 °C is necessary to desorb hydrogen from surface and enable a covalent bonding.

Electrical measurements were carried out using a Farnell DC power supply and Keithley-616 digital electrometer while the C-V measurements were performed using *hp/4192* ALF LCZ device. The samples were subjected heating up to 600 °C within 5 min then left to return to its initial temperature within the same period of time. The nanoscale structure of the treated samples was introduced using Hitachi S-4800 FE-SEM instrument.

Five samples were prepared to introduce the repeatability of this technique. Along 5 days, a sample was daily prepared and processed at the same conditions and the presented results are the average of these samples. Therefore, this technique has very good repeatability as the preparation and processing conditions are kept stable as possible. The experimental preparation and processing conditions mentioned above can be considered as the optimum to obtain the best results in this work.

## 3 Results and discussion

If two identical solids with the same orientation are bonded together without misalignment and without interface contamination, they should merge into one. However, there are always deviations from the ideal case. In the bonding technique, there is always an unavoidable misalignment between the bonded solids and therefore misfit dislocations appear. Misfit dislocations will also appear at the bonded interface if two solids of different orientation or different lattices are bonded. The presence of native oxides, adsorbed surface contaminants and interface bubbles (voids), also inhibit a perfect solid-to-solid transition region. Figure 1 explains the nanostructure of the bonded CdS/Si samples.



**Fig. 1** The SEM micrograph of the CdS/Si structure where the boundary and defects are shown

Defect-etching techniques were found to be more suited for investigations of bulk material defect introduced by the bonding technique, arising mainly from thermal mismatch stress. Defect-etching uses etch selectivity to reveal crystal imperfection such as dislocation. The dislocation appears as pits on CdS/Si bonding interface, as shown in Fig. 1.

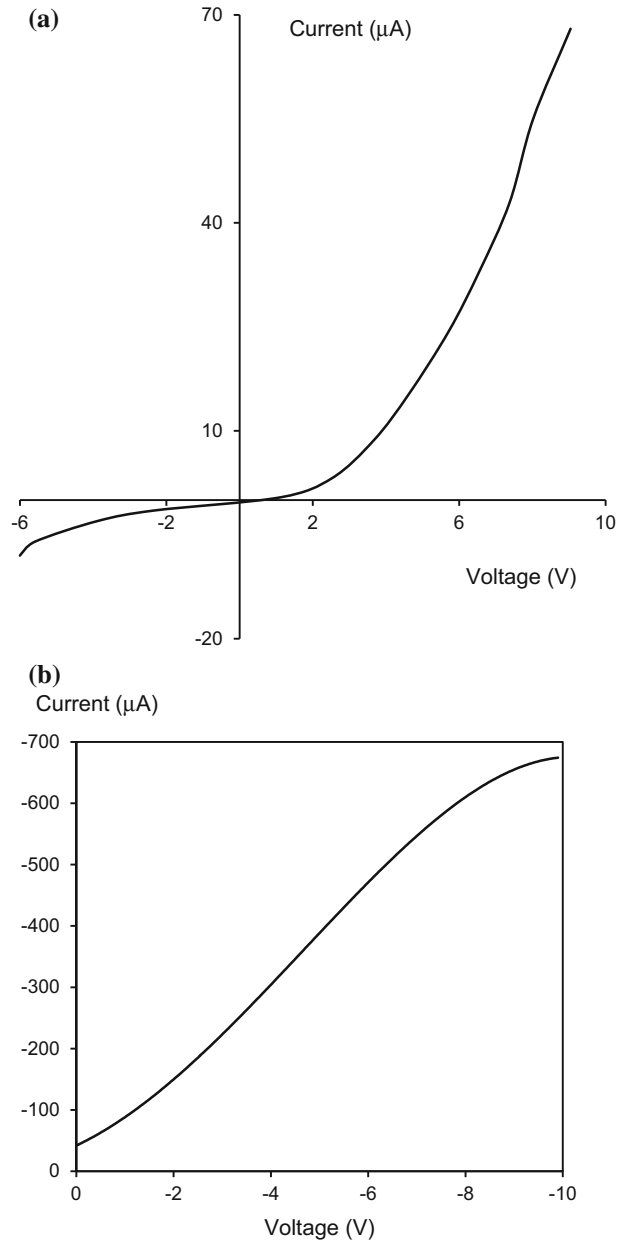
A generalized theory for bonding technique may be difficult to achieve since the electrical properties of the bonded interface depends on many parameters. The electrical properties vary between different reports and it is likely that such deviations are linked to variations in bonding procedures. The disordered interface being composed of misfit dislocation acts as gettering and segregation site in the same way as grain boundaries in polycrystalline semiconductors.

The p-n heterojunction formed under ultra-high vacuum (UHV) conditions and low-temperature results in an ideality factor no more than 2 and indicates low recombination at the interface. Bonding p-n heterojunction in ambient air and subsequent high temperature annealing was seen to yield high recombination near the bonded interface. Figure 2 shows the I–V characteristics of bonded n-p CdS/Si heterojunction. The dark current is about  $6 \mu\text{A}$  and the forward current is uniformly linear while photocurrent up to  $670 \mu\text{A}$  was measured at illumination level of 10 mW. The fabricated heterojunctions exhibit an average ideality factor of 3.5.

The bonded interface is often avoided in the electrically active region of the electronic device. However, the recombination centers of the defective bonded interface are used to control the minority carrier lifetime in power devices.

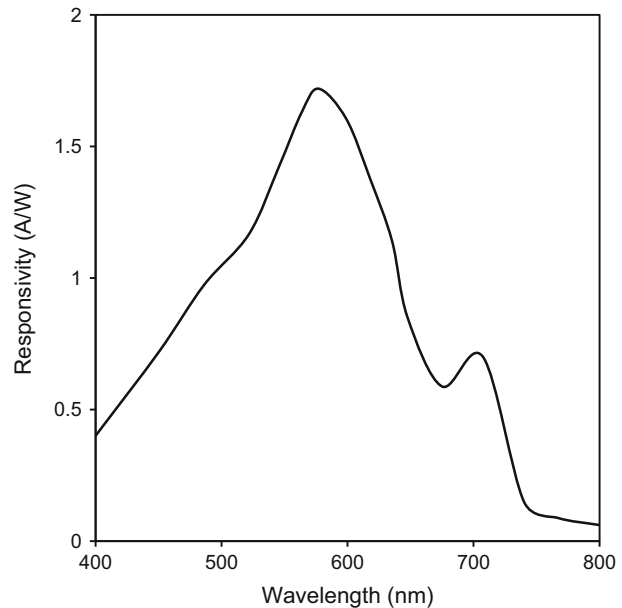
The spectral responsivity of the CdS/Si heterojunction was determined as a function of wavelength as shown in Fig. 3. This heterojunction responds in the 550–600 nm range much more than in the range below 550 nm and beyond 600 nm while the maximum responsivity is observed at 577 nm. Another peak of responsivity can be observed at 707 nm. This cheap technique presents an advantage to produce good photodetectors for the wavelengths within 500–600 nm.

**Fig. 2** The I–V characteristics in dark (a) and under 10 mW illumination (b) for the CdS/Si heterojunction prepared in this work



Integration of CdS and Si has attracted much interest since the unique properties in each material can be combined in devices or systems, such as CdS-based piezoelectric devices and optoelectronics components. The epitaxial growth of CdS on Si substrate is hampered by the difference between the lattice constants of the materials. However, using bonding for the integration, the lattice-mismatch becomes no obstacle.

**Fig. 3** The spectral responsivity of the CdS/Si heterojunction prepared in this work



In each material system, nature has imposed a set of physical properties, such as mobility, optical absorption, resistivity, thermal and mechanical properties. For a given application, the optimal properties may not reside in a single material but in a variety of dissimilar materials. A specific case is to combine compound semiconductor that have direct band gap and high mobility with Si that is extensively used in microelectronic applications.

For lattice-matched materials systems, the material integration is extensively and routinely realized using heteroepitaxy. However, for material systems that are largely lattice-mismatched, heteroepitaxial growth has not been able to produce the high quality material needed in optoelectronics (Yamaguchi et al. 1995; Pasquariello and Hjort 2000; Fontcuberta i Morral et al. 2003).

## 4 Conclusions

A CdS/Si heterojunction was produced by plasma-induced bonding techniques. The structural characteristics explained the good bonding interface between the CdS and Si samples. Electrical measurements showed reasonable enhancement in the heterojunction characteristics compared to that produced by another techniques. Despite the complexity imposed by the plasma processing system, production of heterojunctions with such enhanced characteristics has advantages of low cost and large size devices.

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