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Improved design of all-optical photonic crystal logic gates using T-shaped waveguide

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Abstract In this paper, we propose new structures of all-optical logic gates based on two-dimensional photonic crystal of square type lattice with Si rods in air background. The proposed structures are based on T-shaped waveguide with optimized edge rod radius. An extra reference input port is included in the structure along with the actual input ports required for a logic gate. The simulation results show that the proposed T-shape waveguide can work as a NOT gate and a dual T-shape waveguide can work as NOR, XNOR and NAND gate with proper change in the phase values of logic '1' input. The proposed structures have fast response time with value not more than 0.35 ps. The size of these structures is also small. It is expected that these new T-shaped structure based all-optical logic gates are suitable for large scale optical integration and can potentially be used in on-chip photonic integrated circuits.

Keywords Photonic crystal · T-shaped waveguide · All-optical logic gates · Interference

1 Introduction

The need of all-optical signal processing techniques have been increased dramatically with the development of telecommunication systems for high data transfer speeds and capacity. These techniques are also expected to be the main supporting techniques in future all-optical information networks (Xu et al. 2009; Ji et al. 2011). All-optical logic gates are the basic components evolved from these all-optical signal processing techniques which acts as

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the key components in achieving various networking functions (Ramos et al. 2005; Liu et al. 2013) such as optical computing, clock recovery, signal regeneration, encoding etc. Various approaches have been reported on implementing all-optical logic gates which can achieve high processing speed and high level of integration. For instance, Semiconductor Optical Amplifier (SOA) based nonlinear switches playing a major role in modern optical computing (Soto et al. 2002; Chattopadhyay et al. 2009; Al-Zayed and Cherri 2010; Chattopadhyay and Roy 2011; Cherri 2011; Mehra et al. 2012). Mach–Zehnder Interferometer (MZI) based SOA and the Terahertz Optical Asymmetric Demultiplexer (TOAD) are the examples of SOA based optical logic gates. The MZI based on electro-optic effect is also used to design the all-optical gates (Kumar et al. 2013; Kumar et al. 2014) wherein the logical functioning is performed by varying the electrode voltages. Optical fibers are also become a source in implementing all-optical logic gates (Menezes et al. 2007). But, most of these works are affected with certain limitations such as low speed, big size and difficult to perform chip-level integration. Moreover, the logic gates based on SOA based method are inevitably affected by spontaneous noise (Wang et al. 2006, 2007). Photonic Crystal (PhC) based logic gates can be a better alternative to all these approaches due to their unique properties such as high speed, compactness, low power consumption and better confinement.

Photonic crystal is a versatile platform to construct devices with dimensions of few wavelengths of light being confined. A lot of research work has been done on the realization and optimization of PhC based logic gates. Few of them are Multi Mode Interference (MMI) (Ishizaka et al. 2011; Tang et al. 2014), self-collimation effect (Zhang et al. 2007; Christina and Kaliban 2012), photonic crystal ring resonators (Bai et al. 2009; Yang et al. 2013; Ghadrdan and Mansouri-Birjandi 2013a, b; Bao et al. 2014; Raghda et al. 2014), Y-shaped PhC waveguides (Rani et al. 2013) and also the combination of PhC ring resonator and Y-shaped waveguide (Aryan et al. 2015). To the best of our knowledge, PhC based all-optical logic gates have not been designed so far using T-shaped waveguide. Furthermore, the response time of the proposed all-optical logic gates as well as their size are far better than the recently reported PhC based logic gates.

In this paper, we have proposed all-optical NOT, NOR, XNOR and NAND logic gates using T-shaped waveguide. An extra reference input has been added in these structures which helps in providing the output power when data inputs are not applied. The proposed structure with one T-junction can work as a NOT gate and the structure with two T-junctions can work as NOR, XNOR and NAND logic gate with proper change in the input phase values of logic '1'. The performance of the proposed structures are analyzed and simulated by using Plane Wave Expansion (PWE) and Finite Difference Time Domain (FDTD) methods. By optimizing the radius of the edge rod at the first T-junction, a good contrast ratio with less reflection into the unemployed input is obtained. The response time of the proposed logic gates is also less when compared to the respective PhC based all-optical logic gates.

2 Need of reference input

Photonic crystal based logic gates can be designed by using interference based phenomena. In the interference based logic gates except the MMI based designs, the intensity of the light defines the input logic value. No light is considered as logic '0' and a light signal is considered as logic '1'. This will create a problem in the design of the logic gates such as NOT, NOR, XNOR and NAND while the input(s) is(are) zero (i.e., when $A = 0$ for NOT

gate and A = B = 0 for the remaining gates, where A and B are the inputs of the logic gate). At this input condition, the logic gate needs to produce a light signal which is considered as logic '1'. It is impossible to produce an output light signal when input light is not applied. So, there is a need to have a light source in the structure which can provide an output light signal when input light is not available. Recently, this limitation in interference based designs is eliminated by introducing an extra input referred to be a reference input to design XNOR, NAND gates (Yulan et al. 2013) and also a NOT gate (Yulan et al. 2013; Wu et al. 2012). In the absence of the input light signals, the reference input becomes a source for the output power to be produced as logic '1'. Though the reference input needs an extra input port, this limitation in the interference based designs can be eliminated as well. Similarly, in the logic gates which are designed using this phenomena, there is a need to produce logic '0' or logic '1' as an output when only one input is applied i.e., when A = 1 or B = 1. In order to achieve such an output, the interference length and width of the photonic crystal structure is to be changed (Lee et al. 2008) or sometimes the nonlinear rods are to be created along with change in the interference length and/or width of the structure (Zhu et al. 2006; Danaie and Kaatuzian 2011). This attempt of changing the interference length and width of the photonic crystal structure will increase the size of the structure. In order to solve this problem, the reference input can also be used in such a way that it can be destructively interfere with the input light to produce the required logic '0' output or constructively interfere with the input light to produce logic '1' output. This will avoid the need of changing the interference length and width of the structure as well as the increase in size of the structure. The type of interference can be obtained by having an appropriate path difference as well as the phase difference between the light beams from the input ports and the reference input.

The logic gates designed previously with reference input such as NAND gate (Yulan et al. 2013) and NOT gate (Wu et al. 2012) need to have a reference input power larger than the input beam. The proposed T-shaped waveguide will eliminate this limitation by using a corner rod at the junction made with an impure flint glass material with refractive index 1.92. This glass rod is placed at the corner of the junction towards the output side. This rod will allow the light to concentrate towards the output port of the T-shaped waveguides when inputs are not applied. The proposed T-shaped waveguide based logic gates need the reference input power same as the applied input beam. Moreover, in the proposed logic gates the phase of the reference input is constantly maintained at 180° and the phase of the light signal at the remaining input ports A and B varies with respect to the required type of the output logic.

3 T-shaped photonic crystal waveguide as NOT gate

A T-shaped PhC waveguide can be used as a NOT gate with one of the horizontal port as an output port and the remaining two ports as the input. Among the input ports, the vertical port is applied with the reference input which is very helpful in providing the output power though the inputs are not applied. The junction rods play an important role in the operational behavior of the structure.

3.1 Operating principle

A two-dimensional photonic crystal with T-shaped waveguide is shown in Fig. 1 consists of 9 × 9 array of Si rods with air background. The refractive index of the Si rod is 3.46.

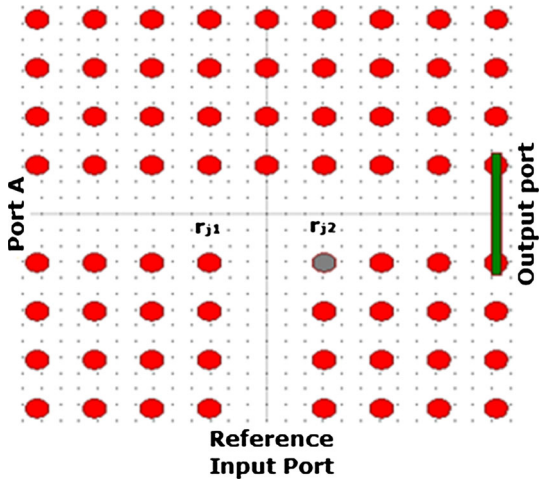

Fig. 1 Proposed structure of NOT gate with T-shaped waveguide

The lattice constant a and the radius of the Si rod are 600 nm and $0.2a$, respectively. Photonic band diagrams are calculated for this structure using PWE method. Three photonic band gaps can be observed in which two are for TE mode and one is for TM mode. Among the three, one of the band gap of TE mode is suitable for third telecommunication window with the range 0.28256 (a/λ) to 0.41693 (a/λ) as shown in Fig. 2. This uniform PhC structure will not allow the light of wavelengths between 1.43 μm and 2.12 μm to pass through it and thus completely reflects them.

The interference of the two input light beams depend upon the wave optics theory. According to wave optics theory, a constructive interference occurs when two light beams differ by a phase difference of $2k\pi$ (where $k = 0, 1, 2,\ldots$). Similarly, a destructive interference occurs, when two light beams differ by a phase difference of $(2\,k + 1)\,\pi$ (where $k = 0, 1, 2,\ldots$). The light beams through input port A and reference input port will interfere with each other either constructively at a phase difference of 0° or destructively at a phase difference of 180°. The reference input beam is always applied with a phase of 180° irrespective of the input. Reference input is always applied in both the input combinations ($A = 0$ or 1). Here, no light is considered as logic '0' input. We maintain the phase of the reference input at 180° for all the logic gate structures. When a light beam is applied as logic '1' at input A, its phase must be 0° so that a destructive interference can occur between the light input beam and the reference input beam to provide a very low intensity as logic '0' output. Both the corner rods of T-junction, r_{j1} and r_{j2} have their own significance in the operational behavior of the structure. The radius of the rod r_{j1} controls back reflection into the unemployed input port i.e., port A when input is '0'. This rod is basically helpful for logic gates with two or more inputs. But in the proposed NOT gate its radius is set to normal value (i.e., $0.2a$), as the unwanted reflection is very less at this value. The junction rod r_{j2} is a key rod in this design to provide a light intensity signal at the output when input is not applied. This light intensity is considered to be logic '1'. This rod is made with an impure flint glass material with refractive index of 1.92. This glass material allows the light to move towards the output side. The impure flint glass material possesses a typical range of refractive index from 1.523 to 1.925. Lower the refractive index value of the rod r_{j2}, lower the output contrast ratio of the gate. So, the refractive index of the edge rod r_{j2} is set to 1.92 in order to have a high output contrast ratio. Thus, in the proposed NOT gate when input light is not applied (i.e., when A = 0), the edge rod r_{j2}

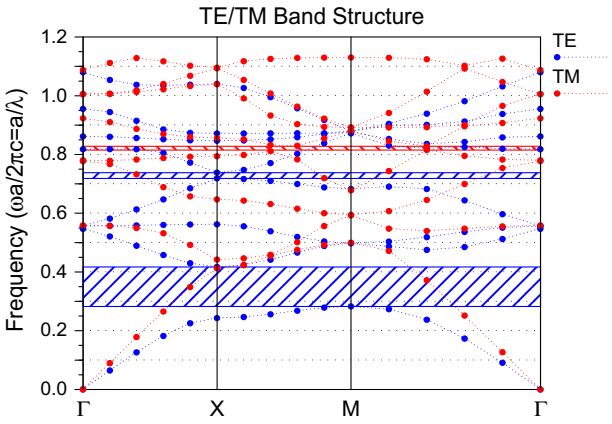

Fig. 2 Band diagram of the uniform PhC structure (*red dotted line*—TM mode, *blue dotted line*—TE mode). (Color figure online)

will allow the reference input light to pass towards the output port which is considered as logic '1'.

3.2 Results and discussion

In these type of structures, the reference input power is same as that of the applied input power unlike the structure proposed in (Wu et al. 2012). A power of 1 mW is taken at both

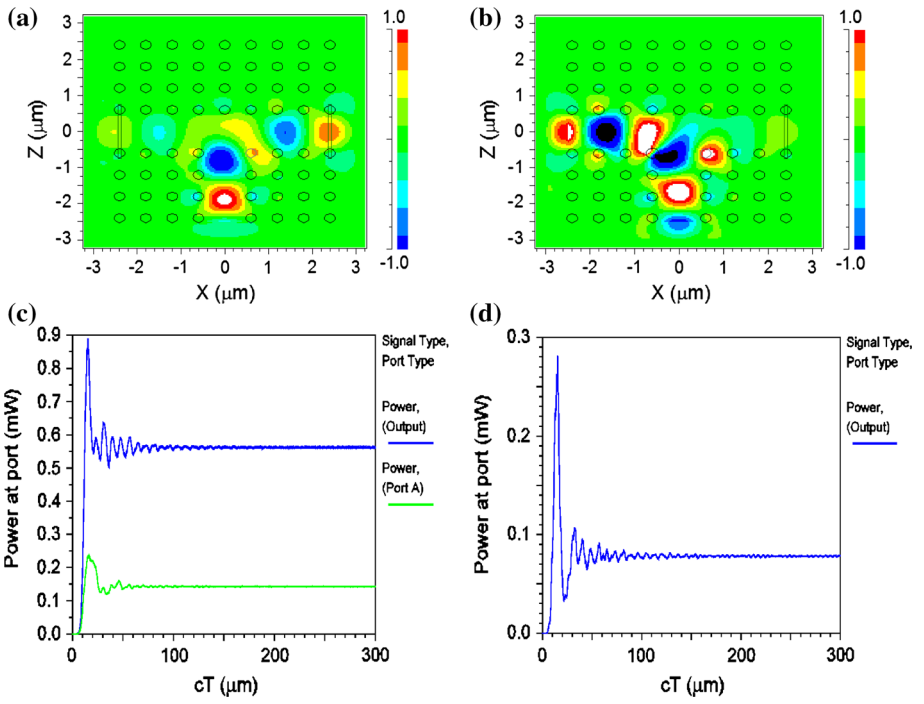

Fig. 3 Optical field pattern of NOT gate for **a** logic 1 output and **b** logic 0 output and power level of NOT gate at the output port and the unemployed input port for **c** logic 1 output and **d** logic 0 output

input ports (*A* and reference input). We assume 1 mW of input light power as a reference power P_a. When no light beam is applied to the input port, means $A = 0$, the light beam from the reference input port reaches the output port. The power obtained at the output port is 0.564 P_a. This is the value of logic '1' obtained at the output port. When the input is applied, means $A = 1$, this input beam is destructively interfered with the reference input beam and a very low power is obtained at the output port. The power obtained at the output port is 0.078 P_a which can be considered as logic '0'. The optical field pattern of the proposed NOT gate structure for both the input logic values and their power level at the respective ports is illustrated in Fig. 3. As illustrated by Fig. 3a, the reference input power reaches the output port when A = 0 and it is due to the edge rod r_{j2}. It can also be observed that a less amount of reference power is reflected into the input port when A = 0 and this is due to the rod r_{j1}. In the figures Fig. 3c, d, the blue colored plot indicates the power obtained at the output port while the green colored plot indicates the power reflected back into the unemployed input port i.e., when $A = 0$. Normally, for both the output states '0' and '1', there would be some unwanted outgoing waves pass into the input and the reference ports which will become harmful to the stability of the system (Wu et al. 2012). The ON to OFF contrast ratio (CR) of the all-optical logic gate can be obtained as follows,

$$\mathrm{CR} = 10log\frac{P_1}{P_0} \tag{1}$$

where P_1 and P_0 are the output power levels for logic '1' and '0', respectively. From this, the contrast ratio of the proposed NOT gate is 8.59 dB. The power level at the output port reaches to 0.564 P_a at $cT = 88$ μm, when $A = 0$. So, the response time of the NOT gate is 0.29 ps for zero input. Similarly, the power level at the output port reaches to 0.078 P_a at $cT = 106$ μm, when $A = 1$. So, the response time of the NOT gate is 0.35 ps for the input applied. Thus, the maximum response time of the NOT gate is 0.35 ps which is slightly better than the cross structure based NOT gate (Wu et al. 2012) and far better than the resonance based NOT gate (Ghadrdan and Mansouri-Birjandi 2013b). The response time of the NOT gate reported by Wu et al. (2012) is 0.464 ps whereas the response time of the NOT gate reported by Ghadrdan and Mansouri-Birjandi (2013b) is 0.84 ps.

The amount of light reflected back into the input port when input is not applied is <0.15 P_a. It may be the least amount of the light reflected back into the unemployed input port compared to the NOT gate reported in (Wu et al. 2012). The simulation results of the NOT gate in (Wu et al. 2012) shows that the reflected power is nearly same as that of the power which reaches the output port where as the proposed NOT gate will reflect only 15 % of the reference input. The size of the proposed NOT gate is very less with 5.04 μm × 5.04 μm dimension compared to the resonance based NOT gate (Ghadrdan and Mansouri-Birjandi 2013b) with 12 μm × 12 μm dimension. Its size is also too small when compared to the interference based NOT gate proposed by Yulan el al (2013). Finally, it can be concluded that the proposed NOT is better in terms of response time and size though the contrast ratio is less.

4 Dual T-shaped photonic crystal waveguide as NOR/XNOR/NAND gate

A NOR/XNOR/NAND gate can be designed using the same T-shaped structure with two vertical waveguides deviated by a value of 5*a* as shown in Fig. 4. The same structure can act as a NOR gate or an XNOR gate or a NAND gate, but with different phase values of the

input light beam. Ports A and B are applied with the input light signals, whereas the reference input signal is applied to the second vertical waveguide.

4.1 Operating principle

The rods r_{j1}, r_{j2} and r_{j3} are the key in the reduction of back reflection into the unemployed input ports and the operational behavior of the structure. Optimization of the rod r_{j1} will keep low back reflection into the unemployed input ports. The rods r_{j2} and r_{j3} are made up of impure flint glass material with refractive index 1.92, so that the light beam from the reference input can move towards the output port at zero input as well as a good interference can occur in between the light beams from port A or port B and reference input port. This value of refractive index will keep high contrast ratio as it was explained in the previous section.

The type of the logical function being performed by the structure is determined by the phase of the input beam applied as logic '1'. At the first T-junction, constructive interference occurs when the two applied input beams are differed by 0° phase, while a destructive interference occurs at a phase difference of 180° between the input beams. At the second T-junction, the interference pattern is inverse which means that constructive interference occurs at a phase difference of 180° between the two input light beams and the destructive interference occurs at 0° phase difference between the two input light beams. This change in the interference pattern at both the T-junctions and the required logical function will determine the phase of the input light beam at ports A and B. We consider the phase of the reference input as 180° to change the input light beam phases logically and comfortably.

At both the T-junctions, the change in the interference pattern occurs due to the path difference between the input light beams. At the first T-junction, the path lengths of the light beam from the ports A and B are same. Thus, constructive interference occurs at 0° phase difference and destructive interference occurs at 180° phase difference as there is no path difference between two input beams. The path length of the input light beams and their path difference can be observed from Fig. 4. The character L indicates the path length of the light beam from the input port to the respective T-junction. L_2 and L_3 are the path lengths from the input port A and B, respectively to the first T-junction. L_5 is the path

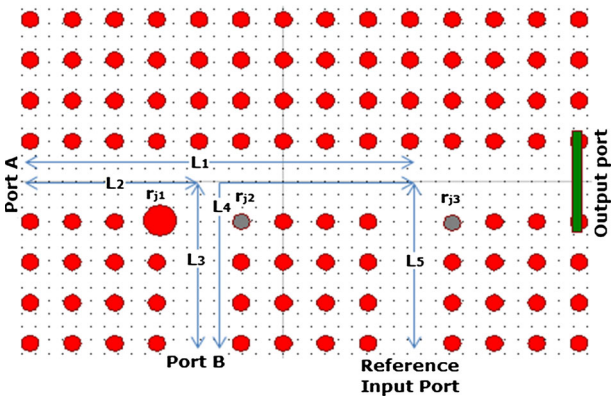

Fig. 4 Structure of the proposed NOR/XNOR/NAND gate

length from reference input port to the second T-junction. These three path lengths are same with value

$$L_2 = L_3 = L_5 = 4a. \tag{2}$$

We consider the path lengths in terms of lattice constant a from the center of the first rod of the respective port to the center of the T-junction. The Path lengths of the input light beam from the ports A and B to the second T-junction are L_1 and L_4, respectively with value

$$L_1 = L_4 = 9a \tag{3}$$

The path difference between the input light beam and the reference input beam at the second T-junction is

$$L_1 - L_5 = L_4 - L_5 = 5a \tag{4}$$

This path difference will create invertible interference pattern at the second T-junction than the pattern that happens at the first T-junction. Constructive interference occurs at a phase difference of 180° between the input beams and destructive interference at a phase difference of 0°. The interference pattern at both the T-junctions will be helpful in determining the phase of the input light beam which is considered to be logic '1'. As the phase of the reference light beam is maintained at 180°, the phase of the light beam applying at port A and/or port B is determined such that the constructive or destructive interference can occur. The phase of input light beam from port A and/or port B for NOR, XNOR and NAND logical functions is shown in Table 1. In the proposed logic gates, the intensity of the input light beam defines the type of the logic value. A light with zero or negligible intensity is considered as logic '0' and a light with high intensity is considered as logic '1'. In the proposed gates, zero light intensity is considered as logic '0'. The phase value of the input light beam is determined in order to create a required type of the interference pattern to obtain a required output. Thus, in the proposed XNOR and NAND gates, the logic '1' has different values of phase for different input combinations as they are not representing the type of the logic input.

The last input combination needs to have light beam at both the input ports A and B. The phases of these light beams are taken such that a constructive interference can happen at the first T-junction. Moreover, the size of the proposed structure is small with 8.04 μm × 5.04 μm dimension.

Table 1 Possible input combinations, required phase values of logic '1' input for NOR, XNOR and NAND logic gates with output logic values

Input combinations		NOR gate			XNOR gate			NAND gate		
A	B	A	B	Output	A	B	Output	A	B	Output
0	0	–	–	1	–	–	1	–	–	1
0	1	–	180°	0	–	180°	0	–	0°	1
1	0	180°	–	0	180°	–	0	0°	–	1
1	1	180°	180°	0	0°	0°	1	180°	180°	0

4.2 Optimization of the radius of the junction rod r_{j1} of the first T-shape waveguide

The normal size of the junction rod r_{j1} allows the unwanted light signals to pass into the unemployed input ports. We optimized the size of r_{j1} such that the reflection into the unemployed input ports is less with good ON to OFF contrast ratio. We calculated the minimum ON to OFF contrast ratio for optimization purpose and it is based on the minimum value of the acquired output power level P_1 considered as logic '1' and the maximum value of the acquired output power level P_0 considered as logic '0'. The maximum ON to OFF contrast ratio of any logic gate can also be calculated based on the maximum value of the acquired output power level P_1 considered as logic '1' and the minimum value of the acquired output power level P_0 considered as logic '0'. As the output of NOR and XNOR gate is common except for the input combination '11', the minimum ON to OFF contrast ratio is same for both. The effect of the radius of edge rod r_{j1} on the contrast ratio is illustrated in Fig. 5 which shows that a high contrast ratio can be obtained at $r = 0.26a$ for NAND/NOR/XNOR gate. But this high contrast ratio is obtained at a cost of high unwanted reflection into the unemployed input ports which is unacceptable. Furthermore, a high contrast ratio can also be achieved at $r = 0.4a$, which allows less unwanted reflection into the unemployed input ports. At this radius of r_{j1}, the unwanted reflection is <0.1 P_a in NOR and XNOR gate while the reflection is <0.14 P_a in NAND gate. So, the radius of the edge rod r_{j1} is maintained at $0.4a$ to get high contrast ratio with low unwanted reflection.

The logical operation of this structure for NOR and XNOR functions differ only by input combination '11', whereas NOR and NAND functions differ by two input combinations '01' and '10'. These differences can be made by changing the phase of the input light beams which are considered as logic '1'.

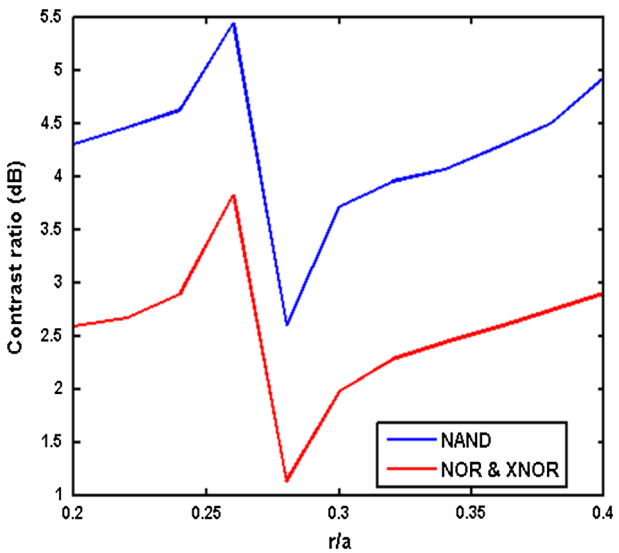

Fig. 5 Plot of *r/a* versus contrast ratio for NOR, XNOR and NAND gates

4.3 Results and discussion for NOR gate

The three input combinations '01', '10' and '11' need to have destructive interference at the second T-junction so as to produce logic '0' output. In accordance with that, the input phases are applied. The optical field pattern for all the four input combinations are shown in Fig. 6. The corresponding output power levels are shown in Fig. 7. At '00' input combination, no input light beam is applied at the ports A and B. Only the reference input will get diverted to the output port and hence it will act as logic '1'. The glass material used for the rod r_{j2} will allow the reference input light to get diverted to output with less power imparted to the unemployed input ports A and B. The output power obtained is 0.795 P_a. The time it takes to reach the output power level is $cT = 96$ μm and the response time is 0.32 ps. For '01' input combination, the power level at the output port reaches to 0.405 P_a after $cT = 103$ μm which is considered to be logic '0'. The response time for this input combination is 0.343 ps. Similarly, for the remaining input combinations '10' and '11', the power level at the output port reaches to 0.407 P_a after $cT = 0.79$ μm and 0.255 P_a after $cT = 0.56$ μm, respectively. The response time for these combinations is 0.26 and 0.19 ps, respectively. So, the response time of the proposed NOR gate is considered as 0.343 ps.

The response time of the proposed NOR gate is far better than the resonance based NOR gate (Andalib and Granpayeh 2009; Isfahani et al. 2009). The reported response time values of these NOR gates are 7.2 ps (Andalib and Granpayeh 2009) and 3 ps (Isfahani et al. 2009). To the best of our knowledge, this is the first NOR that has ever been designed

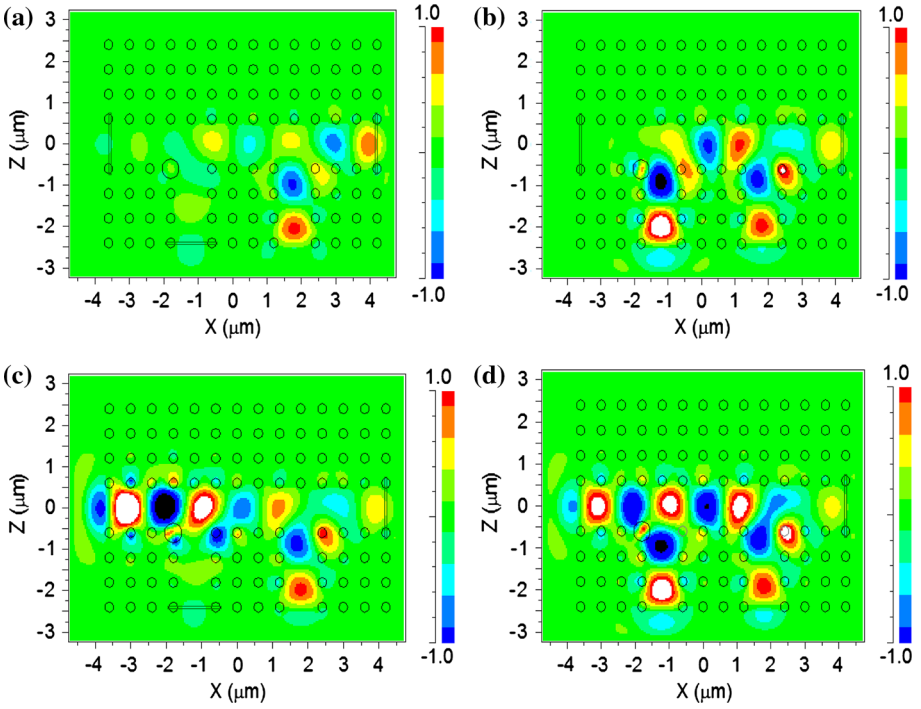

Fig. 6 Optical field pattern of NOR gate for input combinations **a** 00, **b** 01, **c** 10 and **d** 11

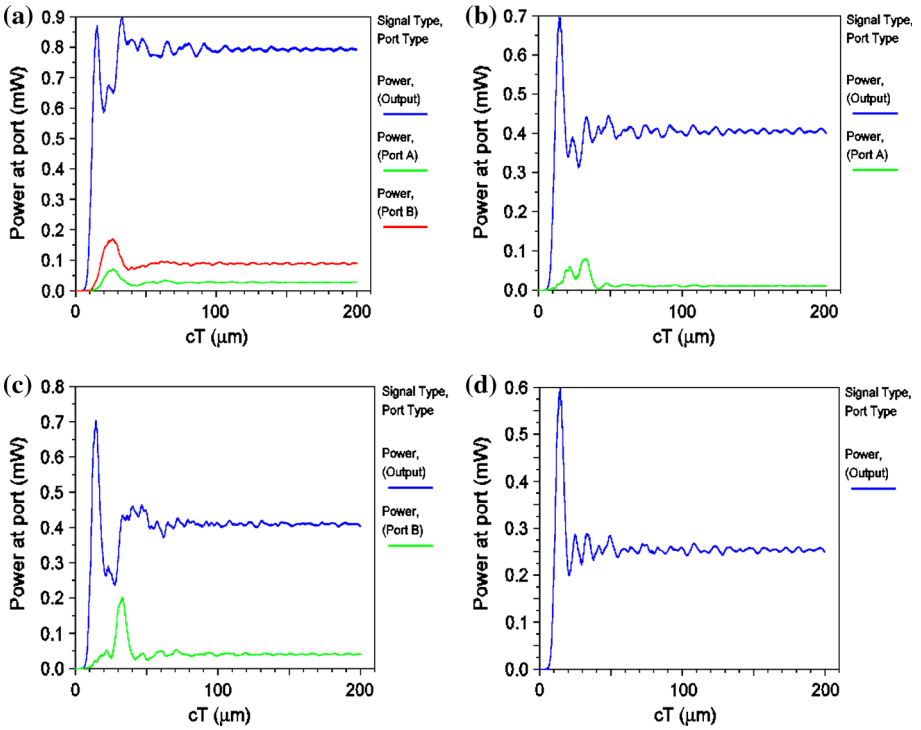

Fig. 7 Power level of NOR gate at the output port and the unemployed input ports for the input combinations **a** 00, **b** 01, **c** 10 and **d** 11

by using interference phenomenon with a fast response time and also with a reference input.

The minimum contrast ratio can be obtained between the output power levels obtained due to the input combinations '00' and '10'. The value of minimum contrast ratio is 2.91 dB. As the output power level of the logic '0' varies from one input combination to the other, the contrast ratio also varies among the input combinations. The maximum value of the contrast ratio can be obtained in between the input combinations '00' and '11' and its value is 4.94 dB. This contrast ratio analysis is specific for our proposed NOR gate. Generally, for a particular design, the contrast ratio analysis depends upon the values of the output power levels obtained for different input combinations. It can also be observed that the unwanted reflection into the unemployed input ports is $<0.1\ P_a$. It became possible with the radius of the junction rod $r_{j1} = 0.4a$. This reduction of unwanted reflection into the unemployed input ports will improve the operational performance of the logic gate. Reflection into the input applied ports also need to be reduced to further improve the overall performance of the logic gate. The size of the proposed NOR gate is also very low compared to the resonance based NOR gate (Andalib and Granpayeh 2009; Isfahani et al. 2009). Although the ON to OFF contrast ratio of the proposed NOR gate is less, its performance is far better in terms of response time, size and reduction of unwanted reflection.

4.4 Results and discussion for XNOR gate

The XNOR gate performs similar to the NOR gate except for the input combination '11'. The optical field pattern, output power level as well as the response time for the input combinations '00', '01' and '10' are similar to the NOR gate. For the input combination '11', the constructive interference is to happen at the second T-junction. So, the phases of the input light beam are 0°. As the constructive interference occurs at the second junction, the power level obtained at the output is high. In this case, it is 1.9 P_a as shown in Fig. 8. The output reaches to this level at $cT = 98$ μm and the response time for this input combination is 0.33 ps. According to the response time analysis, the response time of XNOR gate can be considered as 0.343 ps.

The minimum ON to OFF contrast ratio can be obtained in between power levels of input combinations '00' and '10' and whose value is 2.91 dB. Similarly, the maximum ON to OFF contrast ratio can be obtained in between the power levels of input combinations '11' and '01' and the value is 6.71 dB. The size of the proposed XNOR gate is better than the MMI based XNOR gate (Liu et al. 2013). The size of the XNOR gate reported by Liu et al. (2013) is 6.9 μm × 6.7 μm. The proposed XNOR gate is also small compared to the interference based XNOR gate with reference input (Yulan et al. 2013).

4.5 Results and discussion for NAND gate

The main difference between the operating principle in NOR and NAND gate is the type of the interference in the input combinations '01' and '10'. In NOR gate, the destructive interference occurs at the second T-junction whereas in the NAND gate, the constructive interference should occur in order to provide logic '1' output. Due to this constructive interference, the output power level is above 1.0 P_a. For the remaining two input combinations '00' and '11', the performance of the NAND gate is same as the proposed NOR gate. The optical field pattern and the output power level for the input combinations '01' and '10' are shown in Fig. 9. For the input combination '01', the output power level reaches to 1.42 P_a at $cT = 88$ μm. The response time of the NAND gate for this combination is 0.29 ps. Similarly, for the input combination '10', the output power level reaches to 1.14 P_a at $cT = 103$ μm with a response time of 0.34 ps.

The minimum ON to OFF contrast ratio can be obtained in between the input combinations '00' and '11' and its value is 4.93 dB. Similarly, the maximum ON to OFF contrast

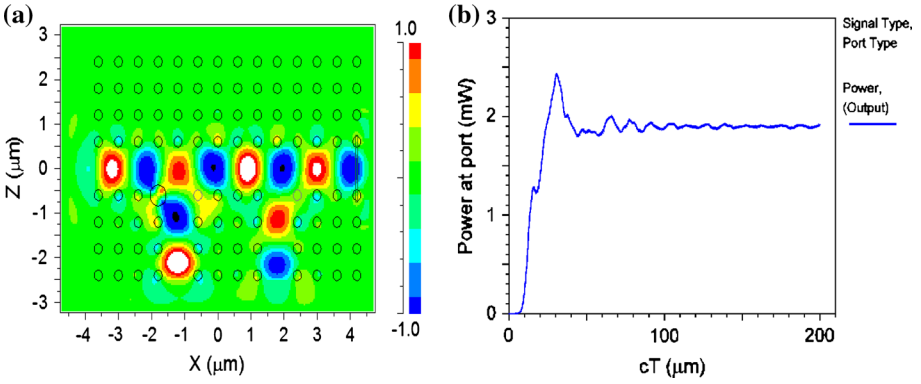

Fig. 8 **a** Optical field pattern and **b** output power level of XNOR gate for the input combination '11'

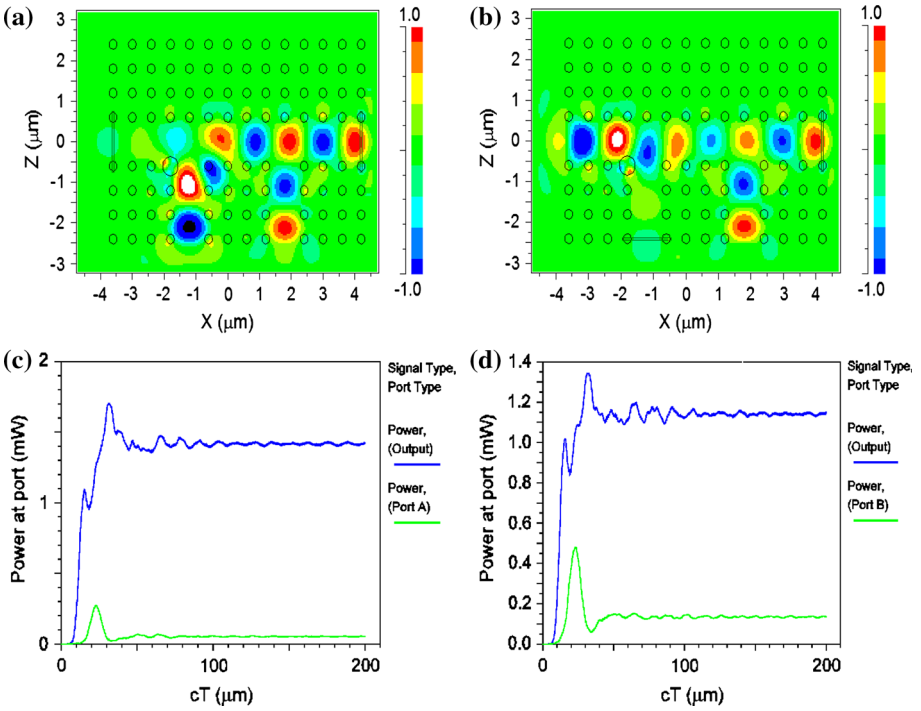

Fig. 9 Optical field pattern of NAND gate for the input combinations **a** 01 and **b** 10 and power level of NAND gate at the output port and the unemployed input ports for the input combinations **c** 01 and **d** 10

ratio can be obtained in between the input combinations '01' and '11' and its value is 7.45 dB. The proposed NAND gate has a very less response time with value even <0.35 ps. The size of the proposed NAND gate is better than the MMI based XNOR gate (Liu et al. 2013) and also the interference based XNOR gate with reference input (Yulan et al. 2013).

Finally, the performance of the proposed logic gates in terms of response time, size and the reduction of unwanted reflection is appreciable although the contrast ratio is less. The fast response time of these logic gates will allow them to be applicable in cascading with other optical devices in high-speed optical communication and networking systems, as these systems need small size optical devices with fast response time. As compared with the logic gates based on other optical methods like SOA in which the operational speed is low due to long response time and also limited by the unavoidable spontaneous emission of noise (Wang et al. 2006, 2007), the proposed logic gates are highly suitable for such high-speed applications.

5 Conclusion

In this paper, a new design of all-optical logic gates have been proposed using T-shaped waveguide in two-dimensional square lattice with Si rods in air. The device performance has been analyzed and simulated by PWE and FDTD methods. The method of operating a T-shaped waveguide as a NOT gate and the performance of a dual T-shaped waveguide as

NOR, XNOR, and NAND gates has been explained. The optimization parameter has been obtained for determining the high contrast ratio with low reflection into unemployed inputs. These logic gates have fast response time with value not more than 0.35 ps. The size of these logic gates is also very small with dimension 5.04 μm × 5.04 μm for NOT gate and 8.04 μm × 5.04 μm for the remaining gates. It is expected that the new proposed designs will help in realizing devices and components for high speed broadband optical communication systems and networks.

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