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Design of an InGaAs/InP 1.55 μm electrically pumped VCSEL

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Abstract The design of an electrically pumped InGaAs quantum well based vertical cavity surface emitting laser (VCSEL) on InP substrate is presented. Such optically pumped VCSELs have already been demonstrated. To design electrically pumped VCSEL, three simulations steps are needed: optical simulation gives access to the standing-wave electric field distribution, to design the active region and the Bragg mirrors. Thermal simulation is helpful to design metallic contacts while the energy band diagram is obtained by electrical simulation to design the buried tunnel junction useful for carrier injection. All these simulations are compared to experiment.

Keywords Electrically pumped VCSEL · Tunnel junction · 1.55 μm · DBR

1 Introduction

Vertical cavity surface emitting lasers (VCSEL) operating at 1.55 μm have been shown to be cost effective light sources for the optical network. They present the opportunity to benefit from an efficient coupling with optical fibers thanks to their circular beam, a spectral purity, and a high modulation bandwidth (typically 2–5 Gb/s; Tayahi et al. 2006). However, highly reflective distributed Bragg reflectors (DBR) lattice-matched to InP present a poor thermal conductivity (Karim 2000). In the present work, we report on 1.55 μm VCSELs with dielectric DBR. Such optically pumped VCSELs (OP-VCSEL) already have been demonstrated (Lamy 2008). The same type of active region and DBR is used to design electrically pumped VCSELs (EP-VCSEL) as shown on Fig. 1. The optical design of the active region and the DBR is presented in part II. Part III contains thermal modeling of optically and electri-

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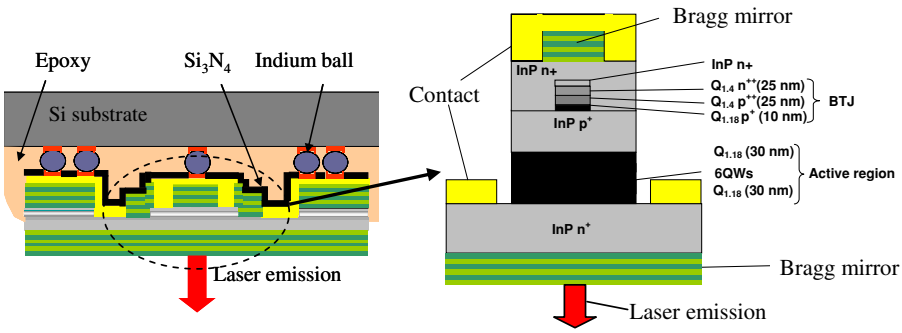

Fig. 1 EP-VCSEL structure

cally pumped devices. The carrier injection is obtained using a buried tunnel junction (BTJ) presented in part IV.

2 Optical design

The optical design objectives consist in reaching a high reflectivity of the DBR and optimizing InP thicknesses to place, respectively, the active region and the BTJ at an anti-node and a node of the standing-wave electric field.

From the optical properties of each layer of the structure (thickness, refractive index, absorption), the algorithm, based on propagations matrices, gives access to the standing-wave electric field, the reflectivity spectrum. The epilayer structure is then optimized to reach monomode VCSEL properties around $\lambda = 1.55\,\mu$m.

The DBRs are realized by magnetron sputtering. The refractive index of the dielectric materials is, respectively, 3.7 and 1.8 for amorphous silicon (a-Si) and amorphous silicon nitride (a-SiN_x). Two ways are envisaged to reach such a reflectivity. A standard DBR is realized using six periods and presents a reflectivity value of 99.5% at $\lambda = 1.55\,\mu$m (Levallois et al. 2005). Thanks to a simulation based on propagations matrices using the refractive indexes of each layer, a hybrid DBR with 3.5 periods and gold layer is shown to have the same reflectivity. Such mirrors have been realized and their reflectivity measured by fourier transform infrared reflexion (FTIR) is in good agreement with simulation results.

The active region, grown by molecular beam epitaxy (MBE), contains six InGaAs (7.2 nm) quantum wells (QW). Lattice matched alloy ($In_{0.8}Ga_{0.2}As_{0.435}P_{0.565}$ named $Q_{1.18}$ because its gap corresponds to $\lambda = 1.18\,\mu$m) is used as a barrier (10 nm). The buried tunnel junction is realized in another strongly doped ($N_D = N_A = 5 \times 10^{19}\,cm^{-3}$) lattice matched InGaAsP alloy named $Q_{1.4}$ ($In_{0.66}Ga_{0.34}As_{0.732}P_{0.268}$). This alloy has been chosen for its small gap to enhance tunneling properties and avoiding absorption at $\lambda = 1.55\,\mu$m. As shown on Fig. 2, the active region and BTJ positions are optimized adjusting InP thicknesses. The calculated reflectivity for this structure give a free spectral range of 170 nm: a longitudinal monomode laser emission of the VCSEL is thus expected.

3 Thermal analysis

Heat dissipation is an important problem in VCSELs due to the small active region compared to edge lasers (Osinski and Nakwaski 1995) and the use of DBR with poor thermal

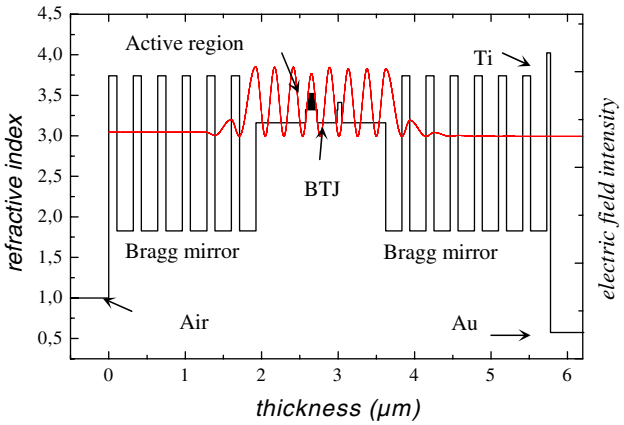

Fig. 2 Standing-wave electric field distribution in the structure

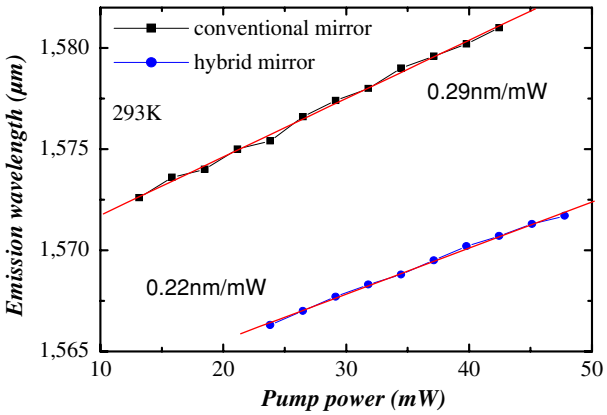

Fig. 3 Wavelength shift as a function of pump power for OP-VCSELs with conventional or hybrid DBR. Simulation (full line) is in good agreement with experiment (*squares* and *circles*)

conductivities. The aim of thermal analysis is to design the metallic contacts and the epilayer structure to enhance thermal conductivity. A two-dimension (with revolution symmetry) finite element model has been used to model OP- and EP-VCSELs. For OP-VCSEL, two optical structures have been fabricated, using standard and hybrid DBR. These two kinds of VCSEL are bonded on silicon substrate thanks to a method employing a gold-indium alloy (Levallois et al. 2005). These devices have showed a laser emission in continuous-wave operation at room-temperature and their wavelength shifts have been measured as a function of pump power as shown on Fig. 3. Considering that cavity is mainly constitute of InP, its refractive index change of $2 \times 10^{-4}\,\mathrm{K}^{-1}$(Martin et al. 1995) implies a calculated thermal shift of $0.1\,\mathrm{nm\,K}^{-1}$, thus the VCSEL thermal resistance is evaluated to 2,900 K/W for the standard DBR and 2,200 K/W for the hybrid VCSEL. These values are in good agreement with simulation results.

For EP-VCSEL, the design of the VCSEL is different from optically pumped devices. Here, as for OP-VCSEL, the use of dielectric material for the DBR requires bonding of the devices on a host-substrate. However, for EP-VCSEL, a flip-chip method using indium micro-ball bumping technology is employed (Bernabé et al. 2005). Indium balls allow to bond devices on a silicon substrate and they ensure also the current injection.

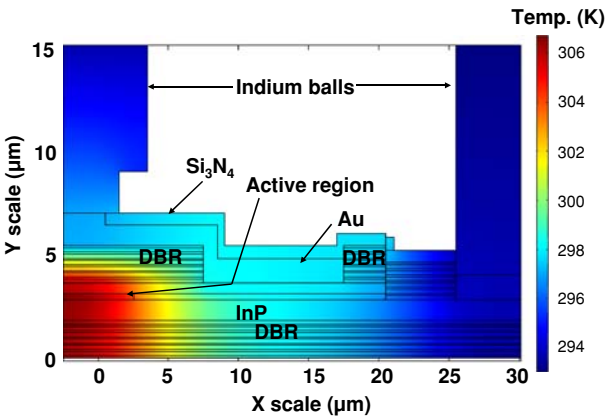

Fig. 4 EP-VCSEL 2D thermal simulation

The final device structure and the gradient temperature inside it are presented in Fig. 4 when 10 mW is absorbed by the active region. As for OP-VCSEL, an active region with a diameter of 10 µm is considered. The thermal conductivities used in the simulation are the following 2.6 $W\,m^{-1}\,K^{-1}$ for the a-Si (Goldsmid et al. 1983), 5.5 $W\,m^{-1}\,K^{-1}$ for the a-SiNx (Park et al. 2006) and 6 $W\,m^{-1}\,K^{-1}$ for the $Q_{1.18}$ (Adachi 1992). The silicon temperature is considered constant at room temperature and the convection between the bottom DBR and the air is neglected. For such a device, the 2D finite element model gives a thermal resistance of 1,500 K/W which is lower than the hybrid OP-VCSEL. As it can be observed in Fig. 4, the heat produce in the active region can be conducted through the electrical contacts toward the silicon substrate, via the indium ball. This new way allows enhancing the thermal characteristics of our devices. The thermal resistance can be also decreased with the use of a thick InP layer, located close to the bottom DBR. The thickness influence of this layer on the thermal resistance has been simulated. A thick InP layer has a beneficial effect on the thermal resistance. However, the total InP thickness has to be maintained lower than 3 µm in order to achieve a free spectral range higher than 50 nm to ensure a longitudinal monomode laser emission. For such InP thickness, the thermal resistance is close to 1,100 K/W.

4 Buried tunnel junction

In EP-VCSELs, the BTJ allows carrier and optical confinement in the active region. To fabricate the VCSEL structure shown in Fig. 1, a first MBE growth is performed until the $Q_{1.4}$ layer, followed by the $Q_{1.4}$ mesa chemical etching (a 15 nm InP layer is over-etched to ensure the current confinement). The final structure is obtained after a re-growth of 380 nm of InP. The optical confinement is ensured by the refractive index difference between the InP and the $Q_{1.4}$ and also by the thickness difference obtained by the conservation of the mesa after the MBE regrowth. A transversal monomode emission should be obtained with a diameter <10 µm. A self-consistent 1D Schrödinger-Poisson algorithm is used to verify the tunnel effect in the reverse BTJ and to avoid current leakage in the reverse InP junction outside the BTJ. If the depletion region is too large and reaches the laser active region, electrical injection is no more confined. Figure 5 presents the bias voltage band diagrams obtained inside and outside the BTJ for two InP p+ thicknesses.

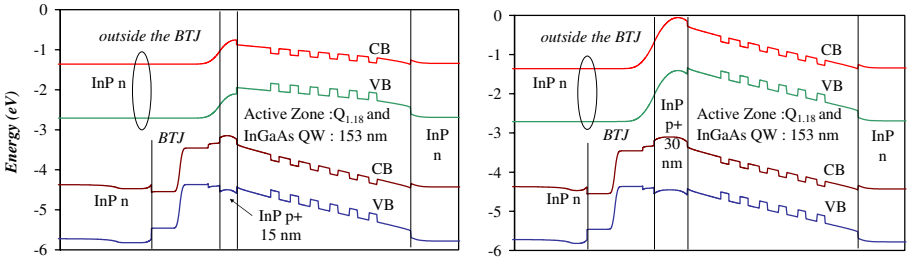

Fig. 5 Simulation of the band diagram of the VCSEL in vertical direction, inside and outside the BTJ for different InP p+ thicknesses: 15 nm on the left, 30 nm on the right

The simulated structure corresponds to Fig. 1. Inside the BTJ, $Q_{1.4}$ doping level is almost $N_D = N_A = 5 \times 10^{19}\,cm^{-3}$, which allows a great tunnel effect verified experimentally by I(V) characteristics. Simulation has shown that a voltage variation only modifies injection current in the BTJ and keeps the band slope in the active region constant. Outside the BTJ, the InP p+ layer has to be thick enough so that a reverse polarization of the InP diode does not modify the active region curvature. As the maximum p doping level of InP is $N_A = 2 \times 10^{18}\,cm^{-3}$, Schrödinger-Poisson simulations have shown that the minimum InP p+ thickness is 30 nm. For an InP p+ thickness of 15 nm, the active region band slope is different inside and outside the BTJ. The built-in electric field of the reverse InP junction is therefore supported by the active region and the BTJ cannot play its role of carrier confinement. First electrical measurements of the VCSEL cavities (without the DBR) have been performed on two samples with an InP p+ thickness of 15 and 260 nm. Such a thickness corresponds to the addition of 15 nm and half-wavelength of InP. The first sample presents strong leakage current outside the BTJ while the second one avoids this problem. These first experimental characteristics are consistent with simulation results.

5 Conclusion

To design electrically pumped 1.55 μm VCSELs on InP, three useful steps of simulation have been presented, all consistent with experiment. Optical simulation gives access to the epilayer structure and to the DBR reflectivity. A 2D thermal model gives access to the thermal resistance of the structure and a simple 1D Schrödinger-Poisson calculation allows understanding why the first samples fabricated in the laboratory presented leakage current. An integrated VCSEL model including these three steps of simulation could be useful to improve this VCSEL design provided the results stay consistent with experiment.

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