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ORIGINAL PAPER

Implementation of chaotic circuits with a digital time-delay block

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Abstract In this paper, the implementation of time-delay chaotic circuits is investigated. To implement the time-delay block, a solution based on a digital circuitry has been adopted. This solution leads to a programmable hardware which can be realized by using available field programmable gate arrays. In this paper, issues raised from this implementation such as the behavior of the system with respect to the precision and the sampling rate of the conversion process have been investigated. The synchronization error is proposed as an indicator of the accuracy of the whole implementation.

Keywords Time-delay circuit · Chaos · Chaotic synchronization

1 Introduction

In some electronic circuits delay blocks are intentionally introduced to implement specific functions. For instance, in measurement applications, the highly integrated time-multiplexing device [1], the particle detector [2], and the time analog-to-digital converter [3] make use of time-delay blocks. In radio frequency applications, in high-speed microprocessors or in memories, delay circuits play an important role in delay-locked loop [4] where they allows to enhance the performance of the integrated circuits.

On the other hand, delays are fundamental in many mathematical models of dynamical systems and, in particular, in neuronal models, where synapses are characterized by the presence of delays. Delays are also important in coupled circuits and in networks where their presence can introduce significant changes in the dynamics or may constitute a fundamental element of the model required to account for the dynamics really observed in experiments [5].

The presence of time-delays in nonlinear systems may also induce chaotic oscillations. For instance, chaos has been observed in piecewise linear continuous-time systems described by a simple functional differential equation with only one variable and in the presence of delay [6]. On the opposite, time-delays may also be useful to suppress chaos in the so-called time-delayed feedback control which constitutes an important method of chaos control [7].

In general, time-delay chaotic systems constitute a topic that received considerable attention in literature. For example, phase synchronization in unidirectional coupled Ikeda time-delay systems was studied in [8], whereas the possibility of generating high-dimensional dynamical signals by the Mackey–Glass system has been investigated in [9].

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In such systems, the typical values of the delay may also be relatively large (in the order of magnitude of milliseconds). From these considerations and in view of the circuit implementation of mathematical models of networks, neuron models, and coupled dynamical systems, the need of general strategies for the implementation of relative large delays arises.

To this aim, two main methodologies can be taken into account: analog methods and digital methods. In the former class, the time-delay is implemented by an analog circuit (usually a long chain of elementary blocks) made of resistors, capacitors, inductors, and/or operational amplifiers. An example is the Mackey–Glass circuit proposed in [9] where a tunable delay is obtained with a network of LCL filters with matching resistors at the input and output. Tuning was achieved by connecting the output amplifier to a certain output terminal. In [10], a delay line is employed to obtain an electronic chaotic circuit. The use of delay units based on operational amplifiers is discussed in [11]. However, one of the disadvantages of these approaches is that they require a large number of components. Furthermore, the design or the parameters of the circuit have to be changed if other values of the delay should be implemented.

In order to overcome the drawbacks of analog methods, a few papers have explored digital approaches for the implementation of relatively small time-delays (in the order of magnitude of nanoseconds), e.g., [1, 2, 12].

The aim of this paper is to investigate the use of time-delay digital blocks for the implementation of chaotic circuits. The effects of some parameters such as the sampling time and the number of bits used in the converters are also investigated.

The paper is organized as follows. In Sect. 2, a general scheme of chaotic circuits with a time-delay digital block is described. Section 3 describes the implementation of the time-delay digital block. An example of implementation based on Field Programmable Gate Arrays (FPGA) is proposed in Sect. 4. Section 5 shows the experimental results. Finally, Sect. 6 concludes the paper.

2 Design of chaotic circuits with digital time-delay blocks

The scheme adopted in this paper is a simple one with only three blocks connected into a feedback configuration, and is described by the following delay differential equation:

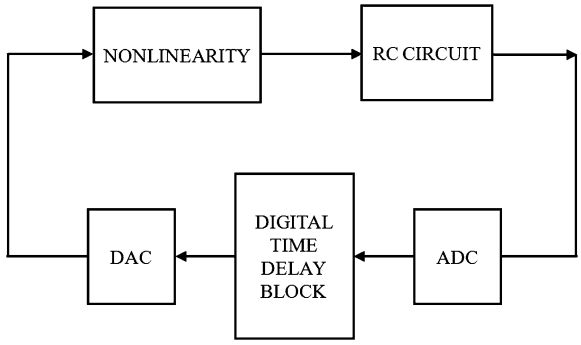

Fig. 1 Block scheme of the time-delay chaotic oscillator with a digital time-delay block

$$\dot{x} = f\big(x, x(t-\tau)\big) \tag{1}$$

where τ is the time-delay. An example of chaotic circuits described by (1) is the Ikeda system [13]. Other examples of time-delay chaotic systems can be found in [7].

The model consists of a nonlinearity, an RC circuit and a time-delay block. Despite its simplicity, it contains all the elements needed to generate chaos, as it will be shown in the following. The effective possibility to generate chaotic behavior depends on the particular nonlinearity used and can be studied by following the approach depicted in [20]. In the particular example considered in Sect. 4, a piecewise linear (PWL) nonlinearity has been used.

From the point of view of the physical realization, the time-delay block implementation is not trivial, because of the typical values of the time-delay used in such chaotic circuits (order of magnitude of milliseconds). In this paper, a digital approach is pursued for the realization of this block.

In the perspective of this approach, the scheme adopted in this paper can be represented as in Fig. 1 where an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC) interfacing the time-delay digital block with the remaining (analog) part of the circuit are included. The analog signal is transformed into a digital one by the ADC, then the digital signal from the ADC is delayed in the time-delay block before being fed through the DAC to the remaining part of the circuit. A delayed analog signal is ob-

tained at the output of the DAC. The signal is delayed by a quantity given by:

$$T_{\text{delay}} = T_{\text{ADC}} + T_d + T_{\text{DAC}} \tag{2}$$

where T_{ADC}, T_d and T_{DAC} are the delay of the ADC, the delay of the digital time-delay block and that of the DAC, respectively. The total delay can be approximated as $T_{\text{delay}} \simeq T_d$ when $T_{\text{ADC}}, T_{\text{DAC}} \ll T_d$.

The analog to digital conversion introduces some error sources whose effects are also investigated in this paper. In particular, the effects of the sampling rate and of the number of bits used in the conversion process have been studied, in order to obtain indications on how to select the DAC and ADC devices in the implementation stage.

In order to evaluate the effects of these parameters on the whole dynamics implemented, an indicator of how accurate is the whole implementation with respect to the target dynamics should be defined. For this purpose, synchronization has been used.

Synchronization of chaos [14] refers to a process in which chaotic systems adjust a given property of their motion to a common behavior. Since Pecora and Carroll [15] showed that two chaotic systems can be synchronized, chaotic synchronization has attracted considerable interest in various fields. For instance, the application of the chaotic synchronization have been proved in chaotically encrypted secure signal transmission [16] where the transmitted information signal can be retrieved if synchronization between chaotic transmitter and chaotic receiver occurs.

In general, the synchronization error grows up in the presence of parametric or structural differences, so that taking also into account that the target dynamics is chaotic, the synchronization error between the circuit with a digital time-delay and the circuit with an analog time-delay can be used to evaluate the effects of the parameters of the conversion process.

3 Digital implementation of the time-delay block

A discrete-time system with transfer function $H(z) = z^{-k}$ represents an ideal delay. Since the output corresponding to a generic input $f(nT_s)$ is $f((n-k)T_s)$, the ideal delay introduced by such block is $T_d = kT_s$, where T_s is the sampling time. The transfer function of this ideal time-delay block can be rewritten as

$$H(z) = z^{-k} = \prod_i z^{-1} \tag{3}$$

so that the ideal time-delay block can be viewed as the series of k identical blocks, each introducing a time-delay equal to the sampling time. In discrete-time systems, the problem of implementing a generic time-delay block is thus solved by taking into account a block characterized by a time-delay equal to T_s and using a number of such blocks in cascade. To this aim, different solutions can be considered.

For small time-delays, the intrinsic delay of Boolean standard gates such as the NOT gate [1, 12] can be exploited. If the intrinsic delay associated with each gate τ_{gate} is supposed equal for each gates, the total delay of N gates in cascade is approximately equal to

$$T_{\text{delay}} = \sum_{i=1}^{N} \tau_{\text{gate\_}i} = N\tau_{\text{gate}}. \tag{4}$$

The number of gates is a variable parameter to get the desired time-delay since τ_{gate}, which depends on the fabrication process, is constant. This approach is appropriate for small time-delays because the typical values of τ_{gate} are in the order of magnitude of picoseconds.

Since in the case under investigation, larger time-delays are needed, another approach has been here introduced and applied later to the circuit implementation. Since the output of a D flip-flop holds the value of the input until the next change of the clock, this device can be considered a block with a time-delay equal to the clock duration T_{clk}. A shift register made of N D flip-flops has been used in our approach. On each rising edge of the clock, a new bit is shifted in from the input and all the subsequent contents are shifted forward. The last bit in the shift register is available at the output. According to the configuration of the shift register, there are two parameters controlling the time-delay: the clock duration T_{clk} and the number of shifted bits N_{shift}. The time-delay introduced by a shift register is given by:

$$T_{\text{delay}} = T_{\text{clk}} N_{\text{shift}}. \tag{5}$$

Figure 2 illustrates the flexibility of this approach. Time delay can changes from microseconds to mil-

liseconds when keeping constant the number of shifted bits while changing the clock frequency and viceversa.

An advantage of this digital implementation, compared to analog approach for delay implementation, is the possibility to use available programmable hardware to realize the desired configuration and to change its parameters on-the-fly. In the following, we describe one of such implementations, in particular based on an FPGA, and show its suitability for the implementation of chaotic circuits. We then investigate the effects of the conversion process parameters on the implementation.

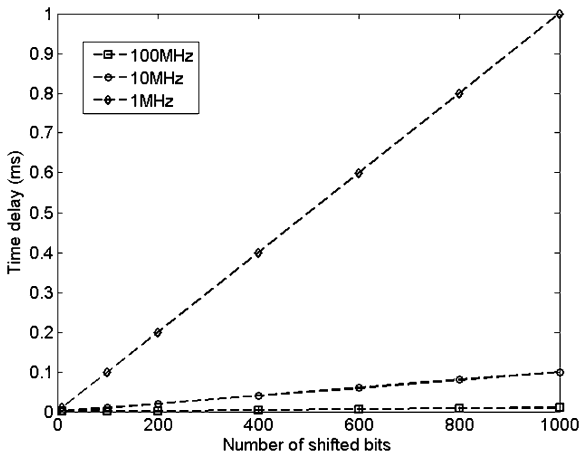

Fig. 2 Time-delay introduced by the shift register in the FPGA versus the number of bits of the register

4 FPGA-based implementation

4.1 Implementation of the time-delay

High performance FPGAs containing millions of gates are currently available in the market [18]. FPGAs can be used in almost all applications including communications, digital signal processing applications or systems on chip, because of their advanced features such as embedded microprocessor and digital signal processing cores. An FPGA can be quickly configured to the desired application so that it is very convenient for the research and prototypal development phase. For these reasons, in this paper for the implementation of the time-delay block, an FPGA has been chosen. In this section, the details of the implementation of the time-delay block are outlined.

The scheme of the time-delay block implemented in the FPGA is illustrated in Fig. 3. It consists of one multiplexer and nine time-delay subcircuits connected in cascade (including one subblock implementing a delay of 1 ms, one subblock implementing a delay of 0.4 ms and seven identical subblocks implementing a delay of 0.2 ms). The time-delay subcircuits utilize shift register configurations as described in Sect. 3. The subcircuits are connected to the multiplexer so that a total delay in the range from 1.4 ms to 2.8 ms can be set. The tuning of the time-delay has been made accessible to the user, by implementing a routine, which thanks to control buttons, allows the

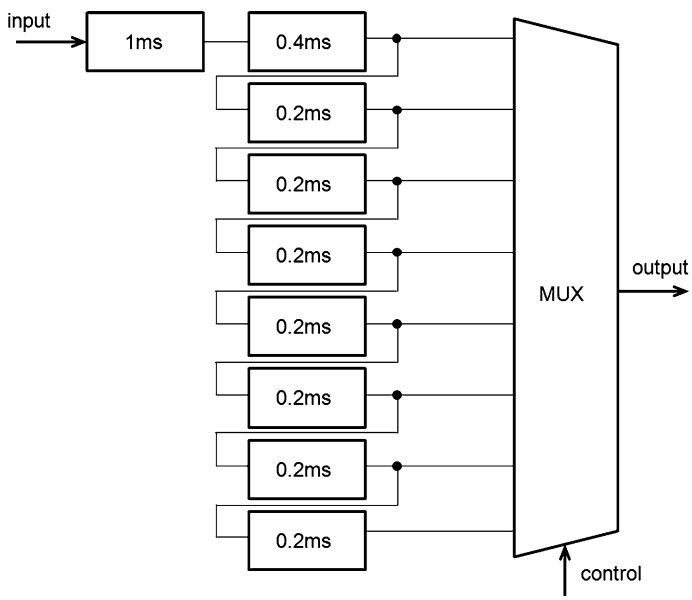

Fig. 3 Block diagram of the time-delay block implemented in the FPGA

user to set the multiplexer parameters, thus selecting the desired time-delay.

The hardware platform used in this work is the ML405 board that is based on the Virtex4 family of FPGAs. The main features of the board are the following: Virtex-4 FPGA XC4VFX20-FF672, 128 MB DDR SDRAM with a 32-bit interface running up to 400 MHz data rate, 100 MHz clock oscillator plus one extra open 3.3 V clock oscillator socket. The delay circuitry prototype has been realized in the Xilinx FPGA chip programmed through a VHDL language. The main resources of Virtex4 used for our application are summarized in Table 1.

4.2 Implementation of the chaotic circuit

In this section, an example of a chaotic circuit obeying (1) is discussed. The chaotic circuit is described by the following state equation [13]:

Table 1 Device utilization summary

Logic utilization	Used	Available	Utilization
Number of Slice Flip Flops	442	17,088	2.62%
Number of 4 input LUTs	73	17,088	0.43%

$$\dot{x} = -ax(t) - b\sin\big(x(t-\tau)\big), \tag{6}$$

where a and b are the parameters and τ is the dimensionless time-delay. Equation (6) represents the dynamics of an optical bistable resonator in which x is the lag of the phase of the electric field across the resonator, b is the laser power intensity injected into the system, and τ is the round trip time of the light in the resonator.

In the following, instead of implementing the sinusoidal nonlinearity appearing in (6), a piecewise linear (PWL) approximation has been used. PWL functions, in fact, have the advantage of ease of implementation [19].

In particular, the following PWL approximation has been used:

$$\sin x \simeq g(x) = \begin{cases} -\frac{2}{\pi}x - 2, & x \in [-\frac{3\pi}{2}; -\frac{\pi}{2}], \\ \frac{2}{\pi}x, & x \in [-\frac{\pi}{2}; \frac{\pi}{2}], \\ -\frac{2}{\pi}x + 2, & x \in [\frac{\pi}{2}; \frac{3\pi}{2}]. \end{cases} \tag{7}$$

The complete schematics of the designed time-delay chaotic circuit including the PWL function (7), the time-delay block implemented with the FPGA approach described in Sect. 4.1 and the RC circuit, is shown in Fig. 4. The circuit makes use of TL084 operational amplifiers (U1A, U2B, U3C, and U4D), eight resistors (from R1 to R8) with 5% tolerance, one capacitor (C1), and the FPGA-based time-delay block.

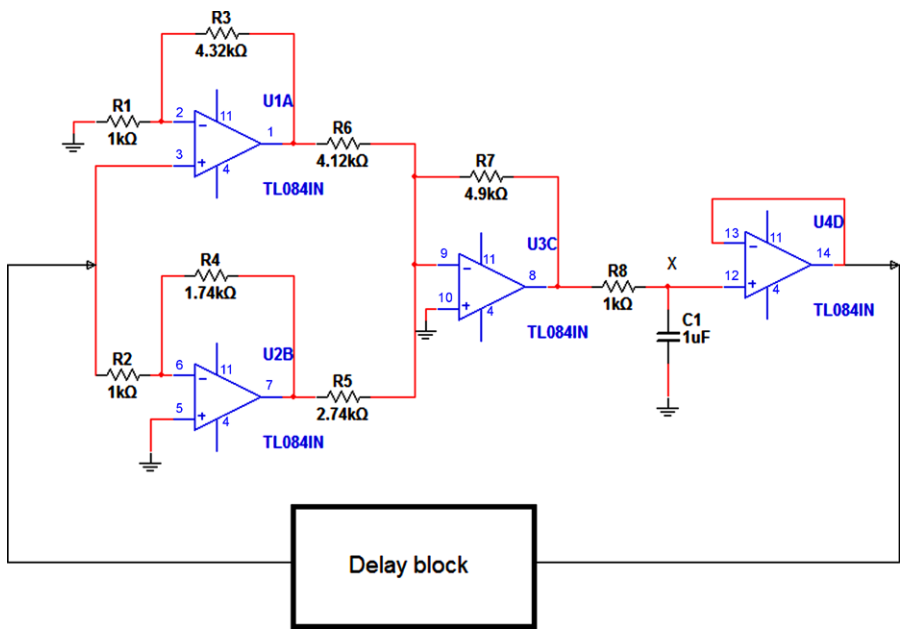

Fig. 4 Electrical scheme of the time-delay chaotic circuit introduced in this paper. The delay block is implemented by means of a FPGA

The first three operational amplifiers are used to build the PWL nonlinearity by letting the operational amplifiers U1A and U2B working in the nonlinear region according to the guidelines described in [19]. The operational amplifier U4D is a buffer. The time-delay block is obtained through the FPGA which implements a time-delay τ given by:

$$\tau = \frac{T_{\text{delay}}}{R_8 C_1},$$

where T_{delay} is tuned through control buttons that set the FPGA multiplexer configuration.

By applying the Kirchhoff's laws and taking into account the parameter values reported in Fig. 4, the following differential equation describing the circuit dynamics can be obtained:

$$\frac{dV_{C_1}}{dt} = -aV_{C_1}(t) - bg\big(V_{C_1}(t-\tau)\big)$$

where $a = 1$, $b = 5$ and V_{C_1} is the voltage across the capacitor C_1.

5 Circuit behavior

The circuit described in the previous section has been realized in laboratory and experimentally investigated. In this section, we briefly discuss the experimental results obtained showing first that chaotic dynamics can be generated, and secondly, the effects of the conversion process parameters on the implemented dynamics.

As discussed in the previous section, the FPGA-based time-delay block can be used to generate a delay ranging from 1.4 ms to 2.8 ms. In the range of τ from 1.6 ms to 2.8 ms, the circuit displays a chaotic regime, as theoretically expected [20]. Figures 5 and 6 show some examples of the waveforms and of the phase portraits experimentally obtained.

These experimental results confirm that the FPGA-based delay block performs effectively for generating chaos. For $\tau \in [1.4\text{ ms}, 1.6\text{ ms}]$, the circuit displays a periodic (limit cycle) behavior. We also notice that large delays in this system lead to instability (in the mathematical model) or saturations (in the real circuit).

As mentioned in Sect. 2, the conversion process affects the accuracy of the implementation. The accuracy of the implementation has been investigated by assuming as a reference model an analog implementation based on Bessel filters and described in [20] and investigating how the synchronization error between the analog implementation and the FPGA-based one is affected by the parameters of the conversion processes (the sampling rate and the number of the bits used).

In particular, an unidirectional coupling scheme [17] has been implemented. The first chaotic system, referred as the master, sends a scalar signal (i.e., the

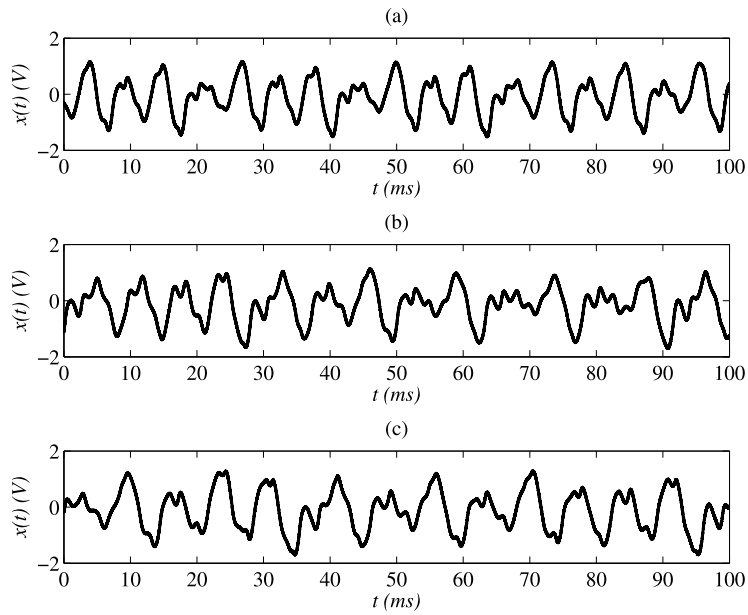

Fig. 5 Waveforms generated by the chaotic circuit of Fig. 4 for different values of the time-delay: (**a**) $\tau = 2.0$ ms; (**b**) $\tau = 2.4$ ms; (**c**) $\tau = 2.8$ ms

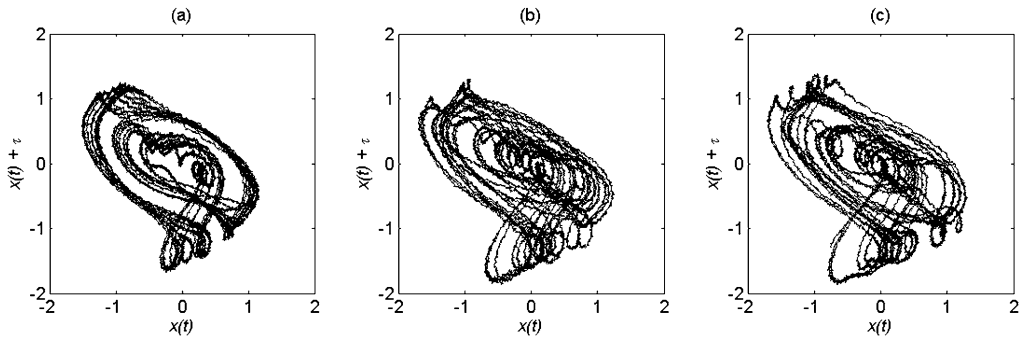

Fig. 6 Phase portraits of the chaotic circuit of Fig. 4 for different values of the time-delay: (**a**) $\tau = 2.0$ ms; (**b**) $\tau = 2.4$ ms; (**c**) $\tau = 2.8$ ms

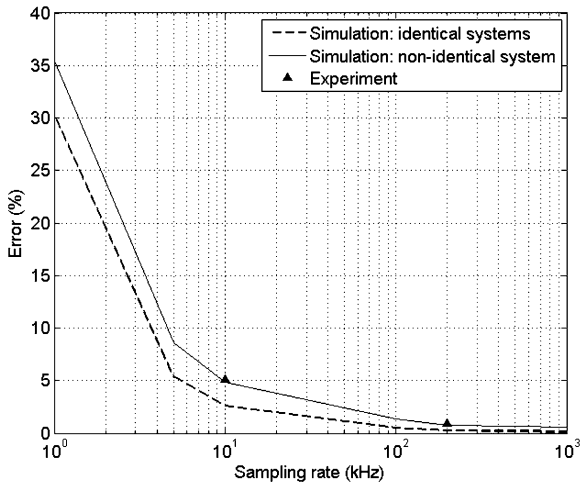

Fig. 7 Numerical results: synchronization error (9) between model with analog time-delay block and model with digital time-delay block versus sampling rate

state variable x) to the second system, referred as the slave. At the slave, the state variables of the two systems are compared and used to build the error signal $e(t) = x_m(t) - x_s(t)$ which is then fed back to the slave, like in an observer. More in detail, the master equation and the slave equation can be written as:

$$\begin{aligned} \dot{x}_m(t) &= -a_m x_m(t) - b_m \sin\big(x_m(t-\tau)\big), \\ \dot{x}_s(t) &= -a_s x_s(t) - b_s \sin\big(x_s(t-\tau)\big) \\ &\quad + K\big(x_m - x_s\big). \end{aligned} \tag{8}$$

The synchronization error has been defined as follows:

$$E = \frac{1}{N}\sum_{i=1}^{N} e(t_i) \tag{9}$$

where $t_1, t_2, \ldots, t_N$ are the sampling times for each time series and N is the total number of samples.

To evaluate how these parameters affect the synchronization error, both numerical simulations with respect to different parameters of the conversion process and experiments in different conditions have been performed. As numerical simulations are concerned, two different cases have been taken into account: identical and nonidentical systems. In the case of identical systems, the parameters appearing in (6) have been fixed equal for the two circuits $a_m = a_s = a = 1$ and $b_m = b_s = b = 5$. In contrast, the case of nonidentical systems, the parameters have been supposed to be affected by a tolerance in the order of magnitude of 5% of the nominal value, i.e., $a_m = a$, $a_s = a(1 \pm 0.05)$, $b_m = b$, and $b_s = b(1 \pm 0.05)$. As it will be shown later, the introduction of the tolerance in the numerical simulations is needed to obtain a good match with the experimental simulations. In fact, the introduced tolerance is in the range of parameter tolerance of the circuit components used.

The results obtained have been reported in Fig. 7 and Fig. 8 showing the synchronization error versus the sampling rate and the number of bits, respectively. Figure 7 indicates that the sampling rate has to be chosen higher than 100 kHz in order to guarantee a low synchronization error. The synchronization error increases significantly when the sampling rate goes under 100 kHz. As regards the number of bits of the conversion process, when it increases, the synchronization error shows small decreases as illustrated in Fig. 8. Therefore, it is not convenient to increase the number of bits beyond 8–10 bits. The synchronization error corresponding to a sampling frequency $f_s = 10$ kHz is always higher than the synchronization error ob-

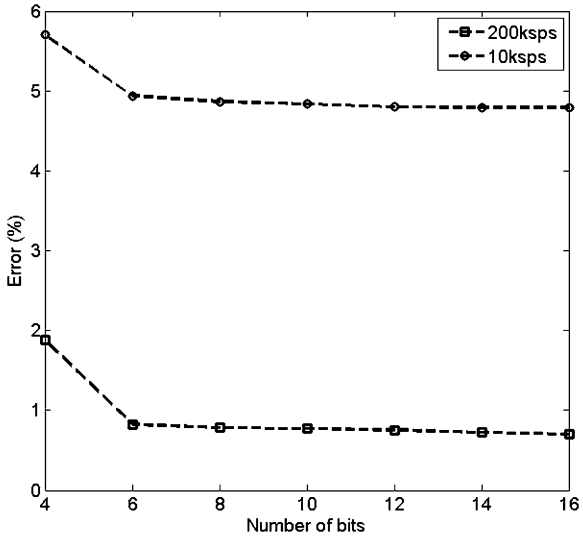

Fig. 8 Numerical results: synchronization error (9) between model with analog time-delay block and model with digital time-delay block versus number of bits

tained with a sampling frequency $f_s = 200$ kHz, independently of the number of bits used. Based on these considerations, the ADC and DAC used have been selected with a number of bits equal to 8 and $f_s = 200$ kHz. The results shown in Fig. 5 and Fig. 6 refer to this case.

The synchronization scheme corresponding to (8) has been implemented as shown in Fig. 9. The coupling circuit includes two operational amplifiers (U9A, U10A) and seven resistors (from R_{17} to R_{23}). The coupling parameter K is calculated as $K = \frac{R_{15}}{R_{23}}$. In the experimental setup, a 5 kΩ-potentiometer has been used as R_{23} to control the coupling strength value. A value of $R_{23} = 1$ kΩ has been used in all the experiments.

The data in the experiments have been acquired by using a data acquisition board (National Instruments USB-6255) with sampling frequency $f_s = 300$ kHz. As mentioned before, the accuracy of the implementation was evaluated by assuming as reference model a totally analog implementation in which the time-delay block has been realized with Bessel filters [20]. This totally analog implementation has been assumed as the master circuit, while the slave is the FPGA-based time-delay chaotic circuit. Synchronization is observed, as shown in Fig. 10(a) when the high speed analog-to-digital converter and high speed digital-to-analog converter (maximum throughput of 200 kHz) are used in the slave circuit. In contrast, when the ADC and DAC with large conversion time (low throughput of 10 kHz) are utilized, a much larger synchronization error occurs as shown in Fig. 10(b). It is worth noting that the conversion process parameters, especially the sampling rate, critically affect dynamical features of the circuits which were represented through the synchronization error. The synchronization errors in Fig. 10(a) and Fig. 10(b) are equal to $E = 0.8948\%$ and $E = 5.1212\%$, respectively (they have been evaluated taking into account an acquisition time window equal to 1 s). These experimental results well fit the simulation results, in the case of nonidentical systems, i.e., when the parameter tolerance of the circuit components used is taken into account, as it can be observed in Fig. 7.

The procedure described to evaluate the effects of the conversion parameters can be applied when a reference model does exist, which is obviously not the general case. Therefore, a more general strategy is here described. The idea is to acquire a long trajectory from the circuit and to use it to synchronize the slave circuit. Instead of the master signal x_m, the acquired signal is used. The experiment, previously described, was repeated by using this approach. First, a circuit with high speed analog-to-digital and digital-to-analog converters has been used. In this case, a low synchronization error ($E = 0.9687\%$) has been observed as shown in Fig. 10(c). On the opposite, when a low sampling rate 10 kHz ADCs and DACs is used, the synchronization error ($E = 5.2375\%$) grows up as shown in Fig. 10(d). The experimental results obtained confirmed that investigating synchronization by using a signal acquired from the chaotic circuit itself is a suitable strategy for the evaluation of the effects of the conversion parameters (or more in general of other parameters) on the accuracy of the implementation.

6 Conclusions

In this paper, a digital approach for the implementation of time-delay blocks in chaotic circuits, where usually the typical time-delays can be relatively large (order of magnitude of milliseconds) has been discussed. The approach makes uses of shift registers to introduce the desired delay and of a FPGA to implement a programmable circuitry. With respect to other approaches based on FPGA [1, 2, 12], the need of quite large time-delays has led to different design choices. While in [1, 2, 12], a number of separated units in cascade

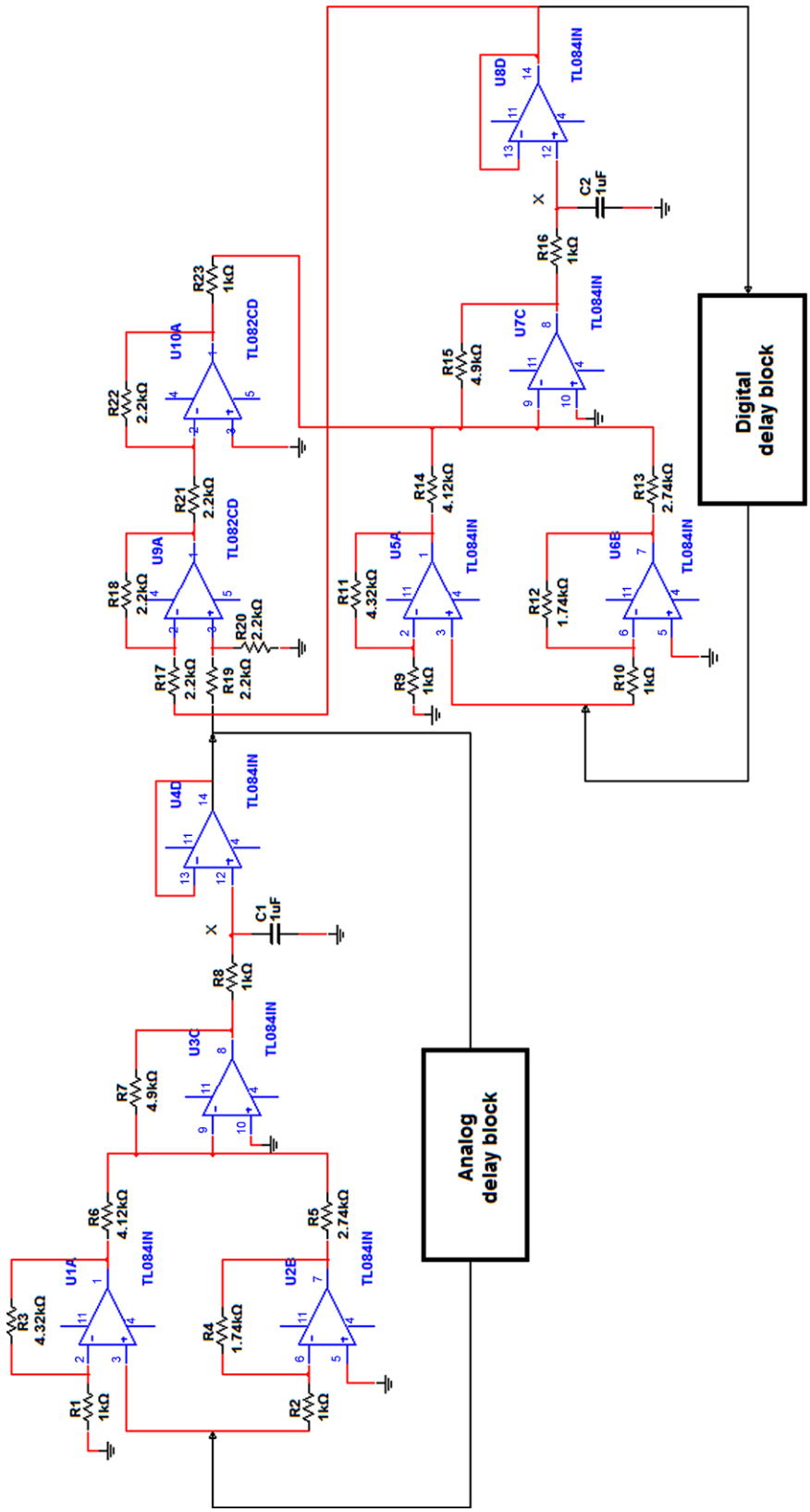

Fig. 9 Synchronization scheme between the chaotic circuit with an analog time-delay block and the one with a (FPGA-based) digital time-delay block. This scheme is used to evaluate experimentally the accuracy of the proposed FPGA-based time-delay chaotic circuit

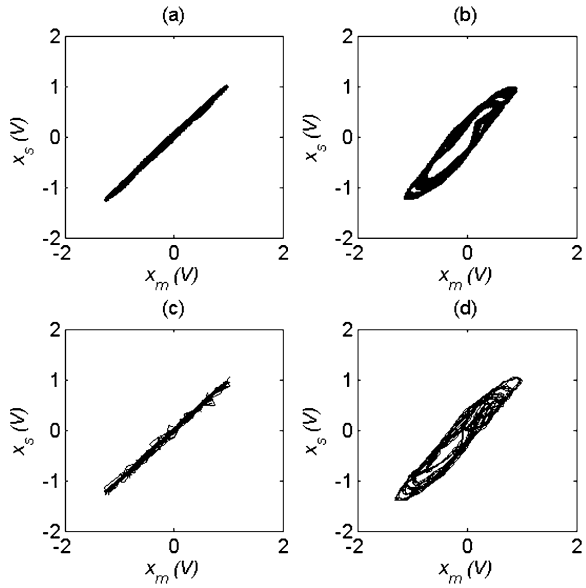

Fig. 10 x_s vs. x_m for (**a**) analog master/FPGA-based slave with high speed ADC; (**b**) analog master/FPGA-based slave with low speed ADC; (**c**) FPGA-based master with high speed ADC/FPGA-based slave with high speed ADC; (**d**) FPGA-based master with low speed ADC/FPGA-based slave with low speed ADC

(FPGA internal Configurable Logic Blocks (CLBs) [1], latches [2] or logic gates [12]) were employed to implement time-delays in a delay line and the separated units are placed manually by means of the floor planning tool (for instance, by means of the FloorPlanner, Xilinx ISE 5.2 software tool [2]), in our paper a shift register has been used. On one hand, this allows to obtain a larger time delay with respect to that implemented in [1, 2, 12]. On the other hand, the appropriate configuration of the shift register could be changed directly at a higher level, by working at VHDL code and optimizing the resources of the FPGA-based implementation.

In this paper, the effects due to the presence of an ADC and a DAC in the scheme have been also considered. These devices introduce a delay which is negligible with respect to the delay intentionally introduced in the circuit. On the other hand, our numerical and experimental analysis has pointed out as a crucial parameter is the sampling rate used in the conversion process, while the number of bits of ADC and DAC is less critical.

Furthermore, this paper has discussed a general method to evaluate the effects of these parameters and/or other sources of errors or parametric differences between implementation and model. The idea underlying our approach was to use the synchronization error between implementation model and ideal model (in simulation) or implementation and reference circuit (in experiments), as a low synchronization error clearly indicate that the two circuits have very similar uncoupled dynamics, since otherwise they cannot be synchronized. To this aim, it is crucial that the coupling in the synchronization scheme is weak, so that small parameter mismatches or structural differences can be detected.

Beyond the application investigated in this paper, i.e., the implementation of a circuit generating chaos thanks to the presence of a time-delay block, the FPGA-based method for realizing time-delays in the order of magnitude of milliseconds can be used to implement time-delayed feedback electronic controllers [7] for other chaotic circuits.

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