J Sol-Gel Sci Technol (2017) 83:675–682
DOI 10.1007/s10971-017-4468-y

ORIGINAL PAPER: SOL-GEL AND HYBRID MATERIALS FOR DIELECTRIC, ELECTRONIC, MAGNETIC AND FERROELECTRIC APPLICATIONS

Annealing temperature-dependent microstructure and optical and electrical properties of solution-derived Gd-doped ZrO_2 high-*k* gate dielectrics

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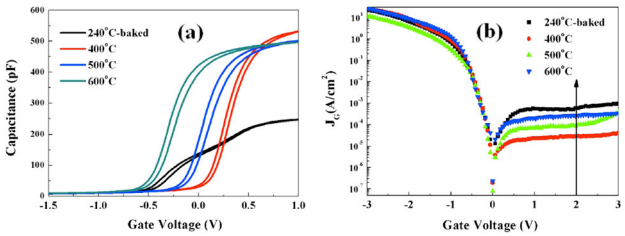
Received: 14 April 2017 / Accepted: 6 July 2017 / Published online: 17 July 2017

Abstract In current work, the microstructure and optical and electrical properties of sol–gel-derived Gd-doped ZrO_2 gate dielectric thin films as functions of annealing temperatures were systemically investigated. Analyzes by x-ray diffraction have indicated that the 240 °C-baked sample as well as those samples annealed at lower temperatures keep amorphous state. In the sample annealed at 500 °C, however, the amorphous phase disappears and tetragonal ZrO_2 is formed. Measurements from ultraviolet-visible spectroscopy (UV/Vis) have demonstrated that transmittance of all samples in the visible region is approximately 80% and the increase in band gap energy has been found with increasing the annealing temperature. Electrical properties of all samples based on Al/Si/$ZrGdO_x$/Al MOS capacitor have been investigated by using semiconductor device analyzer. Through the analysis and calculation of the electrical characteristic curves, solution-processed Al/$ZrGdO_x$/Si/Al capacitor shows improved performances at a annealing temperature of 400 °C, such as high dielectric constant (*k*) of 16.56, lowest oxidation charge density (Q_{ox}) of $-0.74 \times 10^{12}\,cm^{-2}$, and boundary trap oxidation charge density (N_{bt}) of $3.17 \times 10^{12}\,cm^{-2}$. In addition, the leakage current mechanism for 400 °C-annealed sample has been discussed in detail.

Graphical Abstract solution-processed Gd-doped ZrO_2 gate dielectric films were realized. Al/$ZrGdO_x$/Si/Al capacitor shows optimized and improved performances at a annealing temperature of 400 °C.



Keywords Gd-doped ZrO_2 gate dielectric thin films · Annealing temperature · Sol–gel · Optical properties · Electrical properties

1 Introduction

With the development of the semiconductor industry, the feature size of complementary metal-oxide-semiconductor field effect transistors (CMOSFETs) is becoming smaller and smaller. As a result, the thickness of traditional SiO_2 gate dielectrics has reached its physical limits due to high leakage current from channel to gate. By far, many high-*k* gate dielectrics have been paid more attention to replace conventional SiO_2 gate dielectrics due to its relatively large dielectric constant, suitable band gap, and excellent thermal stability in contact with Si [1–4]. Among these high-*k* gate dielectrics, ZrO_2 has been investigated extensively for its

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excellent performance, including large dielectric constant of 25, large band gap of about 5.8 eV, and outstanding physical and chemical stability [5–7]. However, for ZrO_2-based high-*k* gate dielectrics, there still exist some challenges, including the lower crystallization temperature and the oxygen vacancies existed in films, which lead to the formation of uncontrollably increased leakage current and degrade the performance of MOSFET devices. It has been reported that Gd incorporation into high-*k* ZrO_2 gate dielectrics can reduce oxygen vacancies, enlarge the band gap, increase the crystallization temperature, and optimize the electrical properties. By far, much works have been committed to investigate the effect of Gd incorporation on the thermal stability, interfacial and electrical properties of sputtering-derived ZrO_2 high-*k* gate dielectric thin films [8–11]. However, few work has been carried out to study the effect of annealing temperature on the structural and optical and electrical properties of the solution-processed Gd-doped ZrO_2 high-*k* gate dielectric thin films. Compared with physical vapor deposition, chemical vapor deposition, and atomic layer deposition (ALD) [12–15], solution-based method is gradually attracting more attention due to its simple operation, controllable molar ratio of elements, low cost and large-scale production [16–18].

In current work, solution-processed Gd-doped ZrO_2 high-k gate dielectric thin films were spin-coated on Si and quartz substrate, respectively. By means of characterizations from x-ray diffraction (XRD), spectroscopy ellipsometry (SE), ultraviolet-visible spectroscopy (UV/Vis), and semiconductor device analyzer, the effect of rapid thermal annealing temperature on the structural and optical and electrical properties of solution-derived Gd-doped ZrO_2 high-*k* gate dielectric thin films were investigated systematically.

2 Experimental details

2.1 Preparation of the precursor solutions

The Gd-doped ZrO_2 precursor solution was synthesized through dissolving a mixture of Zirconium oxychloride octahydrate ($ZrOCl_2$•$8H_2O$) and Gadolinium nitrate hexahydrate ($Gd_2(NO_3)_3$) in 2-methoxyethanol ($C_3H_8O_2$) solution (AR) with Zr/Gd molar ratio of 9:1. The precursor solution was stirred at room temperature for 360 min by a magnetic stirrer. Then, to get a more pure sol solution, the solutions were filtered through a 0.22 μm injection filter before spin coating.

2.2 Film deposition

First of all, all substrates such as n-type Si (100) wafers and quartz wafers were cleaned by a modified RCA (Radio Corporation of American) to remove surface impurities, and then all the wafers were immersed in a solution of 1% hydrofluoric acid for about 15 s to remove native SiO_2. Finally, all Si wafers and glass substrates dried by N_2 gun were placed in a plasma cleaner to enhance the hydrophilicity of the substrate surface. All the samples were prepared initially by a sol–gel machine at 5000 r.p.m. for 25 s, and then the thin films were placed on the roaster and baked at 240 °C for 5 min to remove the residual solvent and cooled to room temperature. To obtain the desired thickness, the procedure was repeated several times. For XRD characterization, the procedure was repeated five times. For electrical measurements, only one time was done. Finally, all thin films were annealed in vacuum environment (4.6×10^{-5} mbar) with annealing temperatures ranging from 400 to 600 °C for 5 min. The details of the preparation of the $ZrGdO_x$ thin films are shown in Fig. 1. The microstructure of Gd-doped ZrO_2 gate dielectric thin films related with annealing temperature were investigated by XRD. The thickness of Gd-doped ZrO_2 thin films was obtained by spectroscopy ellipsometry (SE) (SC630, SANCO Co, Shanghai). The ultraviolet-visible spectroscopy (UV/Vis) was carried out to investigate the annealing temperature-dependent band gap and transmittance spectra of the Gd-doped ZrO_2 gate dielectric thin films.

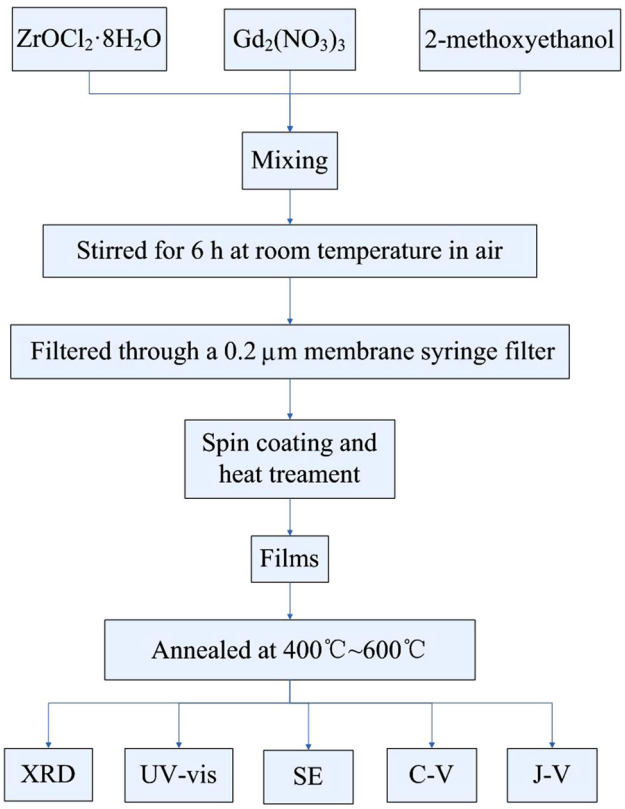

Fig. 1 The schematic flow chart of $ZrGdO_x$ gate dielectric thin films deposited by sol–gel method

2.3 Electrical performance measurements

In order to measure the electrical properties of the Gd-doped ZrO_2 thin films, MOS capacitors based on $ZrGdO_x$/Si gate stack were fabricated. The aluminum electrode with an area of 3.14×10^{-8} m^2 was sputtered to deposit on the top surface of samples. In order to keep ohmic contact, the back electrode was deposited by sputtering Al disk. The capacitance-voltage (*C-V*) and the leakage current density-voltage (*J-V*) of Al/ $ZrGdO_x$/Si/Al MOS capacitors as a function of annealing temperature were measured by using an Agilent B1500A semiconductor device analyzer. All electrical measurements were performed at room temperature in a dark shelter.

3 Results and discussion

3.1 Microstructure investigation

Figure 2 shows the XRD patterns of Gd-doped ZrO_2 gate dielectric thin films annealed at various temperatures. Based on Fig. 2, it can be noted that the 240 °C-baked Gd-doped ZrO_2 gate dielectric thin films are in an amorphous state. Annealing the samples in 400 °C, amorphous state still keeps and no crystallization has been detected. It is well known that microstructure is an important factor to affect the electrical properties of high-*k* gate dielectric thin films. For application in CMOS device, the amorphous states for high-*k* gate dielectrics are desirable due to their lower surface roughness and lower leakage current density [19, 20]. However, with rising the annealing temperature to 500 °C, the amorphous ZrO_2 disappears and new diffraction peaks have been observed, indicating that the crystallization for amorphous Gd-doped ZrO_2 thin films takes place at 500 °C, which is higher than previous results investigated by Chang [18]. Those four peaks located at 30.4, 35.1, 50.6, and 60.1°, corresponding to T(011), T(110), T(020), T(121), are attributed to the tetragonal phase of ZrO_2, which is in good agreement with the observations reported by Park [21]. Continuing increasing the annealing temperature to 600 °C, it can be seen that the intensity of the strong peak (011) of tetragonal ZrO_2 increases obviously, indicating that higher annealing temperature leads to the full crystallization of Gd-doped ZrO_2 gate dielectric thin films. Based on previous analyzes, it can be concluded that the crystallization of Gd-doped ZrO_2 gate dielectric thin films can be controlled by the annealing temperature.

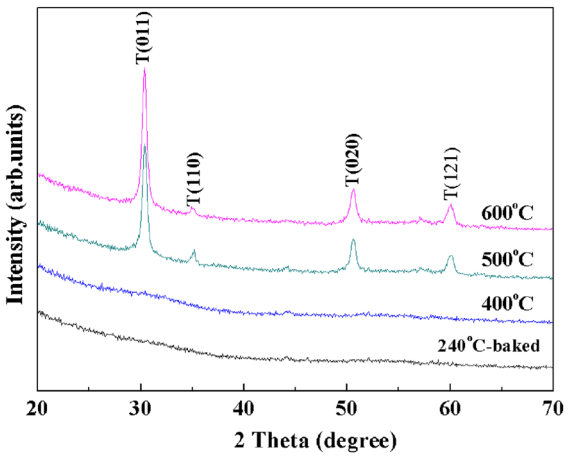

Fig. 2 The XRD patterns of $ZrGdO_x$ gate dielectrics thin films annealed at different temperatures

3.2 Optical properties analysis

For high-*k* gate dielectrics, the investigation of optical constants, such as optical band gap, transmittance spectra and the absorption spectra, will offer the criterion for choosing the suitable gate dielectrics for CMOS devices. Therefore, in current work, the evolution of the optical properties of solution-derived $ZrGdO_x$ thin films deposited on quartz glass was determined by UV/Vis measurements. Figure 3 shows the transmittance spectra as a function of annealing temperature with the range of wavelength from 190 to 900 nm. As demonstrated in Fig. 3, the average transmittance spectra of all samples at different annealing temperatures are about 80% in the visible region. To obtain the band gap of Gd-doped ZrO_2 gate dielectric thin films, UV/Vis absorption spectra of the $ZrGdO_x$ gate dielectric thin films annealed at various temperatures has been illustrated in Fig. 4.

The band gap of the $ZrGdO_x$ films can be obtained by the following formula [22, 23]:

$$\alpha h\nu = \left[A\left(h\nu - E_g\right)\right]^n \quad (1)$$

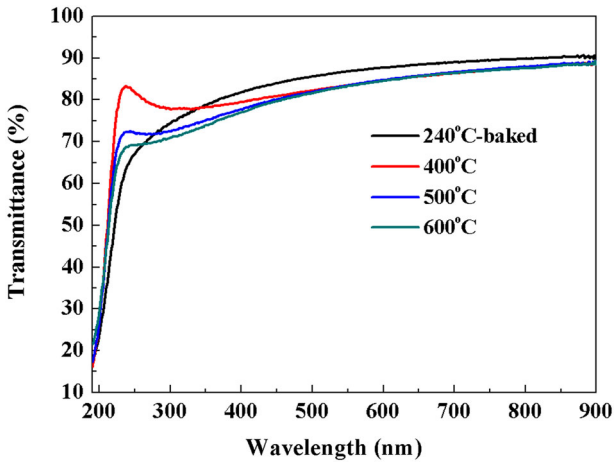

Fig. 3 Transmission spectra of $ZrGdO_x$ gate dielectric thin films

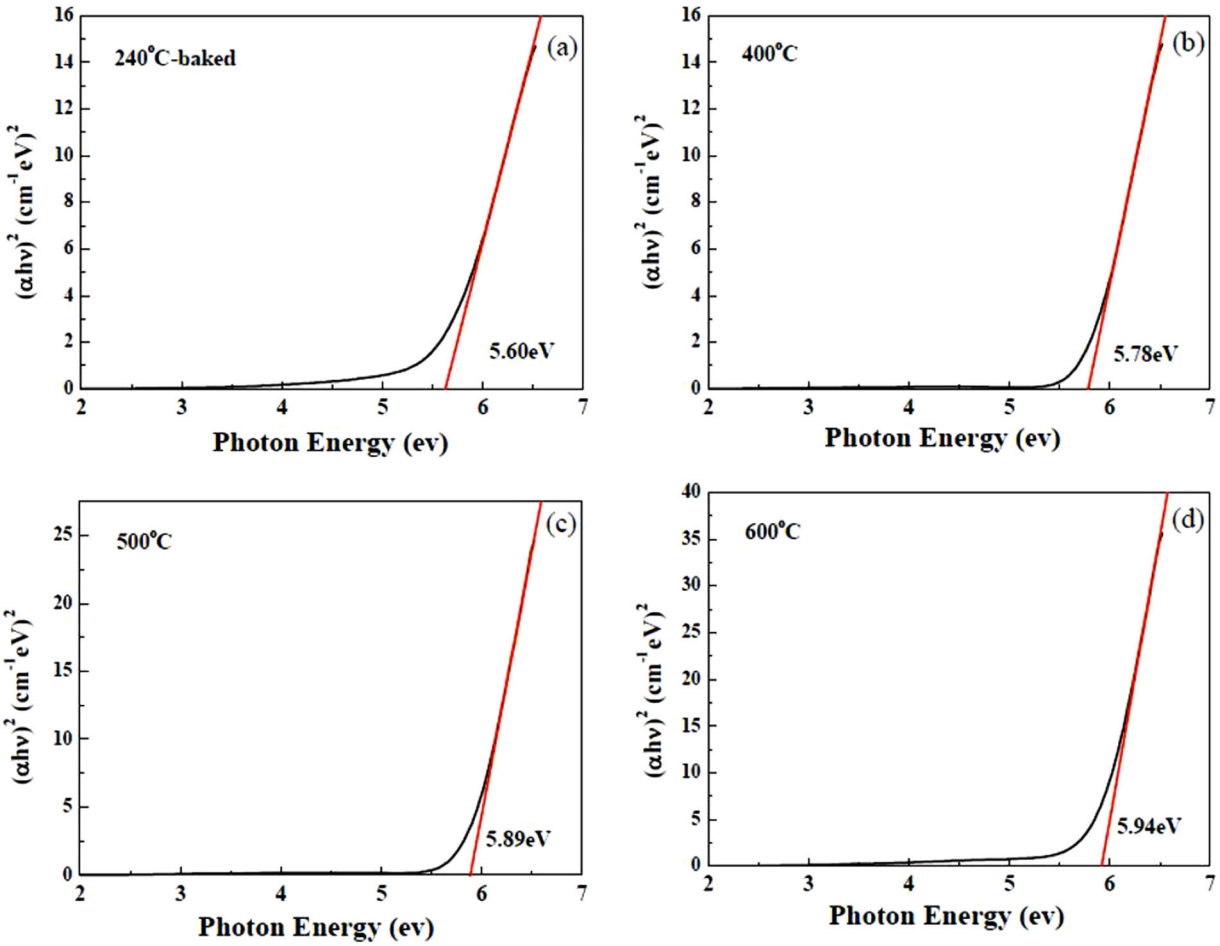

Fig. 4 Band gap determined by optical method using $(\alpha h\nu)^2$~$h\nu$ plots of $ZrGdO_x$ gate dielectric thin films deposited on quartz substrate

in which $h\nu$ is the photon energy, α is absorption coefficient and A is a semiconductor constant characteristic. The transition type of photoelectron between valence band and conduction band determines the value of the index n. Based on the different values of n, it can be determined whether this band gap is a direct band gap or an indirect band gap [24]. In current work, the optical direct band gaps of the $ZrGdO_x$ films were obtained through the linear tangent part of the curve relating $(\alpha h\nu)^2$ and $(h\nu)$ to $(\alpha h\nu)^2=0$. As demonstrated in Fig. 4, the optical direct band gaps have been determined to be 5.60, 5.78, 5.89, and 5.94 eV, respectively, with the increase of the annealing temperature. It is reported that the localized states is an important factor to affect the band gap. The localized states in the band structure attributed to the presence of defects and disorders in the films leads to the low energy gap. And high temperature annealing helps to reduce the oxygen vacancy and disorders in the film, so the density of the local state also decreases. Therefore the band gap increases while the annealing temperature increases [25].

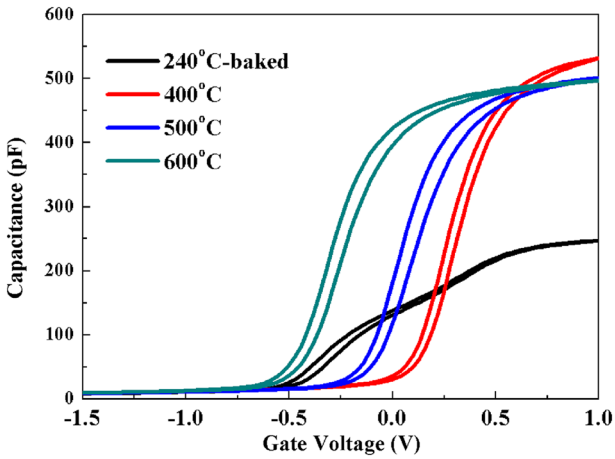

Fig. 5 Annealing temperature-dependent *C-V* characteristics of Al/$ZrGdO_x$/Si MOS capacitors

3.3 Electrical properties observations

Figure 5 shows the *C-V* curves of Al/$ZrGdO_x$/*n*-Si MOS capacitors measured at 1 MHz. As demonstrated in Fig. 5,

all the *C-V* curves show smooth characteristics in the scan region from −1.5 to 1 V and the 400 °C-annealed sample demonstrates the highest accumulation capacitance C_{ox} of 531 pF. Based on the following equations and the accumulated capacitance in the *C-V* curves, the equivalent oxide thickness (E_{ot}) and the relative dielectric constants (k_{hk}) of the $ZrGdO_x$ gate dielectric thin films have been determined [26]:

$$E_{ot} = \frac{k_{SiO_2}\varepsilon_o A}{C_{ox}} \tag{2}$$

$$k_{hk} = \frac{k_{SiO_2} \times t_{hk}}{E_{ot} - t_{SiO_2}} \tag{3}$$

in which k_{SiO2} is the relative dielectric constant of the SiO_2, ε_o is the vacuum capacitance, C_{ox} is the accumulated capacitor, A is the surface area of the aluminum electrode, t_{hk} and t_{SiO2} are the thicknesses of $ZrGdO_x$ films and SiO_2 layer, respectively. As shown in Table 1, the smallest equivalent oxide thickness of 2.04 nm and the highest dielectric constant of 16.56 have been obtained for the 400 °C-annealed sample. It can be seen that with the annealing temperature increasing from 400 to 600 °C, the dielectric constants of $ZrGdO_x$ films show a decreased trend, which can be attributed to the high temperature-induced formation of the low-*k* interfacial layer [27]. The flat band capacitance C_{fb} is calculated by the following formula [28]:

$$C_{fb} = \frac{C_{ox}}{1 + \frac{\varepsilon_{ro}}{\varepsilon_{rs} t_{hk}} \sqrt{\frac{kT\varepsilon_o\varepsilon_{rs}}{q^2 N_A}}} \tag{4}$$

where ε_{ro} is the dielectric constant of $ZrGdO_x$ thin film, N_A is the doping concentration of substrate, ε_{rs} is the dielectric constant of the Si substrate, N_A is the carrier concentration and t_{hk} is the thickness of the film, respectively. The value of flat band voltage V_{fb} and hysteresis ΔV_{fb} can be determined based on the C_{fb} values from *C*—*V* curve respectively. According to Table 1, it can be noted that $ZrGdO_x$ gate dielectric thin film annealed at 400 °C has the lowest flat band voltage. As we know, the flat band voltage has been determined by the traps and defects located at interface layer. Therefore, it can be concluded that the samples annealed at 400 °C have less defects and traps and contributes to the lowest flat band voltage [29–33]. The oxidation charge density Q_{ox} can be expressed by the following equation [28]:

$$Q_{ox} = \frac{-C_{ox}(V_{fb} - \varphi_{ms})}{qA} \tag{5}$$

where ϕ_{ms} is the work function difference between metal electrode and silicon substrate, *A* is the area of Al electrode and *q* is electricity of charge. From Table 1, the Q_{ox} of the 240 °C-baked, 400, 500, and 600 °C-annealed samples were calculated to be $1.67 \times 10^{12}\,cm^{-2}$, $-0.74 \times 10^{12}\,cm^{-2}$, $1.50 \times 10^{12}\,cm^{-2}$, and $4.94 \times 10^{12}\,cm^{-2}$, respectively. Based on previous reports, it can be concluded that the large negative V_{fb} shift and the negative Q_{ox} can be due to the presence of oxygen vacancies, the interface state and defects [34].

The boundary trap oxidation charge density (N_{bt}) was calculated by using following expression [35, 36]:

$$N_{bt} = \frac{-C_{ox}\Delta V_{fb}}{q} \tag{6}$$

As demonstrated in Table 1, the Q_{ox} and N_{bt} are lower than other samples when the annealing temperature is fixed at 400 °C, indicating that 400 °C-annealed sample has demonstrated the improved interfacial quality.

Figure 6 shows the *J-V* curves for Al/$ZrGdO_x$/n-Si MOS capacitors with different annealing temperatures. Based on Fig. 6, it can be seen that the leakage current density for the

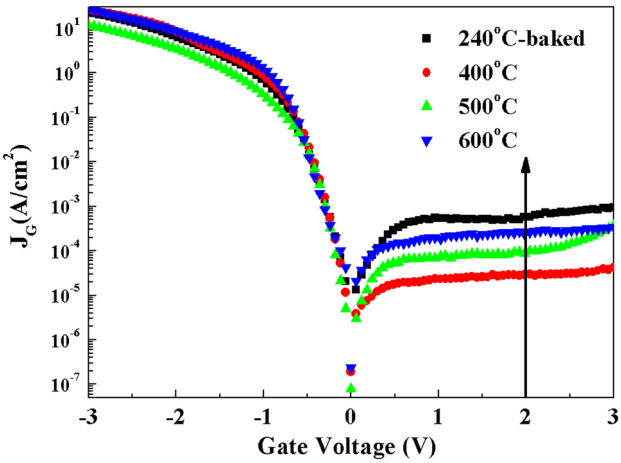

Fig. 6 *J–V* characteristics of MOS capacitors with $ZrGdO_x$/Si gate stacks

Table 1 Parameters of the MOS capacitors extracted from *C-V* curves

Annealing temperature (°C)	C_{ox} (pF)	*t* (nm)	E_{ot} (nm)	*k*	C_{fb} (pF)	V_{fb} (V)	ΔV_{fb} (V)	Q_{ox} (cm^{-2})	N_{bt} (cm^{-2})
240 °C-baked	247	12.49	4.39	11.10	60.59	−0.30	−0.07	1.67×10^{12}	3.44×10^{12}
400	531	8.66	2.04	16.56	69.68	0.10	0.03	-0.74×10^{12}	3.17×10^{12}
500	501	8.20	2.16	14.81	69.07	−0.12	0.06	1.47×10^{12}	5.98×10^{12}
600	496	7.91	2.19	14.09	69.20	−0.47	0.06	4.94×10^{12}	4.94×10^{12}

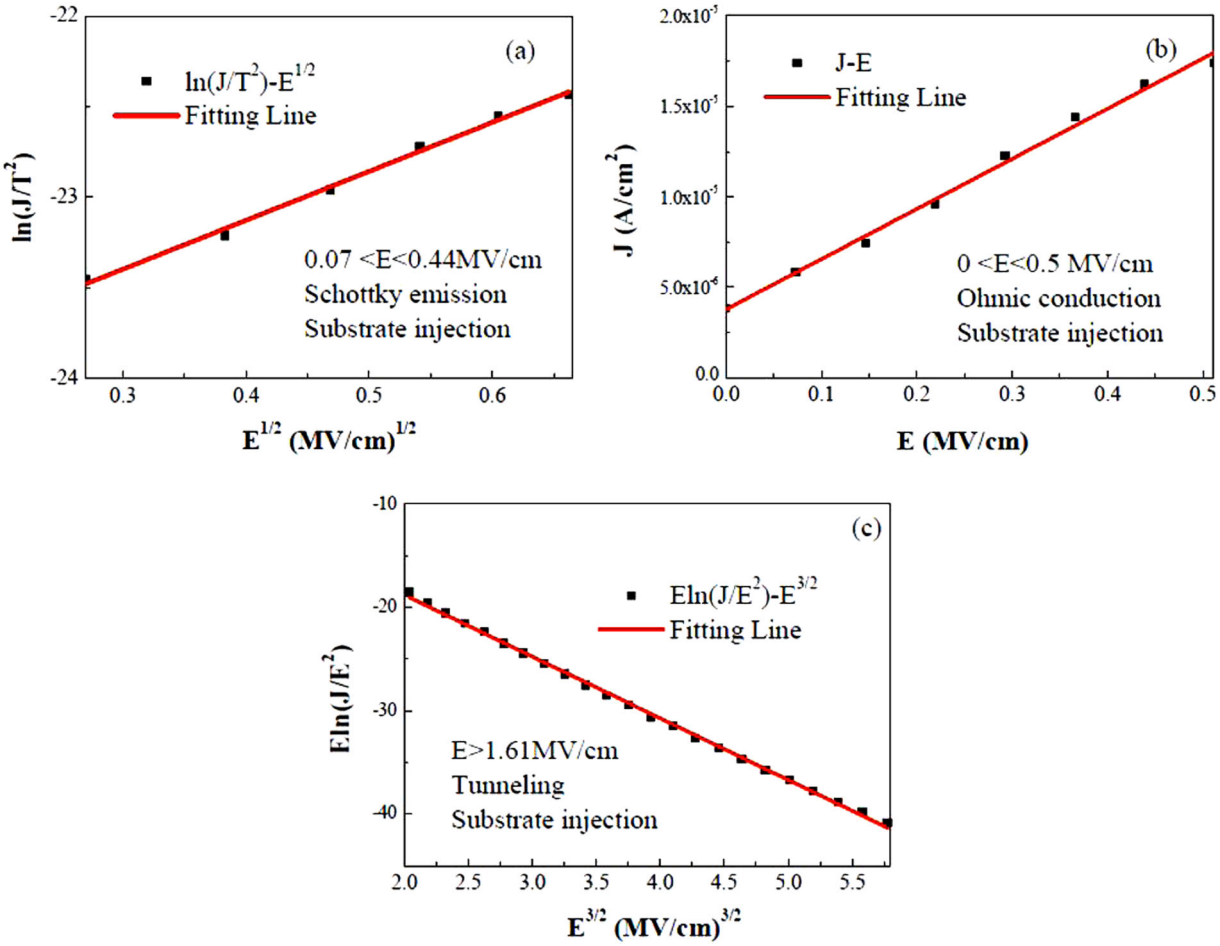

Fig. 7 Leakage current conduction mechanism of Al/$ZrGdO_x$/Si MOS capacitors annealed at 400 °C under substrate injection. **a** The curve of ln(J/T^2) vs $E^{(1)/(2)}$ in low electric field; **b** the curve of J vs E in low electric field; **c** the curve of $E\ln(J/E^2)$vs $E^{(3)/(2)}$ in high electric field

240 °C-baked and the annealed samples at 400, 500, and 600 °C is 5.15×10^{-4} A/cm^2, 2.28×10^{-5} A/cm^2, 7.36×10^{-5} A/cm^2, 1.90×10^{-4} A/cm^2, respectively, when the gate voltage is fixed at 2 V. Indrek [10] has reported that the leakage current density of 6-nm-thick $Zr_xGd_yO_z$ gate dielectrics prepared by ALD is 10^{-6}A/cm^2 at 1 V, and reaches to about 10^{-5} A/cm^2 at 2 V, which is similar to our result. As we know, ALD can prepare highly uniform and dense film and has an excellent prospect in the manufacture of microelectronic device. In our current work, solution-based method was selected and the electrical properties of gate dielectrics was very close to ALD method. Compared to other samples, 400 °C-annealed sample demonstrate the lowest leakage current density, which can be attributed to the lower interface states density at $ZrGdO_x$/Si interface [37]. With the increase of annealing temperature, the leakage current densities increase, which is probably due to the reduced conduction band offset caused by the high oxide charge and trap charge with the increase of annealing temperature based on previous *C-V* results [38]. In addition, the high annealing temperature leads to the crystallization of $ZrGdO_x$ gate dielectric thin films and attributes to the increased leakage current.

According to previous analyzes, it can be concluded that $ZrGdO_x$ gate dielectric thin film annealed at 400 °C demonstrates the improved electrical performance and optimized electrical parameters, suggesting that 400 °C-annealed sample has potential application in CMOSFET devices.

3.4 Leakage current mechanism analysis

In order to investigate the leakage current conduction mechanisms of the $ZrGdO_x$ gate dielectric thin films, the Schottky emission (SE), Ohmic conduction and direct tunneling were analyzed for samples annealed in 400 °C by linear curve fitting method. Schottky emission is a field-assisted thermionic emission of an electron over a surface barrier, which is the most likely current conduction mechanism in gate dielectrics [39]. The leakage current

density determined by SE is given by [40]:

$$J_{SE} = A^* T^2 \exp\left[\frac{-q\left(\phi_B - \sqrt{\frac{qE}{4\pi\varepsilon_o\varepsilon_r}}\right)}{k_B T}\right] \quad (7)$$

in which A is the effective Richardson constant, φ_B is the Schottky barrier height, T, $q\phi_B$, E, ε_o, ε_r, and k_B, are the absolute temperature, the trap barrier height between semiconductor and oxide, the electric field in oxide, the vacuum permittivity, the dynamic dielectric constant and the Boltzmann constant, respectively. Figure 7a presents the plot of $\ln(J/T^2)$ vs. $E^{(1)/(2)}$ for the $ZrGdO_x$ gate dielectrics thin films at low electric field ($0.07 < E < 0.44$ MV/cm), indicating that the *J-E* curve measured in low electric fields fits well with the schottky emission. In addition, Ohmic conduction is caused by the movement of mobile electrons in the conduction band and holes in the valence band. Figure 7b shows the plot of J vs. E and the good and linear fitting at low electric field indicates the existence of Ohmic conduction mechanism. When the electric field has been increased to higher than 0.50 MV/cm, leakage conduction mechanism has been replaced by other mode. The plot of $\mathrm{Eln}(J/E^2)$vs. $E^{3/2}$at different annealing temperatures is presented in Fig. 7c, indicating the existence of direct tunneling when the electric field is higher than 1.64 MV/cm.

4 Conclusion

In summary, the microstructure, optical and electrical properties of $ZrGdO_x$ gate dielectric thin films deposited by sol–gel method as functions of annealing temperatures have been systematically investigated. XRD measurements show that the $ZrGdO_x$ gate dielectric thin films change from amorphous state to stable tetragonal phase with the increase of annealing temperature. Based on the optical properties analysis, it can be noted that annealing leads to the increase in band gap energy, which can be attributed to the reduction in localized states in the band structure. Electrical investigation demonstrates that 400 °C-annealed $ZrGdO_x$ gate dielectric thin film has the improved electrical performance and optimized electrical parameters, such as the highest dielectric constant, smallest flat band voltage hysteresis, border trapped oxide charge density and low leakage current density. Based on the analysis of leakage current conduction mechanism, it can be noted that Schottky emission and Ohmic conduction are main conduction mechanisms in low electric fields. The main conduction mechanism in the high electric field is the direct tunneling mechanism. Therefore, it can be concluded that the $ZrGdO_x$ gate dielectric thin film annealed at 400 °C shows potential application for future MOS devices.

Acknowledgements The authors acknowledge the support from National Natural Science Foundation of China (51572002,11474284), Technology Foundation for Selected Overseas Chinese Scholar, Ministry of Personnel of China (J05015131), Anhui Provincial Natural Science Foundation (1608085MA06).

Compliance with ethical standards

Conflict of interest The authors declare that they have no competing interests.

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