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A NOVEL PROPOSAL FOR AN ALL-OPTICAL "AND" LOGIC GATE USING TWO-DIMENSIONAL PHOTONIC CRYSTALS

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Abstract

We present a novel proposal for an all-optical AND logic gate. It is designed based on line and point defects in two-dimensional photonic crystal (PC) rods in air with square lattice. Material of the rods is silicon with dielectric constant 11.56. Dimension of the proposed device is equal to 12.155×12.155 μm. The device elaborated has a simple structure consisting of two inputs – a main output and two idler outputs. Bit rate of the device is equal to $3\cdot 10^{12}$ bit/s. Maximum contrast ratio is 5.84 dB. It is a good candidate for optical integrated circuits.

Keywords: coupled-mode theory, defects, electromagnetic fields, photonic crystals.

1. Introduction

Logic gates are one of the most important elements in logical circuits and digital signal processing. General logical gates are electronic gates, which means that the particle used in these gates is the electron [1–4]. Nowadays, high-speed devices are necessary with the ever-increasing progress in technology. Because photon with a phase velocity of $\sim 3\cdot 10^8$ m/s is the basic particle in optics, optical devices are suitable alternatives for electronic devices; recently, all-optical devices are introduced which have high velocity (close to the light velocity), simple structure, and low power consumption [5–20].

All-optical logic gates are basic devices in all-optical logical circuits. Many of these devices are designed and fabricated with photonic crystals (PCs) such as XOR [6,11,13,14], OR [6,12–14], NAND [7, 12–14], AND [12, 14], NOR [7, 14], and demultiplexers [5]. PCs are periodic dielectric materials that are very applicable in designing optical devices [5–14]. Most of the devices using PCs operate based on defects [5–14], self-collimation effects [15–18], and nonlinear effects [19, 20].

In this paper, we propose and simulate an all-optical AND logic gate. The proposed gate has two inputs A and B, two idler output ports, and a main output port O. If the two input ports are logical 1, then the main output will be logical 1; otherwise, the main output will be 0. Logical 1 means ON, and logical 0 means OFF. In electrical logical circuits, logical values 1 and 0 are voltages, but in all-optical systems there are light waves with suitable intensity or power. This gate has a few benefits compared to other all-optical AND gates such as high contrast ratio, simple structure, reasonable size, and high speed (Tbit/s).

This paper is organized as follows.

In Sec. 2, we represent the structure of the device proposed. In Sec. 3, we discuss the physics and simulations of the proposed gate, and in Sec. 4 we give our conclusions. The numerical methods for

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simulating the structure are the two-dimensional finite difference time domain (FDTD) and the plane wave expansion (PWE).

2. Structure

In Fig. 1, we show the schematic structure of the proposed all-optical AND logic gate. The gate has square lattice structure with silicon circular rods in air with the refractive index equal to 3.46 ($\varepsilon = 11.56$). Dimensions of the device are $(18a + 2r) \times (18a + 2r)$ μm^2, where a is lattice constant and r is radius of rods, equal to $0.35a$.

One can observe in Fig. 1 that the gate has two input ports A and B and a main output port O. The other two output ports are idler ports and have been created for realization of the gate. There are two types of defects. First are point defects P_1 and P_2 in blue color located for scattering the light waves and guiding light to the output. Second are line defects created in ΓX and XM directions for guiding light waves to the main output as illustrated in Fig. 1.

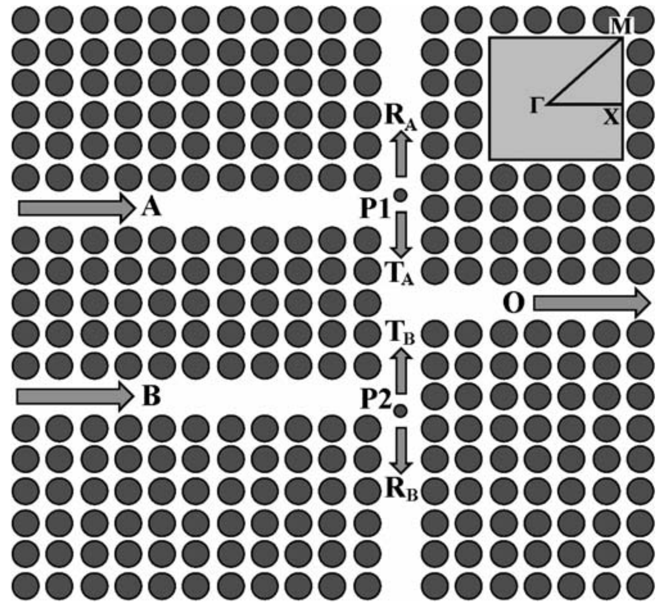

Fig. 1. Schematic structure of the proposed gate; here, P_1 and P_2 rods are scattered rods, A and B are input ports, O is the main output port, and the other two ports are idler ports. Inset: reduced Brillouin zone.

3. Physics and Simulations

In this section, we describe the physics of the gate and its simulation. The photonic band structure for TE and TM modes is shown in Fig. 2. Calculation of the band structure is performed by the numerical PWE method. The Maxwell equations govern the physics of the device [21].

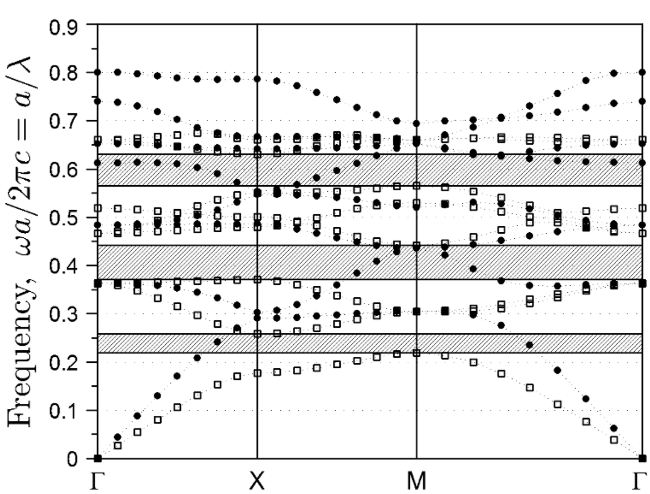

Fig. 2. Electromagnetic band structure of Fig. 1 for the TE (□) and TM (●) modes.

According to the coupled-mode theory (CMT) and simulations, the radii of rods S_1 and S_2 can be determined. The CMT equations at $w = w_0$ for a three-port system with an optical resonator as shown in Fig. 3 read [21]

$$R = \left|\frac{S_{1-}}{S_{1+}}\right|^2 = \frac{(1/\tau_1 - 1/\tau_2 - 1/\tau_3)^2}{(1/\tau_1 + 1/\tau_2 + 1/\tau_3)^2}, \qquad (1)$$

$$T_{1\to 3} = \left|\frac{S_{3-}}{S_{1+}}\right|^2 = \frac{4/\tau_1\tau_3}{(1/\tau_1 + 1/\tau_2 + 1/\tau_3)^2}, \qquad (2)$$

$$T_{1\to 2} = \left|\frac{S_{2-}}{S_{1+}}\right|^2 = \frac{4/\tau_1\tau_2}{(1/\tau_1 + 1/\tau_2 + 1/\tau_3)^2}. \qquad (3)$$

Here, S_{i+} and S_{i-}, $i = 1, 2, 3$, are amplitudes of incoming and outgoing optical waves, $1/\tau_1$, $1/\tau_2$, and $1/\tau_3$ are decay rates at port 1, port 2, and port 3, respectively [21–23], $T_{1\to 2}$ is the transmission from port 1 to port 2, $T_{1\to 3}$ is the transmission from port 1 to port 3, and R is the reflection at port 1, as illustrated in Fig. 3.

Comparing Fig. 3 with Fig. 1, we observe that port 1 is like port A, and ports 2 and 3 are as the same as T_A and R_A. Also, with application of optical wave to port A, S_{+3} and S_{+2} must be zero. If we define a new rule like TTL in digital electronics, power of light more than $0.8P_0$ will be defined as logical 1, and power of light less than $0.3P_0$ will be defined as logical 0. So optical powers $0.96P_0$ and $0.25P_0$ are logical 1 and 0, respectively, where P_0 is the incident optical wave power. For realizing all-optical AND logic gate, radii of P_1 and P_2 must be tuned so as to achieve suitable output power at port O equal to $0.25P_0$, when state A is equal to logical 1 and B is equal to logical 0, and vice versa. For states A equal to logical 1 and B equal to 1, the output power O must be equal to $0.96P_0$. In accordance with numerical simulations, P_1 and P_2 as the radii of rods will be both set to $0.64a$.

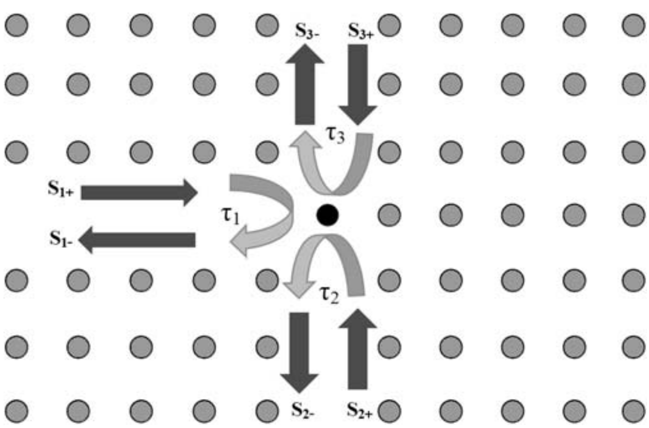

Fig. 3. Schematic of three-port waveguide system with the resonance cavity in gray [21].

The equations governing the device are [5]

$$E_A = E_B = A\,\mathrm{e}^{-i\phi}, \tag{4}$$

where E_A and E_B are the incident TE-polarized light waves with phase ϕ and amplitude A. Because of the structure symmetry of the gate, the incident electrical waves are the same, $E_A = E_B$.

The transmission and reflection amplitudes of light after passing P_1 are $t\,\mathrm{e}^{i\varphi}\,E_A$ and $r\,\mathrm{e}^{i(\varphi+\pi/2)}\,E_A$, respectively, with the transmission phase φ and the reflection phase $\varphi+\pi/2$. The transmission and reflection coefficients t and r are the same as $\sqrt{T_{1\to 2}}$ and $\sqrt{T_{1\to 3}}$ when $R=0$, i.e., $t^2+r^2=1$. Again, due to the structure symmetry and the same incident optical waves, the output electric field is

$$E_O = E_{T_A} + E_{T_B} = 2E_{T_A} = 2t\,\mathrm{e}^{i\varphi}\,E_A \to E_O = 2At\,\mathrm{e}^{i(\varphi-\phi)}\,. \tag{5}$$

Then the intensity and power at port O are

$$I_O = |E_O|^2 = 4A^2t^2 = 4I_0t^2, \qquad P_O = \frac{I_O}{\text{Area}} = \frac{4I_0t^2}{\text{Area}}. \tag{6}$$

We determine numerically all parameters for designing the gate from previous analytical equations by simulations. For determining the radii of the other rods of the gate, we performed frequency analysis in order to choose the best radius for the structure. Figure 4 and Table 1, respectively, contain frequency simulations of Fig. 1 for the two states and truth table of the AND gate.

Table 1. Truth Table of "AND" Logic Gate.

Input A	Input B	Output O (Logical)
0	0	0
0	1	0
1	0	0
1	1	1

The contrast ratio of power for the previous rule of logical 1 and 0 is 4.26 calculated from the relation $10\log(P_{\text{on}}/P_{\text{off}})$ dB, where P_{on} represents the threshold power at state 1 and P_{off} is the threshold power at state 0.

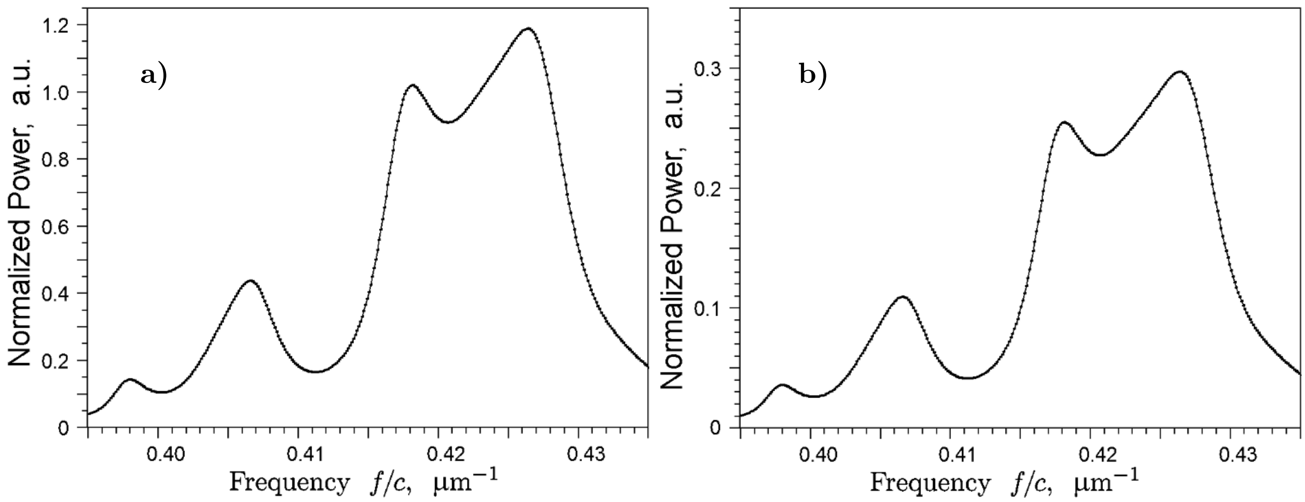

Fig. 4. Frequency analysis for the all-optical AND logic gate. Here, two inputs A and B are logical 1 (a), and one of the inputs is logical 1 and the other is 0 (b).

Based on the previous frequency simulation shown in Fig. 4, at a/λ equal to 0.42, when one of the inputs is logical 0 and the other is logical 1, the output power is $0.25P_0$, which is less than $0.3P_0$ and considered to be off. When two inputs are logical 1, the output power will be $0.96P_0$, which is more than $0.8P_0$, and so is logical 1. As a result, at this value of a/λ, we can realize the all-optical AND logic gate. We choose the wavelength of the incident field $\lambda = 1.55$ μm, which is commonly used in optical devices such as optical fibers and optical logic gates. According to $a/\lambda = 0.42$, with choosing lambda equal to 1.55 μm, the lattice constant $a = 0.65$ μm.

To simulate the structure in time domain, we use numerical solutions to plot the distribution of electric or magnetic fields of the gate by applying Gaussian input waves. One of these numerical solutions is the finite difference time domain (FDTD) [24]. In Fig. 5 a, we show the electrical distribution and normalized power of the TE mode for A and B equal to logical 1. In Fig. 5 b, we show the electrical distribution and normalized power of the TE mode for A equal to logical 1, and B equal to logical 0.

Table 2. Truth Table of the All-Optical "AND" Gate.

Input A	Input B	Output O (Logical)	Output O (Power)
0	0	0	0
0	P_0	0	$0.25P_0$
P_0	0	0	$0.25P_0$
P_0	P_0	1	$0.96P_0$

In Fig. 5, we show the output power for the gate versus its length and the distribution of TE polarized electrical fields. In Fig. 5 a, A and B are logical 1; due to more output power (about P_0) compared to $0.8P_0$, this output port will be logical 1. In Fig. 5 b, A is logical 1 and B is logical 0, and the output power is about $0.25P_0$, which is less than $0.3P_0$; so it will be logical 0. According to the simulations, we designed the all-optical AND logic gate with a reasonable maximum contrast ratio of 6 dB and an ordinary contrast ratio of 4.26 dB. We can conclude, in view of Fig. 5, that the steady state length $cT = 100$ μm, and $f = 1/T = 3$ THz. Therefore, the speed of gate is 3 Tbit/s. Table 2 represents the truth table of AND logic gate.

In Table 3, we compare the proposed all-optical AND logic gate with other counterparts in two-dimensional PCs. Reviewing the literature, the maximum contrast ratio has been utilized for comparison

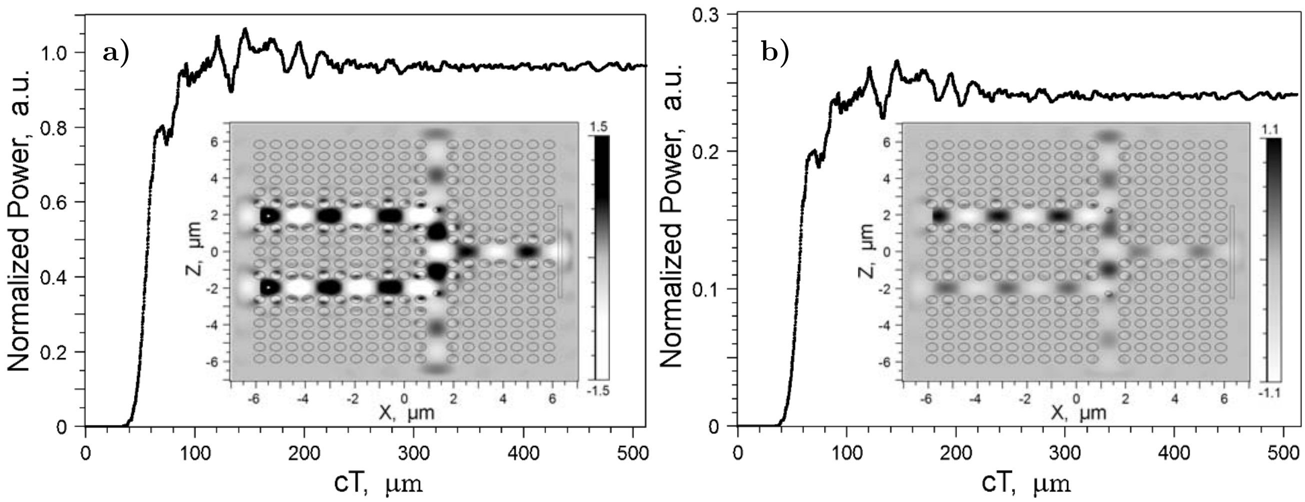

Fig. 5. The output power of the all-optical AND gate proposed and the distribution of the incident electrical field of the TE mode for Gaussian continuous wave. In the plots, c is the speed of light and T is time. Here, A = 1 and B = 1, and the output power is about P_0, which is more than $0.8P_0$, and the output state is logical 1 (a), and A = 1 and B = 0, and the output power is about $0.25P_0$, which is less than $0.3P_0$; then the output state is logical 0 (b). Maps of E_y are shown in insets.

between AND gates by the relation $10\log(P_{\rm on}/P_{\rm off})$. It is better to design logical gates with output power of the ON state as P_0 and that of the OFF state to be zero. Therefore, we can infer from Table 2 that the proposed gate has very suitable output power of the ON state about $0.96P_0$ among others, and output power of the OFF state about $0.25P_0$. So the maximum contrast ratio will be 5.84 dB, which is very high among all other optical AND gates. The footprint of the proposed device is also reasonable and equal to 147.75 μm^2 in comparison with other optical AND gates. The proposed gate has very good bit rate equal to 3 Tbit/s compared to others.

Table 3. Comparison between Our All-Optical "AND" Logic Gates and Some Other Previous Ones.

Parameters	[14]	[23]	[16]	Proposed gate
Size (μm^2)	27.8784	303.42	175.16	147.75
Speed (TBit/s)	0.976	-	-	3
Output power when two inputs are 1	$0.46P_0$	$0.5P_0$	$0.75P_0$	$0.96P_0$
Output power when one input is 1 and the other is 0	$0.17P_0$	$0.125P_0$	$0.25P_0$	$0.25P_0$
Maximum contrast ratio	4.33	6	4.77	5.84

4. Conclusions

In this paper, we presented the design and simulations of a novel all-optical AND logic gate in a two-dimensional PC. The structure of the gate is simple, consisting of silicon rods in air with the dielectric constant equal to 11.56. We used the Maxwell equations as the basis for our calculation and simulations. We considered optical powers greater than $0.8P_0$ as 1, and those less than $0.3P_0$ as 0. The maximum contrast ratio is 5.84 dB, the ordinary contrast ratio is 4.26 dB, and bit rates are 3 Tbit/s. Wavelength of the incident optical wave in the structure is 1.55 μm, which is reasonable for optical fibers and other optical devices. This device is applicable to all-optical digital circuits.

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