J Med Syst (2011) 35:221–235
DOI 10.1007/s10916-009-9359-5

ORIGINAL PAPER

ASIC Design of a Digital Fuzzy System on Chip for Medical Diagnostic Applications

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Received: 18 May 2009 / Accepted: 27 July 2009 / Published online: 27 August 2009

Abstract The paper presents the ASIC design of a digital fuzzy logic circuit for medical diagnostic applications. The system on chip under consideration uses fuzzifier, memory and defuzzifier for fuzzifying the patient data, storing the membership function values and defuzzifying the membership function values to get the output decision. The proposed circuit uses triangular trapezoidal membership functions for fuzzification patients' data. For minimizing the transistor count, the proposed circuit uses 3T XOR gates and 8T adders for its design. The entire work has been carried out using TSMC 0.35 μm CMOS process. Post layout TSPICE simulation of the whole circuit indicates a delay of 31.27 ns and the average power dissipation of the system on chip is 123.49 mW which indicates a less delay and less power dissipation than the comparable embedded systems reported earlier.

Keywords Medical diagnosis · System on chip · Fuzzy logic · ASIC

Introduction

Medical diagnosis is a complicated and judgmental process, based not only on medical knowledge derived from books and literatures and data obtained from various pathological tests, but also is largely dependant on experience, judgment and reasoning which essentially are the functions of human brain [1]. But, in many situations, availability of human brain for decision-making becomes scarce. Instruments, in those situations, play a major role in helping to reduce human suffering.

In third world countries, doctors are scarcely available in rural areas. Despite huge strides in overall development, the health coverage to majority of population in third world countries like India is a distant dream. India, today, has a population far exceeding 1 billion. But there is a finite limit of elasticity in providing health care in terms of infrastructure, facility, the manpower and the funds. Wide disparities persist between different income groups, between rural and urban communities, and between different states and even districts within states.

A recent statistical data shows that 75% of qualified consulting doctors reside in urban areas and another 23% in semi-urban areas, and only about 2% of doctors reside in rural areas, where, unfortunately, nearly 78% of Indians reside [2]. This has created an unwarranted unbalance in patient–doctor ratio to more than 10,000 patients for one doctor in rural India [3]. Further, this is compounded by factors like high cost of health care and lack of investment for health care in rural areas, inadequacy medical facilities in rural and inaccessible areas, problem of retaining doctors in rural areas, etc [2]. The need for a low cost system that can predict an imminent health hazard and red-alert the patients to contact doctor for necessary care, therefore, becomes pertinent.

Recently, fuzzy logic has been widely applied in the medical diagnosis and feature extraction [4–7]. One of the advantages of fuzzy logic is that it can be established empirically without explicit mathematical models of non-

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linear physiological systems [8, 9]. Fuzzy logic is used in situations where approximate values of patient data are to be analyzed using linguistic variables [10]. In order to implement the fuzzy logic on hardware, a fuzzy processor needs to be developed. A number of works have been carried out in the development for hardware for fuzzy systems. The pioneer in this investigation field was Togai and Watanabe [11], who proposed the first hardware for fuzzy logic. Lim and Takefuji first proposed of implementing fuzzy rule based systems on silicon [12]. A large number of contemporary fuzzy systems use general purpose processors to process fuzzy inferences [13, 14]. Although, the solution is a highly flexible one, it is only appropriate where the inference speeds required are not excessively high, i.e. in the order of a few KFLIPS. The performance can be improved by suitable algorithmic modification [15]. However, with very high values this approach is quite inadequate, especially in high performance applications.

In high performance fuzzy systems, therefore, it is necessary to use hardware architecture capable of performing fuzzy computations [16, 17]. Manzoul and Tayal in [18], and Jaramillo-Botero and Miyake in [19] proposed the implementation of high speed fuzzy controllers using multiprocessor based parallel computing architectures. Multiple processors entail for costly solution of the system. The cost of multiple chips can be minimized by using single chip multiprocessor architectures (MP SoC). Using a multiprocessor system-on-chip architecture is a crucial step to optimize performance, energy and memory constraints at the same time, as has been reported by Orsila et al in [20]. Aranguren proposed the implementation of a pipelined fuzzy processor with a single rule unit [21]. Samoladas and Petrou propose two parallel architectures in SIMD mode [22]. Salvador presents a systolic architecture of four antecedents and 70 rules for consequences [23]. Although such a design is not very flexible as in the case of general purpose processors, it gives better results in terms of performance. The benefit of hardware implementation of a processor is also explained in [24] by Raychev, Mtibaa and Abid. However, the design and implementation flexibility is considerably improved by mapping the design into reconfigurable architectures like FPGA. The authors have proposed an FPGA based medical diagnostic decision making embedded system in [25] and further optimized its performance to improve speed and diagnosing accuracy in [26, 27, 28].

However, the medical diagnostic system has been developed to cater the needs of rural health care centre that are devoid of physicians. Hence, the diagnostic systems are required in bulk amounts. It is therefore reasonable to go for an ASIC design of the medical diagnostic system on chip, since ASIC when amortized over large volumes prove to be economical than FPGA. Compared to an FPGA based embedded system which may have a projected cost of around 4,000 INR (including peripherals) the cost of the system on chip used for medical diagnostic applications may be around 1,500 INR amortized over a volume production of 100,000 units which is quite practical.

The current work describes the development of system on chip using fuzzy logic that has been applied for medical diagnostic applications. The system on chip under consideration uses fuzzifier, memory and defuzzifier for fuzzifying the patient data, storing the membership function values and defuzzifying the membership function values to get the output decision. However, for simplicity of design, the ASIC design of the has been considered for triangular-trapezoid membership functions, in spite of the fact that better results have been obtained for sigmoid membership functions [27]. In order to minimize the delay in transport of fuzzified patient data from the memory to the computational circuit and vice versa, the memory used for storing patient data has been designed to be on chip. The circuit to be designed involves a large number of functional blocks and minimizing the chip area as well as power delay product constitutes one of the important goals of the ASIC design. This has been made possible by using 8T full adders previously proposed by the authors in [29] as the building blocks of current design in place of the conventional 14T or 16T full adder designs.

The paper is organized as follows. "Functional Architecture of Smart Agent based medical diagnostic system" focuses on the functional architecture of the medical diagnostic system on chip. "Architecture of medical diagnostic system on chip" discuses the architectural design of the medical diagnostic system on chip. "Architecture of the fuzzifier" describes the architecture of the fuzzifier used for fuzzifying patient data. The transistor level design of the system on chip and results has been described in "Transistor level design of the system on chip".

Functional architecture of smart agent based medical diagnostic system

Figure 1 shows the generalized functional architecture of a smart system on chip used for medical diagnosis.

In Fig. 1, the smart agent is represented by a fuzzy system. At least two entities are required in this concept of diagnostics. The healthcare personnel who need not be physicians provide data by measuring the patients' health parameters. But for operating the system no health care personnel is needed. A simple village technician is good enough to operate the instrument and predict the health condition from the instrument's output leading to an early diagnosis of the condition of criticality of the patient. The smart instrument performs the diagnosis at regular times

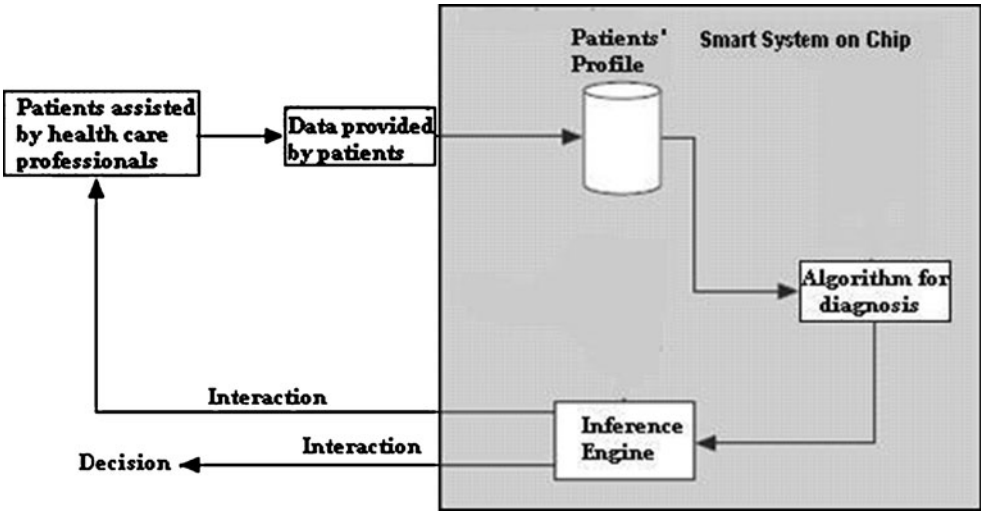

Fig. 1 Functional architecture of smart system on chip

and predicts future states of the patient using fuzzy logic. The instrument scans through the patients' profile that is stored in a patients' base. Based on previously fed data, the smart instrument can give an early signal of deterioration in the patient's health status and indicate an imminent emergency situation. Initially the data provided by the patients (in our particular case B.M.I., glucose, urea, creatinine, systolic and diastolic blood pressure) under the assistance of health care professionals is stored in a patients' profile. The data from the patients' profile is subjected to a diagnostic process using a knowledge base for diagnosis. The diagnosis process is based on fuzzification of patient data. The inference engine makes a prediction about the future physiological state of the patient based on the fuzzified data. The authors in their previous works [25–28] have already illustrated the details of the diagnosis algorithm and inferencing process. Based on the prediction, the smart system gives an indication about the possible next physiological state of the patient. Thus the system gives a decision about the approaching critical condition of the patient without the assistance of the physician. The role of the health care personnel is merely to enter pathophysiological data and the instrument uses fuzzy reasoning techniques to automatically infer about imminent health hazard of the patient. The authors in their previous works have proposed FPGA based medical diagnostic embedded system and already established the concept of diagnosis of patients with the help of smart system in absence of physician [25–28]. The proposed smart system actually makes a decision on approaching critical condition of patients on the basis of measured health parameters of the patients in accordance with the established medical norms. Any deviation from the normal course of decision that may be based on the experience and intuition of the medical practitioner is not possible in the smart instrument. Thus the role of an experienced medical doctor for diagnosing critical patients cannot be substituted by the smart instrument. However, using the diagnostic system, a diagnosing accuracy of up to 97.5% has been obtained.

Architecture of medical diagnostic system on chip

Figure 2 shows the architecture of the medical diagnostic system on chip.

Although the algorithms and architectures shown in [27, 28] yielded better results of accuracy of diagnosis, the current system on chip under consideration is based on the algorithm of diagnosis reported by the authors in [26] for the sake of simplicity of implementation.

The chip accepts patient data through the 8 bit input port *Data*. The different pathophysiological data being entered are Body Mass Index, glucose, urea, creatinine, systolic and diastolic blood pressure. These data are being recorded by the health care professionals using simple low cost instruments. The different input parameters to be entered are chosen in consultation with medical practitioners. If the data inputted are different from the accepted format, the instrument will not accept the data. On the other hand, if the values of data are entered wrongly it will result in erroneous decisions. Prior to entry of data, the chip is reset with the *Start* input. The system has been designed to store the data of multiple patients at the same time. The different patients are identified by patient id. This id is also used for consulting the patient profile in all future visits of the patient. The patient id is entered through 4 bit input port *ID*. The chip has been designed to be a small prototype only capable of storing only 100 patients' data. However, the concept can be extended to store a larger number of patients' data by increasing the capacities of internal memories. The entered data is fuzzified and the possibilities of low, moderate and high values of

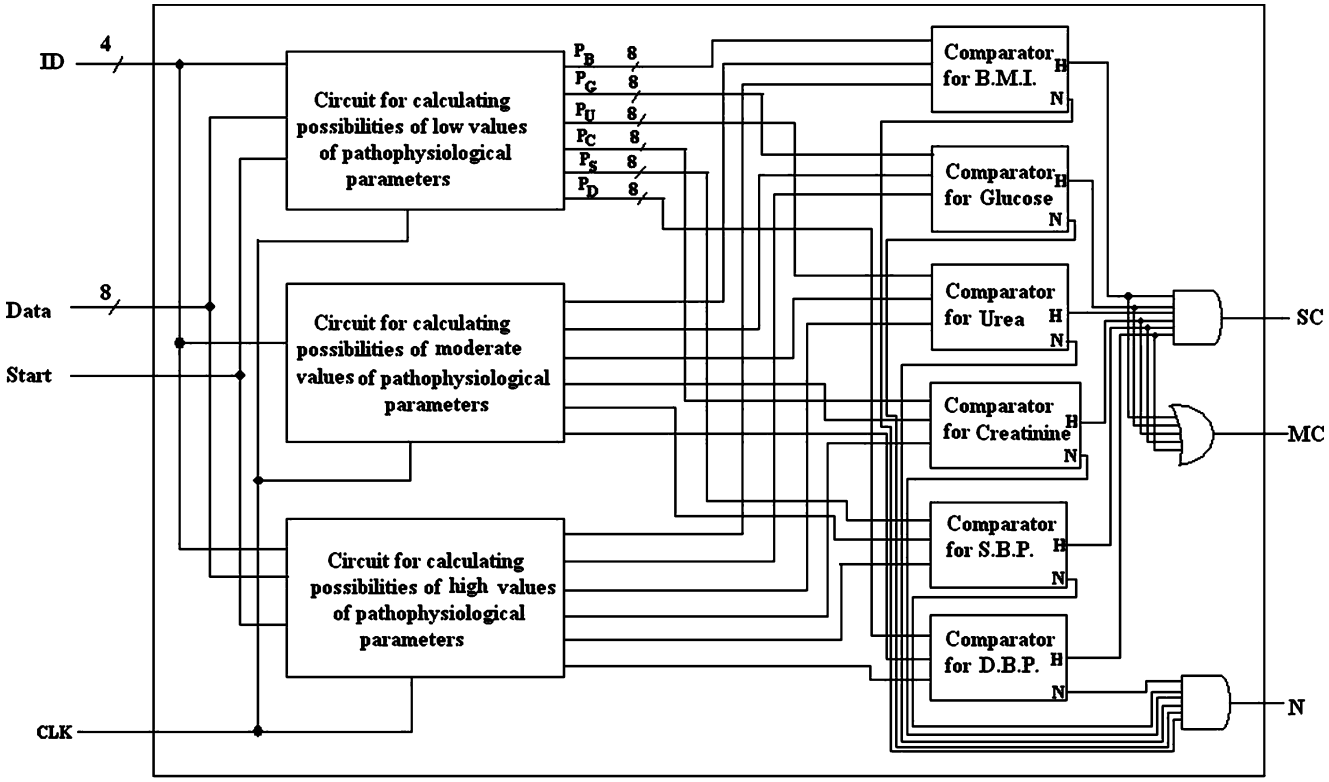

Fig. 2 Architecture of the medical diagnostic system on chip

different pathophysiological parameters viz. B.M.I., glucose, urea, creatinine, systolic and diastolic blood pressure is calculated using fuzzy logic using the circuit blocks shown in Fig. 2, which are again detailed in Fig. 3. The details of algorithms for fuzzification, inferencing and defuzzification have been specified in our earlier works [25–28]. Based on the possibility values, decision is taken whether the condition of patient is normal (N), moderately critical (MC) or severely critical (SC) using the comparators and the AND/OR gates. The comparators compare the high, moderate and low possibility values of different pathophysiological parameters. If the high values are greater than the other two, the comparators give a logic high output in H. If all the comparator outputs H are high then the SC output is high which indicates an approaching severe critical condition of the patient. The MC output (for moderately critical condition) is also high in that case but it is ignored. If some comparator outputs H are high, then MC is high but SC is low indicating an approaching moderately critical condition of the patient. When the moderate values are greater than the other two, the comparator outputs N are high. . If all the comparator outputs N are high then the N output is high which indicates a normal condition of the patient.

Figure 3 shows the architectural design of the circuit for calculating the low, moderate and high values of pathophysiological parameters.

Mode of operation of the circuit for calculating the possibility values of different pathophysiological parameters

Prior to entry of data, the *Start* input resets the *Address Counter* to "0000" and also the *Mod-6 counter* to "000". The value at the output of *Mod-6 counter* indicates the type of data to be entered. Table 1 shows the type of data identified for different outputs of *Mod-6 counter.*

The output of Mod-6 counter indexes into the four 6X3 SRAM blocks named *XA Mem, XB Mem, XC Mem* and *XD Mem*. Each of these memory blocks stores the threshold values of membership functions of the different pathophysiological parameters. The patient data are fuzzified using the fuzzifier circuits and the membership function values are stored in the 2KX12 SRAM blocks shown as *Memory* in Fig. 2. In order to minimize the delay in transport of fuzzified patient data from the memory to the computational circuit and vice versa, the memory used for storing patient data has been designed to be on chip which minimizes the delay of the circuit to a large extent. Each 12 bit word in the memory consists of most significant 8 bits storing the membership function values and least significant 4 bits storing the sequence number of the time instant of entry of data. The count of the sequence number is indicated by the address counter. Initially, the sequence number is taken same as the output of the *address counter.* As soon as the counter resets to 0000, the *decrementer* is

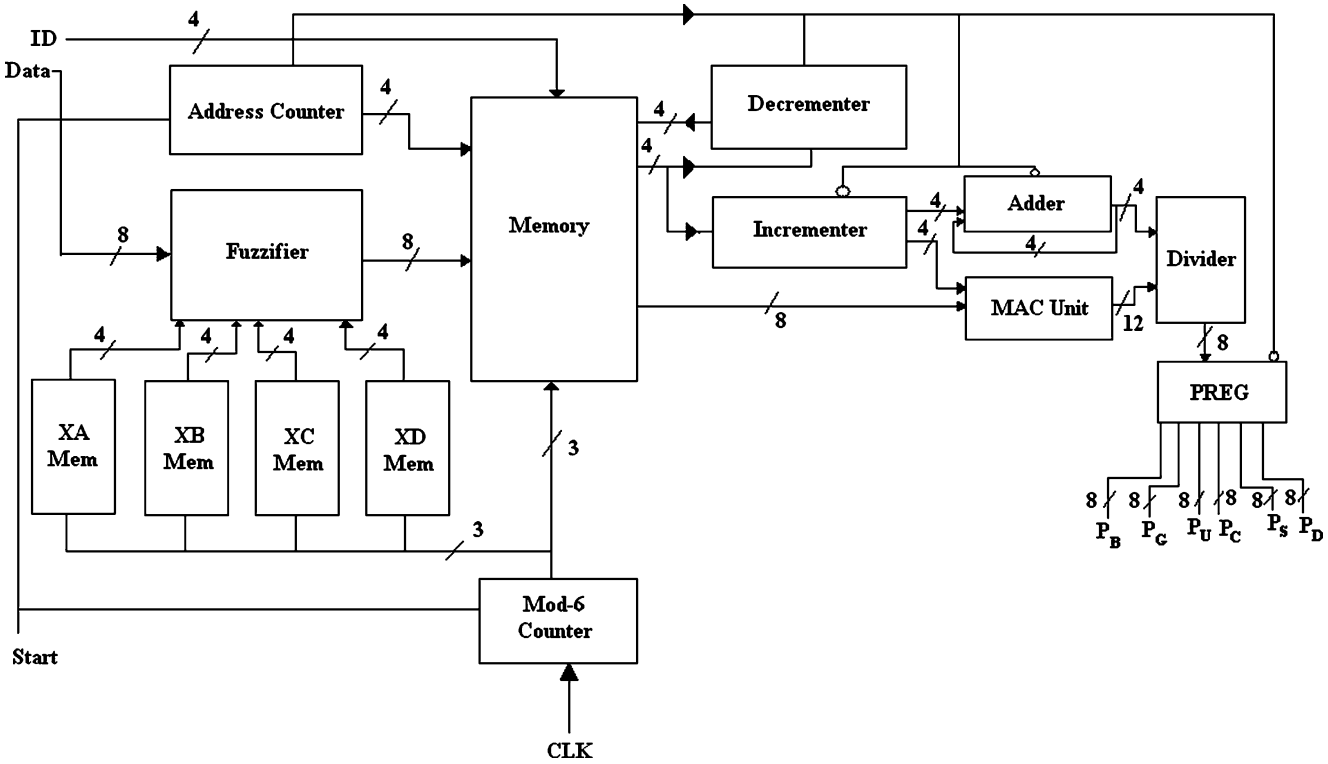

Fig. 3 Architectural design of the circuit for calculating the possibility values of different pathophysiological parameters

enabled and the *incrementer*, *adder* and *PREG* are disabled, so as to temporarily suspend any calculation of possibility values. The decrementer decrements the sequence number values by one so that the newly entered data that will enter into location xxxxxxx0000 will have the sequence number 1111. The idea is to give maximum weight to the most recently entered data, as has been established in [25–28]. The sequence number is incremented by one by the *incrementer* and the MAC Unit performs the time weighted summation $\sum_{i=1}^{n} i\mu(x)$, where $\mu(x)$ refers to the membership function value and i refers to the sequence number of the time instant at which the current set of pathophysiological data is taken. The divider performs the division $\frac{\sum_{i=1}^{n} i\mu(x)}{\sum_{i=1}^{n} i}$. The output of the divider is stored as current possibility value is the 6X8 SRAM block named as PREG. The comparators compare the current possibility values and indicate whether the condition of the patient is moderately critical (MC) or severely critical (SC). The design of the divider, comparator, MAC Unit, counters and memories are all based on standard circuits available in [30]. The architecture of the fuzzifier is shown below in "Architecture of the fuzzifier".

Table 1 Different types of data identified for different outputs of Mod-6 counter

Output of Mod-6 counter	Type of data
000	B.M.I.
001	Glucose
010	Urea
011	Creatinine
100	Systolic blood pressure
101	Diastolic blood pressure

Architecture of the fuzzifier

The fuzzifier has been designed considering shape of a generalized trapezoidal membership function. Trapezoidal and triangular (a special case of trapezoidal) membership functions have been chosen for fuzzification for the ease of implementation of the circuit since it is easier to implement the linear edges of trapezoidal membership functions compared non linear edges as in Gaussian or sigmoid membership functions. The shape of a generalized trapezoidal membership function is shown in Fig. 4.

The generalized trapezoidal membership function is defined in terms of four parameters X_A, X_B, X_C and X_D. As evident from Fig. 4, the universe of discourse of the input variable X is subdivided into five regions: region I ($X \leq X_A$) and V ($X \geq X_D$) are characterized by zero membership, i.e. $\mu_I(X) = \mu_V(X) = 0.0$. Region III ($X_B \leq X \leq X_C$) is characterized by full membership i.e. $\mu_{III}(X) = 1.0$. Region II and IV are characterized by membership functions

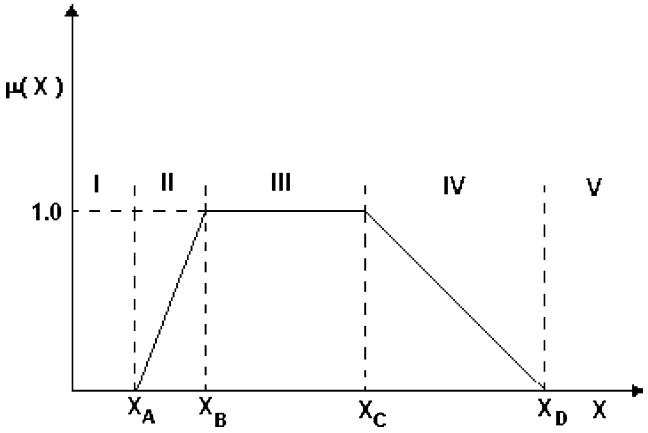

Fig. 4 A generalized trapezoidal membership function

taking values in the range $0.0 \leq \mu(X) \leq 1.0$. The membership functions in regions II and IV are defined by the equations:

$$\mu_{II}(X) = \frac{(X - X_A)}{(X_B - X_A)} \tag{1}$$

and

$$\mu_{IV}(X) = \frac{(X_D - X)}{(X_D - X_C)} = \frac{(X - X_D)}{(X_C - X_D)} \tag{2}$$

respectively. Equations (1) and (2) may be expressed as:

$$\mu_{II}(X) = S1.(X - X_A) \tag{3}$$

and

$$\mu_{III}(X) = S2.(X_C - X_D) \tag{4}$$

where $S1 = \frac{1}{(X_B - X_A)}$ and $S2 = \frac{1}{(X_C - X_D)}$ represent the slopes of the two oblique edges of the trapezium. In our specific example of renal diagnosis, the fuzzy sets for the moderate values of the different pathophysiological parameters absolutely represent the fuzzy set shown in Fig. 4. However, for the low fuzzy sets, regions I and II in Fig. 4 are assumed to be absent and for the high fuzzy sets, regions IV and V are assumed to be absent. Similarly, if the fuzzy set is a triangular fuzzy set with oblique edges, then region III is assumed to be absent. The architectural design of the fuzzifier is shown in Fig. 5. The fuzzifier is used for fuzzification of pathophysiological parameters used for medical diagnosis viz. B.M.I., glucose, urea, creatinine, systolic and diastolic blood pressure.

Parameters X_A, X_B, X_C and X_D are stored in four 8 bit registers. The input X, which represents the value of pathophysiological parameters, is fed to the four subtractors. The output of the subtractors consist of the differences $(X - X_i)$, (i=A, B, C, D) and the sign bit of the result. The sign bits $(Sgn(\Delta_i))$, (i=A, B, C, D) are assumed to be 1 if the difference is positive and 0 if the difference is negative (inverse of the normal convention being followed). The sign bits are fed to a priority decoder that has four outputs R_{I-V}, R_{II}, R_{III}, R_{IV}. Only one of the four outputs can be at logic high according to the truth table shown in Table 2.

The asserted output indicates the region in which the variable X falls. If R_{I-V} is asserted then $\mu(X)$ is assigned a value of 0.0 by the switch logic. If R_{III} is asserted, then $\mu(X)$ is assigned a value of 1.0 by the switch logic. If the R_{II} or R_{IV} is asserted, the membership is assigned a value given by the product $\mu(X) = M1 \cdot M2$. An 8×8 multiplier obtains the product. M1 is chosen to be equal to mantissa of S1 or S2 by the multiplexing logic accordingly as R_{II} or R_{IV} is asserted. S1 and S2 are chosen as 11 bit floating point numbers of which 3 bits are reserved for exponent and 8 bits for mantissa. The mantissa is given as input to the multiplier through the multiplexing logic. M2 is chosen to be equal to Δ_A or Δ_D accordingly as R_{II} or R_{IV} is asserted. The three bit exponent is used to control a shifter so that 8 bits out of 16 bits of the output of the multiplier is selected as an 8 bit fixed point value of $\mu(X)$ which is delivered to the output of the fuzzifier.

Transistor level design of the system on chip

As evident from the preceding discussion, the circuit to be designed is quite complicated and minimizing the chip area constitutes one of the important goals of the ASIC design. The transistor count has been minimized by proposing a new 8 transistor full adder in the present design which is based on the design of a three transistor XOR gate.

Design of three transistor XOR gate

The design of the full adder is based on the design of a new XOR gate. The proposed design of full adder uses three transistor XOR gates. The design of a three transistor XOR gate is shown in Fig. 6.

The design is based on a modified version of a CMOS inverter and a PMOS pass transistor. When the input B is at logic high, the inverter on the left functions like a normal CMOS inverter. Therefore the output Y is the complement of input A. When the input B is at logic low, the CMOS inverter output is at high impedance. However, the pass transistor M3 is enabled and the output Y gets the same logic value as input A. The operation of the whole circuit is thus like a two input XOR gate. However, when A=1 and B=0, voltage degradation due to threshold drop occurs across transistor M3 and consequently the output Y is degraded with respect to the input. The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of transistor M3. Specifically from

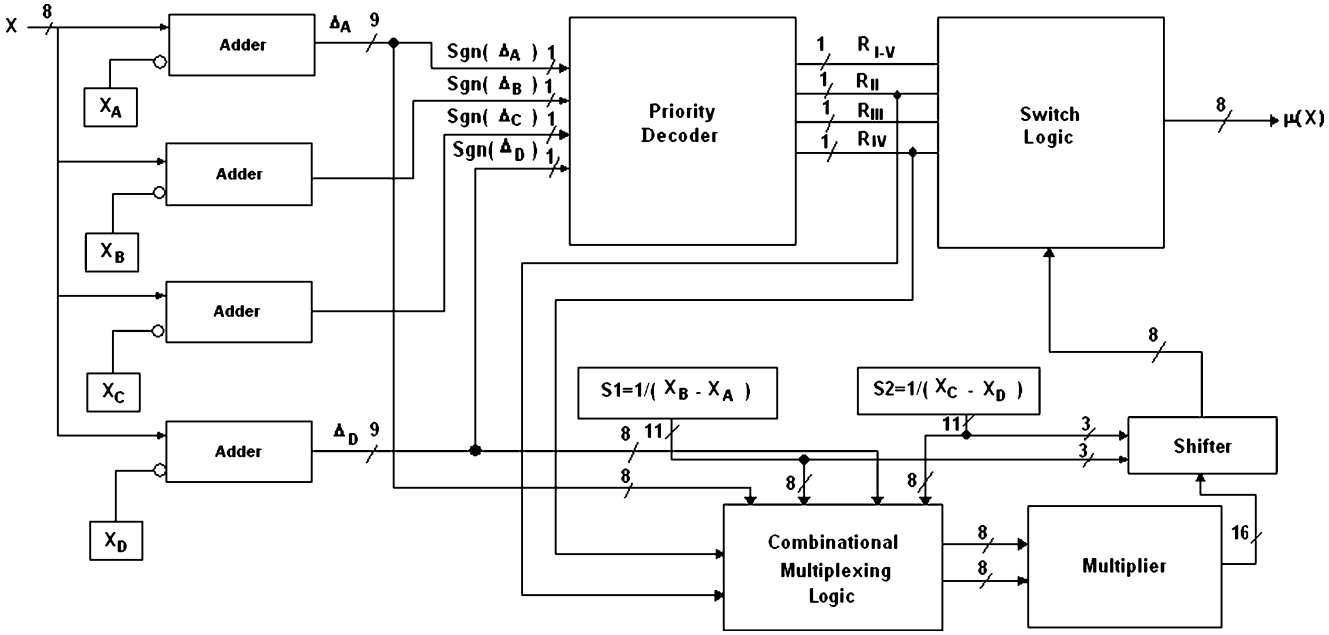

Fig. 5 Architectural design of the fuzzifier

[31], we find the following Eq. (5) that relates the threshold voltage of a MOS transistor to its channel length and width.

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + \phi_o} - \sqrt{\phi_o}\right) - \alpha_l \frac{t_{OX}}{L}(V_{SB} + \phi_o) - \alpha_v \frac{t_{OX}}{L} V_{DS} + \alpha_w \frac{t_{OX}}{W}(V_{SB} + \phi_o) \quad (5)$$

where V_{T0} is the zero bias threshold voltage, γ is bulk threshold coefficient, ϕ_o is $2\phi_F$, where ϕ_F is the Fermi potential, t_{OX} is the thickness of the oxide layer and α_l, α_v and α_w are process dependent parameters. From (5) it is evident that by increasing W it is possible to decrease the threshold voltage and therefore by increasing the width of transistor M3, keeping the length constant, it is possible to minimize the voltage degradation due to threshold voltage drop. The decrease of threshold voltage when the channel width of transistor M3 is increased has been studied in different technologies and shown in Fig. 7.

The absolute value of threshold voltage ($|V_{th}|$) of PMOS transistor M3 decreases from 0.661 V to 0.516 V when its W/L ratio is increased from 1/1 to 5/1 in 0.35 μm technology and also decreases from 0.267 V to 0.143 V when its W/L ratio is increased from 1/1 to 5/1 in 0.15 μm technology. Therefore, the voltage degradation due to threshold drop when A=1 and B=0, can be considerably minimized by increasing the W/L ratio of transistor M3.

A second problem of current feedback through transistor M1 also occurs when A=1 and B=0. The output of the pass transistor is fed back through transistor M1 which is operating in the active region since its gate has a logic high input. This difficulty can be overcome by decreasing the W/L ratio of transistor M1. With W=L, the channel resistance of transistor M1 amounts to 2.34 MΩ in 0.15 μm technology and 1.82 MΩ in 0.35 μm technology. With A=1 and B=0, the drain current through transistor M1 is 0.314 μA in 0.15 μm technology and 1.51 μA and this greatly limits the currents through it thereby minimizing the steady state power dissipation. The resistance can be further increased and the current can be further decreased by

Table 2 Truth table of the priority decoder

Inputs				Outputs			
$Sgn(\Delta_A)$	$Sgn(\Delta_B)$	$Sgn(\Delta_C)$	$Sgn(\Delta_D)$	R_{I-V}	R_{II}	R_{III}	R_{IV}
X	X	X	1	1	0	0	0
X	X	1	0	0	0	0	1
X	1	0	0	0	0	1	0
1	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0

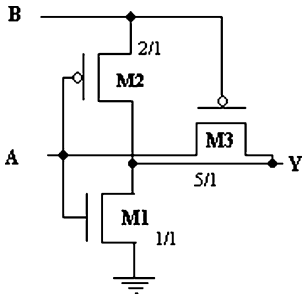

Fig. 6 Design of 3T XOR gate

further minimizing W/L ratio. For example with W/L=0.5, the drain current through transistor M1 is 0.157 μA in 0.15 μm technology and 0.755 μA in 0.35 μm technology. Typical values of W/L ratios for transistors M1, M2 and M3 are 1/1 (or 1/2), 3/1 and 5/1 respectively as shown in Fig. 6.

The detailed simulation and analysis of 3T XOR gate proposed by the authors have been shown in [29].

Design of 8T adder

We have proposed the design of an eight transistor full adder using novel three transistor XOR gates in [29]. The design of the three transistor XOR gate has already been described in the preceding section. The Boolean equations for the design of the eight transistor full adder are as follows:

$$Sum = A \oplus B \oplus Cin \tag{6}$$

$$Cout = BCin + CinA + AB = Cin(A \oplus B) + AB \tag{7}$$

The logic circuit of the full adder is shown in Fig. 8.

The OR gate can be realized using a wired OR logic [32]. The circuit diagram of the eight transistor full adder is shown in Fig. 9.

The sum output is basically obtained by a cascaded exclusive ORing of the three inputs in accordance with Eq. (6). The carry output is obtained in accordance with Eq. (7). The final sum of the products is obtained using a wired OR logic. The W/L ratios of transistors M1–M6 are same as the corresponding ones in Fig. 6. The W/L ratios of transistors M7 and M8 are taken as 5/1. It is quite evident from Fig. 8 that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain the carry output which obviously stands out to be smaller than the circuit shown in [33]. The design has been done using 0.15 μm and 0.35 μm technologies to establish the technology independence of the proposed design. The voltage drop due to the threshold drop in transistors M3 and M6 in Fig. 9 can be minimized by suitably increasing the aspect ratios of the two transistors. However, the threshold voltage drop of $|V_{T,p}|$ provided by the pMOS pass transistor M3 when a=0 and b=0 is used to turn on the nMOS pass transistor M8 and therefore we get an output voltage equal to $|V_{T,p}|-V_{T,n}$, where $V_{T,p}$ is the threshold voltage of the pMOS transistor and $V_{T,n}$ is the threshold voltage of the nMOS transistor. The difference value is very close to 0 V. Similarly, the threshold drop of the transistors M7 and M8 can be minimized by suitably increasing the aspect ratios of transistors M7 and M8. The detailed simulation and analysis of 8T full adder proposed by the authors have been shown in [29].

Layout design of the 8T full adder

The layout of the proposed 8T full adder has been designed and simulated. The designed layout using 0.35 μm technology using TSMC035 is shown in Fig. 10.

In order to make the layout symmetric, the big sized PMOS transistors have been laid on two n-wells with the NMOS transistors on the p type substrate in between. Moreover, since the interconnect density is low as evident from Fig. 10, itself, it also leads to a low power implementation of the adder [34].

Design of the different blocks of the circuit

The designed 8T adder has been used to implement the adders required in the fuzzifier. Apart from its use in adder design, the adder has been used to implement the 8×8 multiplier used in the fuzzifier. The other building blocks of the proposed SOC have been designed using standard architectures available in literature [30].

The 8×8 multiplier has been designed using the 8T full adder based on the standard architecture as specified in [30]. Multiplier architecture is essentially divisible into three stages: a partial product generation stage, a partial

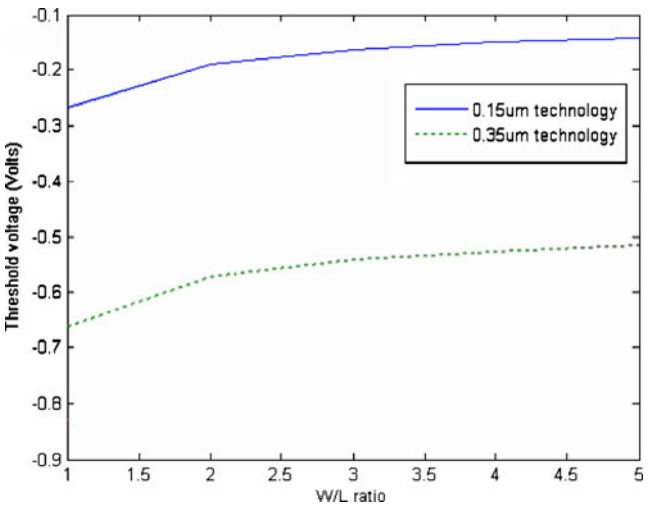

Fig. 7 Variation of threshold voltage with W/L ratio of PMOS transistor in different technologies

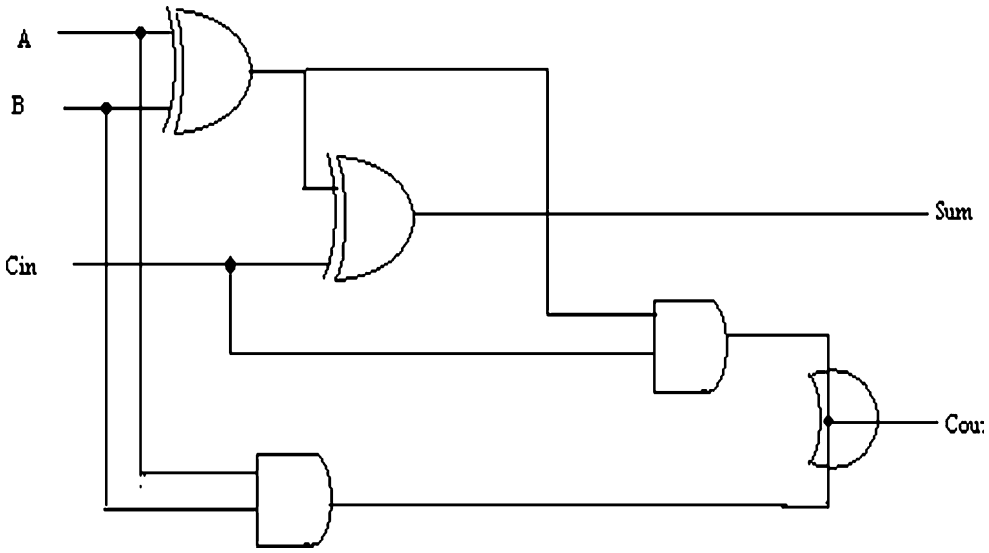

Fig. 8 Logic circuit of the full adder

product addition stage and final addition stage. Specifically in multiplication process, a considerable amount of time is wasted in partial product addition. Therefore speeding up the second stage and lowering its power dissipation are the most eminent means of achieving performance improvement of the multiplier [35]. The partial product addition is accelerated with the help 4–2 compressors. However, the standard 4–2 compressors available in literature make use of two cascaded full adders resulting in four XOR delays. J. Gu and C.H. Chang proposed the design of a 4–2 compressor using three XOR delays in [36]. Moreover, the carry bits are also generated in synchronism with sum generation unlike the standard 4–2 compressor. The current multiplier design makes use of the 4–2 compressor proposed by Gu et al. in [36].

The combinational multiplexing logic stated in Fig. 5 is essentially an array of eight 2×1 multiplexers. The 2×1 multiplexers have been designed using the two transistor implementation stated in [37]. The shifter has been designed to be a funnel shifter as specified in [30]. The priority decoder and switch logic have been designed using CMOS pass transistor logic using the truth table.

The memories XA, XB, XC and XD and the patient data memory stated in Fig. 3 have been implemented using six transistor static RAM cells. The incrementer circuit has been implemented using half adder circuit based on the standard design specified in [30]. Similarly the decrementer has been designed using half subtractor circuit using the design specified in [30].

Design of the whole circuit

Using the architectural schematic of the medical diagnostic system on chip shown in Figs. 2, 3 and 5, the transistor level schematic of the whole circuit has been designed as shown in Fig. 11.

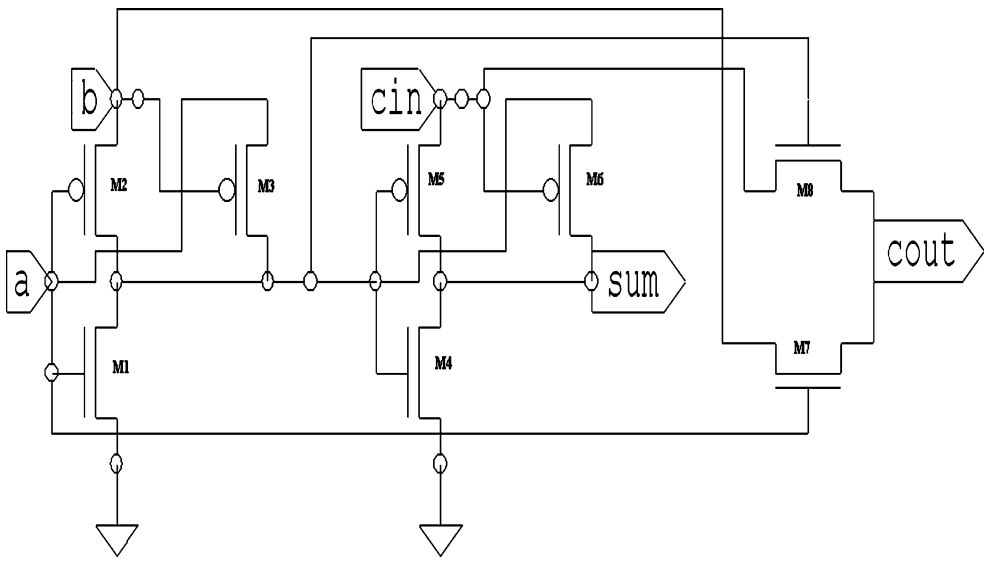

Fig. 9 Design of the eight transistor full adder

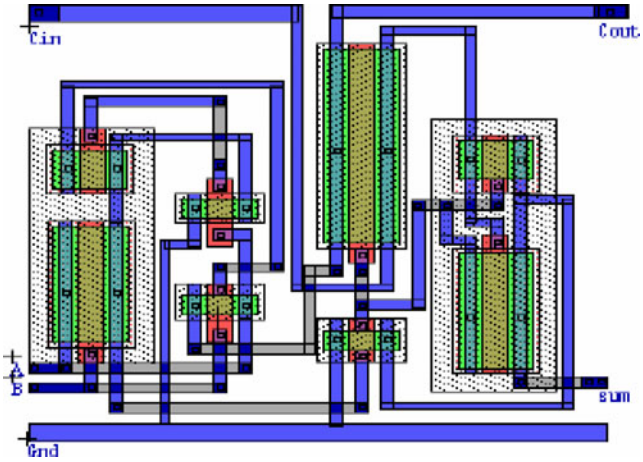

Fig. 10 Layout of the 8T full adder

The layout of the designed circuit is shown below in Fig. 12.

The entire circuit consists of 5,248 transistors and occupies a chip area of 76,148.48 μm^2. The transistor count is much low compared to a comparable design using 10T adders which required 6,364 transistors.

Simulation and results

The whole circuit has been designed using TSMC 0.35 μm CMOS process. The circuit has been simulated with TSPICE. Simulations have been performed with the individual components as also with the whole fuzzifier and the whole diagnostic system on chip. The power and delay analysis results are presented in Table 3.

The results indicate a low value of the power dissipation and delay of the proposed fuzzifier circuit. The whole fuzzifier circuit is found to have a delay of only 0.4 ns which is superior in performance compared to the one

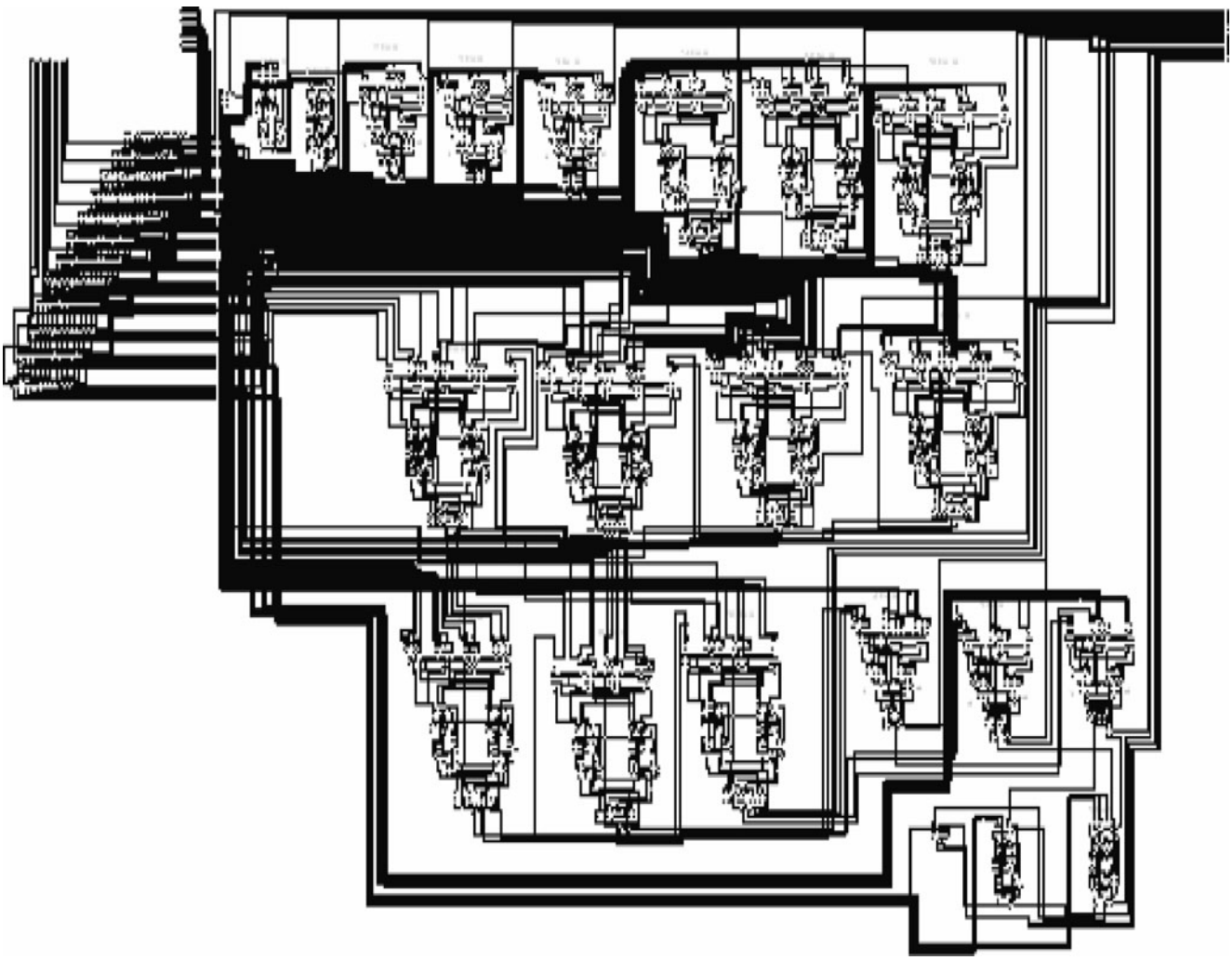

Fig. 11 Transistor level schematic of medical diagnostic system on chip

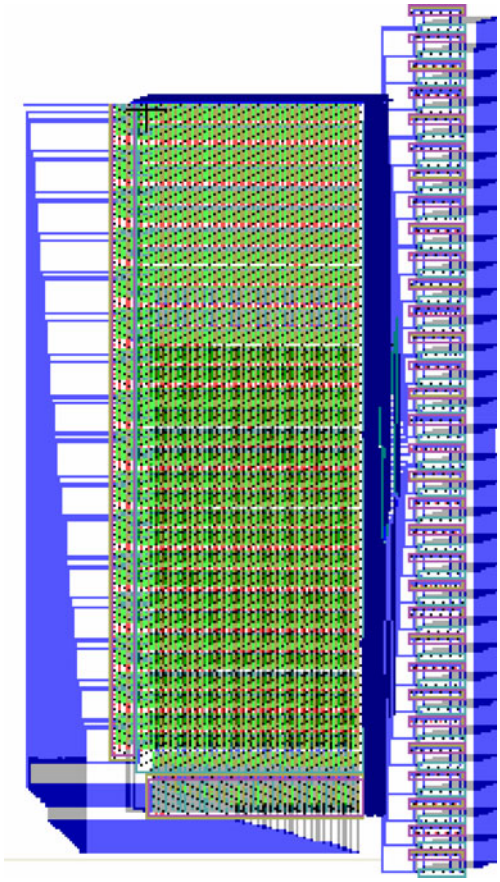

Fig. 12 Layout design of the medical diagnostic system on chip

reported in [38] that has a delay of 15 ns. The average power dissipation of the fuzzifier is around 80 mW which is better than the reported result of 186 mW [39]. Post layout simulation of the whole circuit indicates a delay of 13.27 ns and the average power dissipation of the system on chip is 123.49 mW.

Performance comparison with an FPGA based diagnostic embedded system

The performance of the proposed medical diagnostic system on chip has been compared with that of a comparable FPGA based diagnostic embedded system. The authors in their previous works have proposed FPGA based medical diagnostic decision making embedded systems. The power dissipation and delay posed by the developed system on chip has been compared with delay of the previously reported FPGA based embedded systems performing the same function and shown below in Table 4.

The results of comparison show that the proposed medical diagnostic system on chip dissipates much less power and has much less delay and hence much less power delay product than the comparable FPGA based embedded systems 1 and 2 reported in [26, 27]. The huge minimization in delay is attributed to the huge minimization of delay using system on chip architecture, since the on chip interconnect delays are few hundredths of off chip on board interconnect delays [40]. This also elucidates the benefit of deploying the proposed diagnostic system on chip in the rural health care centres of third world countries where economy of power and bulk data processing in view of scarcity of physicians are the matters of prime concern.

Results of patient data

The system is then tested with data of 80 patients to ascertain the accuracy of diagnosis. Simulation has been carried out with the data in the binary fixed point format. To show the applicability of the system and the diagnostic algorithm, the data of a sample patient of age 42 years has been analyzed and shown in the paper in Table 5.

Using these data, the system computes the membership function values using the membership functions of the different pathophysiological parameters described in [25–28]. The membership function values obtained at different instants of time is shown in Table 6.

In the above table, μ_L, μ_M and μ_H refers to the membership function values for low, moderate and high values of different pathophysiological parameters. From the above table, we come to know that the patient attains a critical condition when $\mu_H=1$ for all parameters. This happens at time T10.

Table 3 Power and delay of different blocks of the proposed medical diagnostic system on chip circuit

Block	Average power dissipation	Delay
Adder	8.4 μW	0.3 ns
Priority decoder	1.2 mW	27.21 ps
Combinational logic	2.74 mW	9.622 ps
Shifter	1.04 mW	1.83 ps
Multiplier	75.8 mW	0.685 ps
Router	7.1 mW	4.21 ps
Comparator	6.1 μW	31.25 ps
Memory	8.1 μW	0.4 ns
PREG	2.3 μW	13 ps
MAC unit	7.68 mW	9.64 ns
Mod-6 counter	4.47 mW	8.74 ps
Address counter	6.23 mW	8.87 ps
XA Mem	1.25 μW	3.28 ps
XB Mem	1.27 μW	3.26 ps
XC Mem	1.23 μW	3.29 ps
XD Mem	1.24 μW	3.27 ps
Incrementer	3.4 μW	0.3 ns
Decrementer	3.7 μW	0.32 ns
Divider	7.21 mW	1.66 ns

Table 4 Performance comparison of the proposed SOC against FPGA based embedded system

Type of system	Power dissipation	Delay	Power-delay product
Embedded system 1 [26]	320 mW	0.292 μs	93.44 nJ
Embedded system 2 [27]	380 mW	0.24 μs	91.2 nJ
Proposed system on chip	123.49 mW	31.27 ns	3.86 nJ

Using these membership function data, the system computes the possibilities of low, moderate and high values of different pathophysiological parameters at different instants of time. Table 7 shows the possibility values of different parameters at different instants of time.

Bayesian analysis has been carried out on the population under study to estimate the reliability of the system. In order to estimate the reliability of diagnosis, the definitions of statistical terms used in [41] have been used. As follows from the application of Bayes' theorem, the predictive value of any diagnostic test is influenced by the prevalence among the tested population, and by the sensitivity and specificity of the test [42]. In our particular case, the total population under study was 80.

Bayesian analysis of patients' data

Let A be the number of patients where the diagnostic test yields a positive result and the patient really has a disease, B be the number of patients where the diagnostic test yields a positive result and the patient does not have a disease, C be the number of patients where the diagnostic test yields a negative result and the patient really has a disease and D be the number of patients where the diagnostic test yields a negative result and the patient does not have a disease.

Hence, (A+B+C+D)=40.

Therefore,

Sensitivity of diagnosis, $Se = \frac{A}{(A+C)}$

Specificity of diagnosis, $Sp = \frac{D}{(B+D)}$

False positive rate=1−Sp $= \frac{B}{(B+D)}$

False negative rate=1−Se= $\frac{C}{(A+C)}$

Accuracy of diagnosis $= \frac{(a+d)}{(a+b+c+d)} \times 100\%$

In our particular case, A=24, B=1, C=1, D=54.

Hence, $Se = 0.96$, $Sp = 0.98$, $1 - Se = 0.04$, $1 - Sp = 0.02$

Accuracy of diagnosis=97.5%

The result of Bayesian analysis yields a high accuracy of diagnosis by the proposed chip.

Conclusion

The chapter highlights the ASIC design of the medical diagnostic system on chip. The chip is designed to accept pathophysiological data of patients. The patient data is fuzzified and the membership function values are stored in memories and based on the membership function values, decision is taken as to whether the condition of the patient is normal, moderately critical or severely critical. Efforts have been made to minimize the delay of the circuit as far as possible by proposing a high speed 8T full adder in the present design, which shows a better speed than all the adder designs available in literature so far as our knowledge is concerned. Moreover, using 8T full adders, the designed system on chip required as low as 5,248 transistors for its implementation which is much low compared to a comparable design using 10T adders which required 6,364 transistors. This led us to an area efficient implementation of the circuit. Compared to an FPGA based embedded system which may have a projected cost of around 4,000 INR (including peripherals) the cost of the system on chip used for medical diagnostic applications may be around 1,500 INR amortized over a volume production of 100,000 units which is quite practical. Bayesian analysis has been carried out to ascertain the reliability of diagnosis

Table 5 Result of a sample patient of age 42 years

Time	B.M.I.	Glucose	Creatinine	Systolic blood pressure	Diastolic blood pressure
T1	27.97	120	1.0	128	87
T2	28.31	125	1.1	131	88
T3	28.57	128	1.2	132	90
T4	28.87	127	1.3	136	94
T5	28.61	128	1.4	137	96
T6	29.00	128	1.4	138	98
T7	29.17	128	1.4	139	98
T8	29.73	129	1.4	140	97
T9	30.15	129	1.8	140	100
T10	30.62	131	2.4	143	101

Table 6 Membership function values of different pathophysiological parameters

Time	Membership function values																	
	B.M.I.			Glucose			Urea			Creatinine			S.B.P.			D.B.P.		
	μ_L	μ_M	μ_H	μ_L	μ_M	μ_H	μ_L	μ_M	μ_H	μ_L	μ_M	μ_H	μ_L	μ_M	μ_H	μ_L	μ_M	μ_H
T1	0.00	0.50	0.50	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00
T2	0.00	0.17	0.83	0.00	0.50	0.50	0.00	1.00	0.00	0.00	1.00	0.00	0.00	0.90	0.10	0.00	1.00	0.00
T3	0.00	0.14	0.86	0.00	0.20	0.80	0.00	1.00	0.00	0.00	1.00	0.00	0.00	0.80	0.20	0.00	1.00	0.00
T4	0.00	0.11	0.89	0.00	0.30	0.70	0.00	0.95	0.05	0.00	0.67	0.33	0.00	0.40	0.60	0.00	0.60	0.40
T5	0.00	0.14	0.86	0.00	0.20	0.80	0.00	0.15	0.85	0.00	0.33	0.67	0.00	0.30	0.70	0.00	0.40	0.60
T6	0.00	0.10	0.90	0.00	0.20	0.80	0.00	0.20	0.80	0.00	0.33	0.67	0.00	0.20	0.80	0.00	0.20	0.80
T7	0.00	0.08	0.92	0.00	0.20	0.80	0.00	0.10	0.90	0.00	0.33	0.67	0.00	0.10	0.90	0.00	0.20	0.80
T8	0.00	0.03	0.97	0.00	0.10	0.90	0.00	0.05	0.95	0.00	0.33	0.67	0.00	0.00	1.00	0.00	0.30	0.70
T9	0.00	0.00	1.00	0.00	0.10	0.90	0.00	0.05	0.95	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00
T10	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00

Table 7 Possibility values of different parameters at different instants of time

Time	Membership function values																	
	B.M.I.			Glucose			Urea			Creatinine			S.B.P.			D.B.P.		
	P_L	P_M	P_H	P_L	P_M	P_H	P_L	P_M	P_H	P_L	P_M	P_H	P_L	P_M	P_H	P_L	P_M	P_H
T1	0.00	0.50	0.50	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00	0.00	1.00	0.00
T2	0.00	0.18	0.82	0.00	0.67	0.33	0.00	1.00	0.00	0.00	1.00	0.00	0.00	0.93	0.07	0.00	1.00	0.00
T3	0.00	0.14	0.86	0.00	0.70	0.30	0.00	1.00	0.00	0.00	1.00	0.00	0.00	0.87	0.13	0.00	1.00	0.00
T4	0.00	0.14	0.86	0.00	0.54	0.46	0.00	0.98	0.02	0.00	0.87	0.13	0.00	0.68	0.32	0.00	0.84	0.16
T5	0.00	0.13	0.87	0.00	0.33	0.57	0.00	0.70	0.30	0.00	0.69	0.31	0.00	0.55	0.45	0.00	0.69	0.31
T6	0.00	0.12	0.88	0.00	0.29	0.71	0.00	0.56	0.44	0.00	0.59	0.41	0.00	0.45	0.55	0.00	0.55	0.45
T7	0.00	0.11	0.89	0.00	0.26	0.74	0.00	0.44	0.56	0.00	0.52	0.48	0.00	0.36	0.64	0.00	0.46	0.54
T8	0.00	0.10	0.90	0.00	0.23	0.77	0.00	0.36	0.64	0.00	0.48	0.52	0.00	0.28	0.72	0.00	0.42	0.58
T9	0.00	0.07	0.93	0.00	0.20	0.80	0.00	0.29	0.71	0.00	0.38	0.62	0.00	0.23	0.77	0.00	0.34	0.66
T10	0.00	0.06	0.94	0.00	0.16	0.84	0.00	0.24	0.76	0.00	0.31	0.69	0.00	0.18	0.82	0.00	0.28	0.72

and a high diagnostic accuracy of 97.5% has been obtained. Further works need to be done to create an inference table so as to incorporate the different fuzzy inferences in diagnostic decision making.

Acknowledgements The authors would like to acknowledge the support lent by Ministry of Communications and Information Technology, Government of India for providing the necessary support to carry out the work.

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