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Detector and Readout Assembly and Characterization for the Simons Array

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Abstract

The Simons Array (SA) is a cosmic microwave background (CMB) polarization experiment comprised of three telescopes that will observe the CMB at 90, 150, 220, and 270 GHz with more than 22,000 Transition Edge Sensor (TES) bolometers. The cryogenic receivers inside each telescope are named POLARBEAR-2a, POLARBEAR-2b, and POLARBEAR-2c (PB-2a, PB-2b, and PB-2c, respectively). To allow for the large number of detectors, SA uses frequency-division multiplexing with multiplexing factor of 40. We describe the process developed to assemble the readout circuit repeatably for SA. After assembly, we characterize the readout circuit and TESs at cryogenic temperatures in a condition of negligible incident optical power. Impedances in the readout circuit bias our estimates of TES parameters, and we describe a method to account for this.

1 Introduction

The Simons Array (SA) is a cosmic microwave background (CMB) polarization experiment consisting of three telescopes in Chile's Atacama Desert [1]. SA is the successor to POLARBEAR-1 (PB-1), which deployed in the same location in 2012. Each of the SA telescopes will contain a cryogenic receiver called POLARBEAR-2a (PB-2a), POLARBEAR-2b (PB-2b), and POLARBEAR-2c (PB-2c), with a total of more than 22,000 Transition Edge Sensor (TES) bolometric detectors. This is a factor of 18 increase in detector-count relative to PB-1. To facilitate this, we have developed a readout scheme that allows us to bias forty TESs with a single pair of wires through frequency-division multiplexing [2,3]. Here, we describe the assembly and

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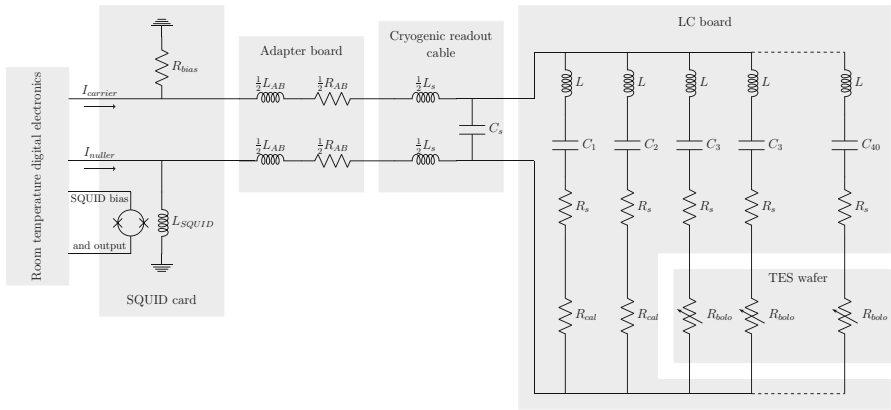
Fig. 1 The PB-2 readout circuit is shown with the physical locations of the circuit elements labeled in the shaded boxes. Each TES is biased with an AC tone, I_{Carrier}, in the range of 1.5–4.2 MHz, which is converted to a stiff voltage bias on the TES by the bias resistor, R_{bias}. A nulling current, I_{Nuller} is used to zero the current through the SQUID input coil, L_{SQUID}, and to minimize the SQUID's input impedance. Some sources of parasitic impedance are included in the schematic: L_{s} and C_{s} are the inductance and capacitance associated with the NbTi broadside-coupled stripline, respectively; R_{s} is the resistance associated with losses in the dielectric of the capacitor and contact resistance in the connector for that channel on the LC board; L_{AB} and R_{AB} are the inductance and resistance associated with the adapter board, respectively. Each bias circuit includes thirty-eight TESs (R_{bolo}) and two 1 Ω calibration resistors (R_{cal})

characterization of the cryogenic readout circuit for PB-2a and show results of TES characterization using this readout circuit.

A schematic of the PB-2a readout circuit is shown in Fig. 1. These circuit elements are located on five different pieces of hardware, indicated by the gray boxes. We have developed an assembly procedure for the cryogenic readout circuit that emphasizes modularity and repeatability. For information on the development of the individual hardware components, see [4,5].

We characterize the TES detectors and cryogenic circuit in-laboratory. We report a characterization of a PB-2a development TES wafer and deployment cryogenic circuit. The circuit creates a Thévenin equivalent resistance, R_{Th} in series with the TES, which both affects the TES performance and can bias our characterization. Here, we describe a method of measuring R_{Th} and removing its bias from the TES characterization. For a characterization of two recent TES batches that are likely to deploy with PB-2a and PB-2b, please see [6].

2 Assembly of DfMux Readout Circuit

The PB-2 cryogenic readout circuit consists of five pieces of hardware, listed in the first column of Table 1. In order to facilitate permutations of detectors and readout hardware, we have developed three modular assemblies called the SQUID (Superconducting Quantum Interference Device) card, the TES wafer, and the readout quantum. Each SA receiver needs seven TES wafers, 28 readout quanta, and 28 SQUID cards, so it is crucial that the assembly of these modules is repeatable. The assemblies undergo

Table 1 The five hardware components required to bias a TES wafer are listed in the first column. The LC board, cryogenic readout cable, and SQUID card have sub-components that are listed in the second column. Each LC board houses two LC chips, each of which has the forty inductors and capacitors. The cryogenic readout cable has two NbTi broadside-coupled striplines. Each SQUID card can house up to eight SQUIDs and eight bias resistors

| Components required to bias and read out a TES wafer		
Component	Sub-component	Quantity
TES wafer	–	1
Adapter board	–	4
LC board		15
	LC chip	30
Cryogenic readout cable		15
	Broadside-coupled stripline	30
SQUID card		4
	SQUID chip	30
	Bias resistor	30

shipping, handling, and thermal cycling, so they need to be robust to vibrations and stress. We focus here on the assembly of the readout quantum and the SQUID card and the interfaces between the three modular assemblies.

2.1 Readout Quantum

A readout quantum consists of three or four LC boards, an equal number of cryogenic readout cables, and one adapter board. A readout quantum with four (three) LC boards is called a large (small) readout quantum. Each LC board is soldered to a single cryogenic readout cable, and all of the readout cables are soldered to a single adapter board. Tin-lead solder alone does not adhere to NbTi, so we use a combination of ultrasonic solder and tin-lead eutectic solder [4]. Figure 2a shows the solder and strain relief on an LC board. A G10 clamp provides strain relief to the cryogenic cables. The strain relief clamp does not protect against the stress imposed by differential thermal contraction or vibrations during shipping, so we vet each solder connection by brushing it vigorously with a stiff brush. This has been an effective method to identify mechanically weak connections, which we preemptively repair in order to avoid failures during testing or CMB observations. Repair typically entails either reapplying solder or replacing the cryogenic readout cable.

2.2 SQUID Card

A total of four SQUID cards is needed to read out each TES wafer, with each card consisting of a printed circuit board and either eight (corresponding to a large readout quantum) or six (corresponding to a small readout quantum) SQUID chips. The printed circuit boards are assembled with surface-mount resistors, including the 30 mΩ bias
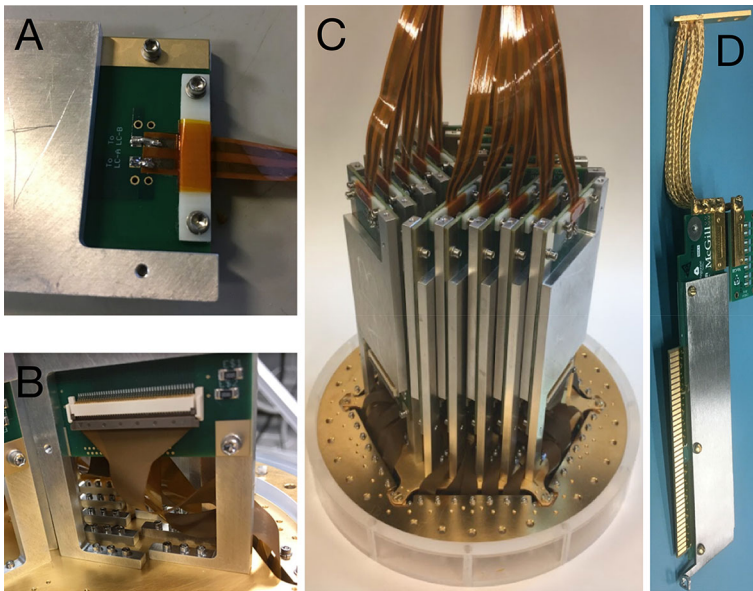
Fig. 2 **a** A cryogenic readout cable is soldered to an LC board and secured with a G10 clamp. **b** The electrical interface between the LC boards and the TES wafer is made with low-resistance ZIF connectors. **c** Fifteen LC boards are installed on a TES wafer. Each LC board has a cryogenic readout cable attached. **d** A gold-plated OFHC copper heat strap is attached to a SQUID card and an adapter board. The adapter board does not yet have readout cables attached (Color figure online)

resistor (R_{bias} in Fig. 1), at a commercial assembly facility. A thin square of niobium foil is then glued to the boards at each location where a SQUID chip will be placed. Each SQUID chip is individually mounted to the card in the center of a niobium foil square using rubber cement. During this mounting, pressure is applied to the chips in the corners that do not contain areas designated for wire bonding or SQUID elements in order to ensure adhesion. After all eight chips have been mounted to the board, they are then wire-bonded. Finally, a magnetic shield which surrounds the SQUID card is installed. An image of a fully assembled SQUID card is shown in Fig. 2d.

2.3 Interfaces

LC boards are mounted to the back of the TES wafer and connected electrically with low-resistance Zero Insertion Force connectors ($\sim$ 15 mΩ contact resistance) (Fig. 2b, c). Each TES wafer requires fifteen LC boards, so we use three large readout quanta and one small readout quantum per wafer. After LC installation, we install a low-emissivity, gold-plated oxygen-free high-conductivity (OFHC) copper can that surrounds the LC boards and provides radiative shielding and mechanical support.

Mating low-impedance micro-D connectors are used to connect the adapter board and SQUID card. These connectors have contact resistance of 26 mΩ and inductance of 20 nH. A gold-plated OFHC copper strap is used to provide a thermal path between the 4 K cryostat walls, the SQUID card, and the adapter board (shown in Fig. 2d).

3 Characterization of Cryogenic Circuit and TES Bolometers

Before fielding our detector and readout assemblies, it is critical to perform in-laboratory characterization to ensure that the hardware meets our specifications. This is a description of the typical testing that we perform in a non-optical cryostat. This in-laboratory characterization was performed using a development PB-2a wafer in a test cryostat at the University of California, San Diego, using observation-ready digital readout electronics at room temperature [7]. The cryostat is cooled with a Pulse Tube Cryocooler and a ^{3}He/^{4}He evaporation refrigerator and has three stages with temperatures of 3 K, 350 mK, and 270 mK. The 270 mK stage is used to cool the TES array and the LC boards and is referred to as the bolometer stage. The 350 mK stage is used as a thermal intercept for cryogenic readout cables and thermometry cables that are connected between the bolometer stage and the 3 K stage. The temperature of the bolometer stage can be manipulated by applying power to the ^{3}He adsorbing charcoal heater using a Proportional–Integral–Derivative control loop. Please see [6] for a characterization of two recent PB-2 TES wafer batches.

To find the resonances of the bias circuit, we perform a network analysis by injecting tones into the circuit while the bolometer stage is cooled to 270 mK, below the TES transition temperature, and measuring the current driven through the SQUID input coil. The injection point is either the carrier or the nuller path, and the resulting measurements are referred to as a carrier network analysis and a nuller network analysis, respectively. The resonant frequencies of the carrier and nuller network analysis are affected by the inductance of the SQUID input coil, but this inductance is nulled in actual TES operation. The ratio of a carrier network analysis to a nuller network analysis approximates a network analysis of the bias circuit without the SQUID input coil. We refer to this ratio as a DAN network analysis, shown in Fig. 3. Each peak corresponds to an LC resonance, and we see forty peaks in this DAN network analysis, indicating perfect yield. A known error in the LC chip design, which has been fixed for PB-2b and PB-2c, causes the two highest frequency peaks to overlap. We choose the frequencies of highest admittance to bias the TESs. The two heavily damped resonances at ~ 2.1 MHz and ~ 2.7 MHz correspond to the 1 Ω calibration resistors which do not superconduct.

We can measure the TES normal resistance, critical temperature and the Thévenin equivalent series resistance, R_n, T_c, and R_{Th}, respectively, by measuring the TES resistance as a function of its temperature. To perform this measurement, we apply a small voltage bias of about $0.1 \mu V$ to each TES simultaneously and record the amplitude and phase of the resulting current while manipulating the temperature of the bolometer stage. We sweep up and down in temperature to investigate hysteretic behavior. $R(T)$ curves from ten multiplexed channels are shown in Fig. 3. The low-temperature resistance is nonzero because of non-superconducting impedance in the readout circuit and is characteristic of a Thévenin equivalent resistance in series with each TES. Each TES has a unique R_{Th} because: (1) R_{Th} has a contribution from frequency-dependent stray impedances, and (2) there is a unique stray resistance associated with each capacitor in the LC filter [5]. A histogram of R_{Th} for a set of multiplexed detectors is shown in Fig. 3c. We use this measurement of R_{Th} to calibrate our other TES measurements.
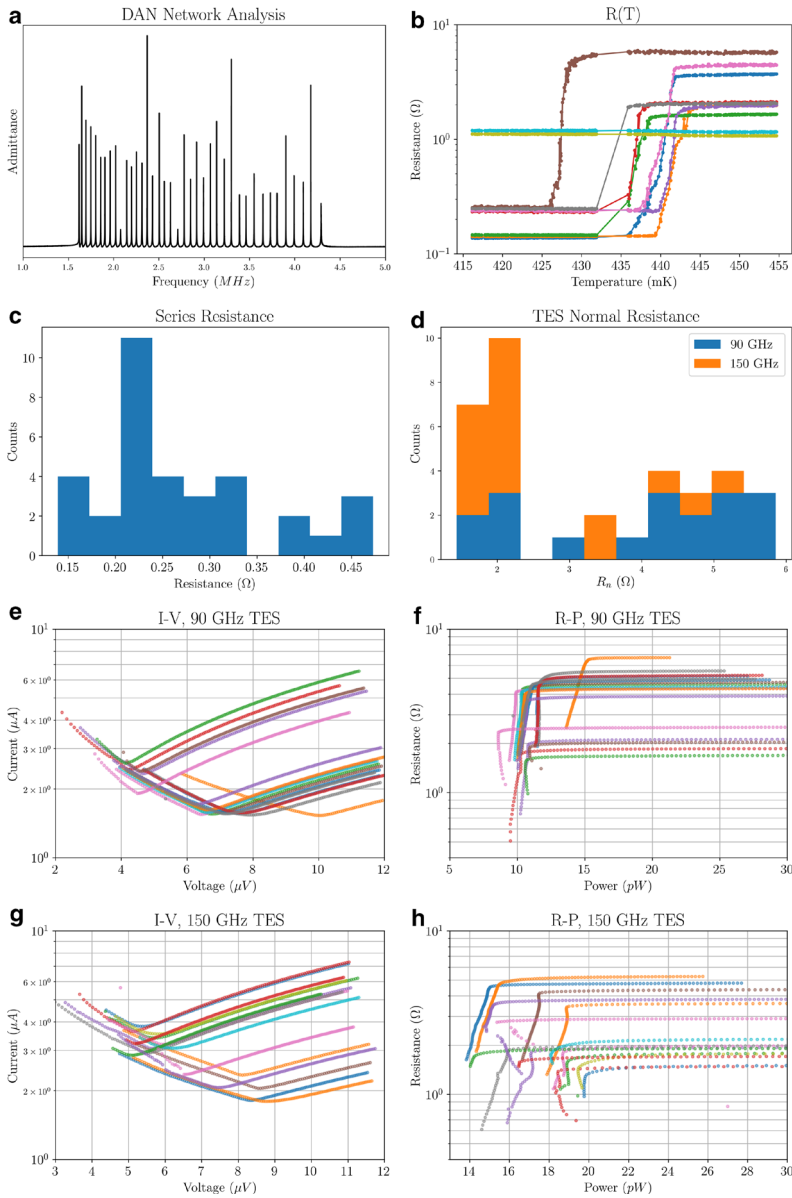
Fig. 3 The results of the measurements described in Sect. 3 are plotted here. Each plot is labeled with the respective measurement name. **a** DAN network analysis. **b** $R(T)$ for ten multiplexed TESs. The low-temperature resistance is nonzero due to a Thévenin series resistance. Data were cut in 432–437 mK range due to an unintentional abrupt temperature change. **c** A histogram of the series resistance for a multiplexed set of detectors. **d** The normal resistance for a set of multiplexed detectors. The normal resistance is calculated using Eq. 1 to account for the bias due to series resistance. **e–h** $I–V$ and $R–P$ curves for a set of multiplexed detectors. These measurements were corrected for the bias induced by series resistance using Eq. 2 (Color figure online)

R_{Th} induces an additive bias in our TES resistance measurement, which we subtract to retrieve the TES resistance:

$$R_{\mathrm{bolo}} = R_{\mathrm{measured}} - R_{\mathrm{Th}}. \tag{1}$$

We define R_{n} as the high-temperature ($\sim 500\,\mathrm{mK}$) TES resistance and T_{c} as the temperature at which the TES resistance is 80% of R_{n}.

Because this characterization is done in a dark cryostat, we know how much optical power is being deposited on the TES (i.e., none). This allows us to measure the TES saturation power, P_{sat}, by varying the electrical power on the TES. As a proxy for P_{sat}, we typically measure the power at the turnaround of the TES I–V curve, P_{turn}. The turnaround is defined as the point at which $\mathrm{d}I/\mathrm{d}V = 0$. P_{turn} and P_{sat} usually vary by only 5–10%, and P_{turn} can be found more robustly in TESs with varying properties. To measure the TES I–V curve, we apply a large amplitude voltage bias to a multiplexed set of TESs while the bolometer stage is above the TES transition temperature. We then lower the bolometer stage temperature to $270\,\mathrm{mK}$ while Joule heating keeps the temperature of the TESs above T_{c}. After the bolometer stage temperature has stabilized, we decrease the voltage bias while measuring the amplitude and phase of the current through the SQUID input coil, I_{SQUID}. The series impedance, R_{Th}, creates a voltage divider with the TESs and biases our measurement. To account for this, we subtract the voltage dropped across the stray resistance from the bias voltage,

$$V_{\mathrm{TES}} = V_{\mathrm{bias}} - I_{\mathrm{SQUID}} \times R_{\mathrm{Th}}, \tag{2}$$

where V_{bias} is given by

$$V_{\mathrm{bias}} = I_{\mathrm{carrier}} R_{\mathrm{bias}}. \tag{3}$$

When calculating P_{turn} from the I–V measurement, we use the corrected voltage, V_{TES}. I–V measurements for thirty-eight multiplexed TESs are shown in Fig. 3e–g. From the I–V curve, we can calculate the resistance and power at each point in the transition. A plot of resistance vs. power is also shown in Fig. 3f–h.

The spread in TES properties between detectors shown here is much larger than our requirements and much larger than the spread in more recently fabricated TES wafers. A thorough characterization of two recent TES wafer batches that are likely to deploy in PB-2a and PB-2b has been published recently, and the interested reader is referred to [6].

4 Conclusions

SA will map the polarization of the CMB at 90, 150, 220, and 270 GHz using polarization-sensitive TES bolometers and frequency-division multiplexed readout. This readout scheme allows us to bias forty cryogenic detectors with a single pair of wires. The cryogenic readout hardware has been assembled into three modular packages, allowing for permutations of hardware while preparing to field the SA instruments. We have demonstrated the characterization of TESs and the cryogenic

readout circuit in a dark test cryostat. Series impedance in the readout circuit can bias our measurements of TES parameters, but the series impedance can be measured and its bias removed.

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