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An 84 Pixel All-Silicon Corrugated Feedhorn for CMB Measurements

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Abstract Silicon platelet corrugated feedhorn arrays for cosmic microwave background (CMB) measurements at millimeter wavelengths (130 GHz to 170 GHz) have been developed for deployment for the polarization-sensitive upgrade to both the Atacama Cosmology Telescope (ACTpol) and the South Pole Telescope (SPTpol). We present fabrication developments and the first results of a prototype monolithic feedhorn array consisting of 84 horns. Measurements at room temperature show good beam quality across the needed bandwidth, return loss of <-20 dB, an insertion loss of <-0.4 dB, and cross polarization of <-23 dB. The 32 platelets were aligned to a 1σ variation of 8 μm.

Keywords Observational cosmology · Millimeter wavelength optics · MEMs · Microwave feedhorns

1 Introduction

Silicon platelet corrugated feedhorn arrays for cosmic microwave background (CMB) measurements at millimeter wavelengths (130 to 170 GHz) have been developed and

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are being manufactured for deployment in the polarization-sensitive upgrade to the Atacama Cosmology Telescope [1] (ACTpol) as well as the polarization-sensitive upgrade to the South Pole Telescope [2] (SPTpol). We present the first results of a prototype monolithic feedhorn array consisting of 84 horns. Corrugated feedhorns allow for a wide bandwidth (>25%), low side lobes (<−30 dB), and low cross-polarization (<−30 db) [3]. In addition to the excellent microwave properties, an all-silicon feedhorn has low thermal mass and thermal contraction matched to silicon based detectors, and can take advantage of the significant advantages that photolithography affords. Specifically, photolithography enables precise control (<5 μm) of both feature sizes and locations over a large area. This precision guarantees tight tolerances for layer-to-layer alignment within the feedhorn stack as well as to the detector wafers through the use of alignment pins in photolithographically defined alignment holes.

Previous results have shown that a single feedhorn can be made out of silicon and show microwave properties similar to commercially available horns [4, 5]. This paper introduces results from an 84 pixel feedhorn array fabricated from 100 mm diameter silicon wafers.

2 Method

Silicon platelets for feedhorn arrays have been fabricated at the NIST Quantum Fabrication Facility in Boulder, CO on 100 mm diameter substrates. For the prototype feedhorn array, 32 individual platelets with 84 pixels each were fabricated, aligned, and plated with Cu/Au. Figure 1 shows the profile used for the prototype platelet array, details of which can be found in Ref. [5]. The square waveguide is needed to provide single-modded operation over the detection bandwidth. To produce a large number of platelets, a robust manufacturing process with high yield and low defects has been developed. An overview of the process has been given in Ref. [5]. A silicon wafer (double-sided polished, 0.001 Ω cm–0.004 Ω cm resistivity, ⟨100⟩ orientation, and 500 μm thick) is wet-oxidized to grow a silicon dioxide film 0.8 μm thick. A combination of two masks, one an oxide and the other photoresist, allow for two silicon-etching steps.

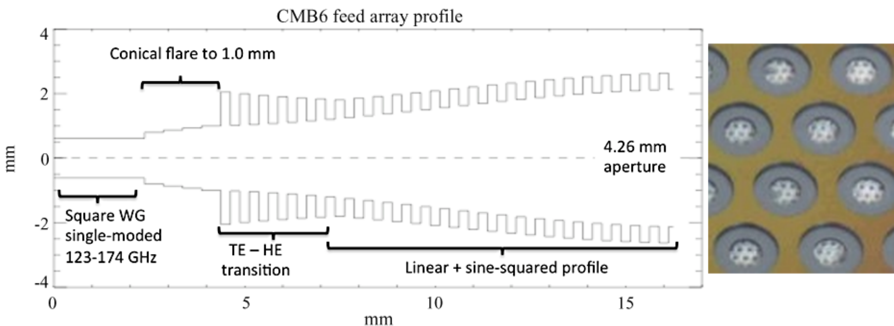

Fig. 1 (Color online) Feedhorn profile for a 32 platelet array on left and close-up of a single wafer in TE-HE transition on the right showing the dual radius corrugations

As in any photolithography process, proper control of the surface chemistry is critical. This is especially important for the HF etch when the 1 μm photoresist is masking the silicon dioxide. If the 1 μm photoresist is not well adhered to the silicon dioxide, the HF can propagate between the silicon dioxide and photoresist, causing poor sidewall transition widths. If well adhered, the sidewall width may be as small as 1.5 μm for the 0.8 μm thick silicon oxide layer.

To provide well-adhered photoresist, a wafer is cleaned for 30 minutes in 70°C N-Methylpyrrolidone (NMP), rinsed, and dried. Within one hour a hexamethyldisilazane (HMDS) adhesion promoter is applied at 4000 rpm and baked at 115°C for 90 seconds. Within another hour the 1 μm photoresist (Shipley SPR660[1]) is applied and baked. Timing is important in these two steps to provide a clean and consistently prepared wafer surface to maximize both adhesion and process repeatability. The photoresist is then exposed, developed, inspected, and is now ready for the HF etch.

After the wafer has the hard mask etched into the silicon dioxide, a 3 μm photoresist (Shipley SPR220-3 (see footnote 1)) is applied, exposed, and developed. After inspection, the wafer is etched in a deep reactive ion etch (DRIE). The DRIE utilizes the Bosch process to form nearly vertical sidewalls with excellent mask selectivity [6]. After etching, the wafer is rinsed in acetone to remove the photoresist and then put in an ultrasound to help remove passivation material that is not well adhered to the sidewalls. A solvent (Dupont EKC-265 (see footnote 1)) is used to remove the passivation material deposited during the DRIE etch. The EKC-265 is heated to 70°C and the wafer kept in the solvent for 4 hours.

After the wafer is rinsed and dried, a roll-on photoresist (Dupont MX5020 (see footnote 1) is applied to the backside of the wafer to protect the etcher's chuck. A second DRIE is applied to the wafer by use of the hard silicon dioxide mask to control the etch features. The second DRIE step is to etch the corrugation feature 250 μm into the 500 μm thick wafer. The depth of the corrugations are controlled by etch time. Etch uniformity is dependent on the etch pattern, but is typically 1–2% yielding a corrugation depth of 250 ± 5 μm. At the same time, features etched in the first DRIE propagate completely through the wafer. After the second DRIE step the parts are cleaned by use of NMP, acetone, and acetone ultrasound, and dried after an isopropanol rinse. Finally, the wafers are cleaned in EKC-265 and rinsed, and then the oxide is stripped in a final HF etch. Figure 2 (left) shows finished platelets before the final HF etch.

Finished platelets are then individually metalized, aligned, bonded and finally the assembled stack is electroplated. The seed layer is sputtered Ti (200 nm) followed by Cu (1 μm) at 20 Torr. The goal is to cover all surfaces of the individual platelets with a metallic film that will provide good adhesion and a solid seed layer for subsequent electro-plating. Alignment of the stack is performed in a clean room with alignment pins in designated photolithographically defined holes. The 2.5 mm alignment holes are oversized from alignment pins by 10 μm in diameter. Alignment of the prototype

[1]Products or companies named here are cited only in the interest of complete technical description, and neither constitute nor imply endorsement by NIST or by the US government. Other products may be found to serve just as well.

Fig. 2 (Color online) Finished platelets before final HF etch (*left*) and finished feedhorn array after plating (*right*). The finished array is ∼55 mm wide and the wires (on *right*) are used to connect the feedhorn to the cathode during plating, and are subsequently removed

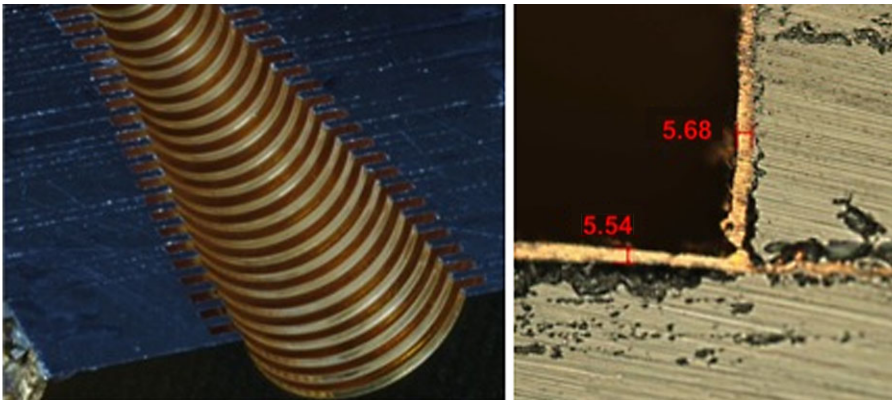

Fig. 3 (Color online) Finished single-pixel feedhorn (from Ref. [3]) was diced (*left*) and inspected (*right*) for Cu/Au coverage. Units for red measurements in the right are in μm. Note that the metallization extending to the *right* in the *right figure* is the Ti:Cu seed layer that extends between the platelets

array to <8 μm standard deviation was achieved. Figure 2 (right) shows the finished prototype array after plating.

3 Results and Discussion

Previous work has shown good microwave performance of a single pixel silicon platelet feedhorn [4]. However, direct verification of plating coverage had not been previously reported. This single-pixel silicon-platelet feedhorn has been diced and diamond-lapped to check the coverage (Fig. 3.) Based on a survey of all the corrugations in this feedhorn, we find the plating coverage to be uniform (6 μm ± 1 μm) and to have only a very few 5 μm to 30 μm defects in coverage.

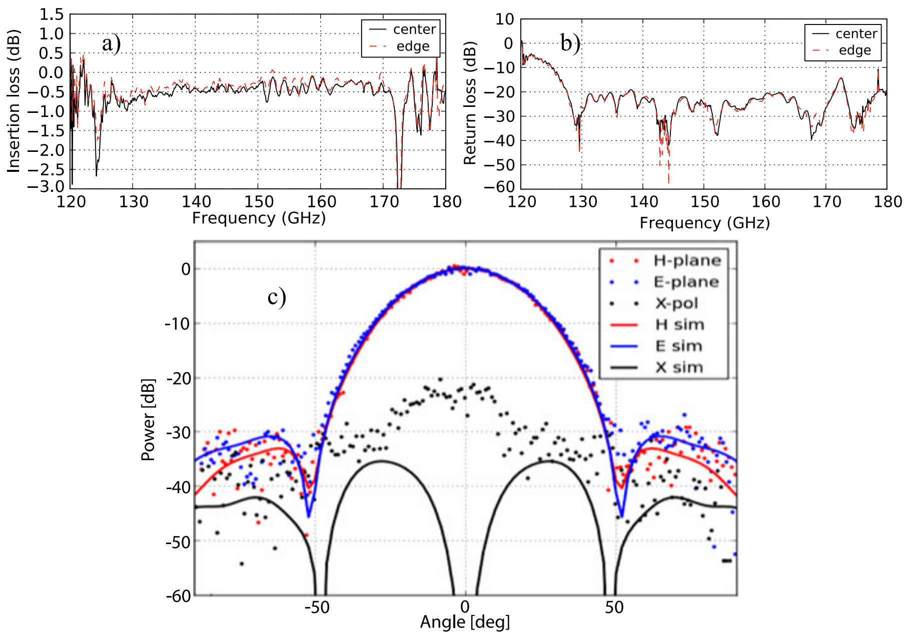

Fig. 4 (Color online) Insertion loss (**a**) and return loss (**b**) measurements of a center (*solid black*) and edge (*dashed red*) pixel. A beam map (**c**) at 150 GHz is shown for a center pixel with the E-plane (*blue*), H-plane (*red*), cross-polarization (*black*), data (*dots*), and modeling (*solid lines*)

When the final array was plated, a single wafer that had undergone the same processing was included. This witness wafer showed good Cu:Au coverage and excellent adhesion.

Vector network analyzer (VNA) measurements were made on the finished feedhorn array. The experimental setup for the VNA measurements has been presented previously [5]. The insertion loss (Fig. 4a) and return loss (Fig. 4b) have been measured on a center and an edge pixel to determine uniformity of the feedhorn array. Figure 4c shows the beam map for a center pixel. Over the 120 to 170 GHz band the average return loss was measured to be <-20 dB, and the insertion loss was <-0.4 dB. Insertion loss was measured at room temperature and is expected to be less lossy at cryogenic temperatures. Beam maps were made at 150 GHz and showed a symmetric beam with low cross polarization of <-23 dB and side lobes that are <-30 dB.

To test the cryogenic robustness of the feedhorn array, room temperature return loss and insertion loss measurements were made after seven thermal cycles to 4 K. They showed no deviation from the pre-cycled data.

4 Conclusion

We have presented the fabrication developments and measurements for a monolithic 84 pixel all-silicon feedhorn array. The measurements demonstrate that the silicon-

platelet corrugated feedhorn provides performance comparable to that of conventional all-metal devices. The wafer substrates used for this array were 100 mm in diameter. Development to transfer the 100 mm substrate process to a 150 mm substrate process has been completed successfully. A 12-wafer stack with multiple corrugated waveguide sections and a $\lambda/2$ corrugation depth has been fabricated and plated. Measurements show a waveguide loss of 0.3 dB/cm at room temperature for 150 mm wafer diameters.

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