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Strategies for dislocation density reduction in CdTe epilayers grown directly on (211) Si substrates using MOVPE

M. Niraula[1,*], B. S. Chaudhari[1], R. Okumura[1], and Y. Takagi[1]

[1] *Department of Electrical and Mechanical Engineering, Graduate School of Engineering, Nagoya Institute of Technology, Gokiso, Showa, Nagoya 466-8555, Japan*

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ABSTRACT

Two different techniques, namely in-situ cycle annealing and post-growth patterning and annealing, were studied to reduce dislocation density in thick CdTe epilayers grown directly on (211) Si substrates using metal organic vapor phase epitaxy (MOVPE) for their applications in X-ray, gamma ray detector development. During in-situ annealing, it was observed that annealing initiated at a later stage of growth reduced the dislocation density more effectively than annealing initiated at the early growth stage. Nonetheless, in both cases, the dislocation density was reduced compared to the unannealed samples of similar thicknesses. On the other hand, the post-growth patterning of CdTe/Si into square islands, and subjecting these patterned samples to annealing was found to be more effective in reducing dislocations compared to the in-situ whole wafer annealing. However, subsequent growth of CdTe on the patterned and annealed samples to achieve thicker epilayers resulted rough surface, making them unsuitable for detector development.

1 Introduction

Epitaxially grown high-quality single crystal CdTe layers on large-area alternative substrates, such as Si, GaAs, offer potential for diverse applications. These extensive crystals can be used in the development of large-area infra-red (IR) focal-plane arrays for defense and space application, tandem solar cells for efficient energy conversion, and X-ray, gamma ray detectors for nuclear medical imaging, security, as well as in a range of scientific applications [1–5]. Particularly, heteroepitaxy of CdTe on Si not only yields large-area crystals but also enables the integration of IR and X-ray imaging detector arrays with Si-based readout electronics. Nevertheless, the valence mismatch, along with substantial differences in lattice constants and thermal expansion coefficients between CdTe and Si poses considerable challenges in this heteroepitaxial growth. This difficulty results in the formation of highly defective epilayers with a high density of dislocations. Various techniques, including multistep growth with in-situ thermal annealing [4–7], selective growth on patterned substrates [8, 9], thermal cycle annealing on planar or mesa-structured samples

Address correspondence to E-mail: niraula.madan@nitech.ac.jp

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[10–13], and the incorporation of strain superlattices, have been investigated to reduce the dislocation densities in mismatched heteroepitaxy [14, 15].

Recently, growth of CdTe on Si substrates by molecular beam epitaxy (MBE) or metalorganic vapor phase epitaxy (MOVPE), has resulted high-quality epilayers with dislocation densities in the low to mid-10^5 cm^{-2} range [5, 9, 10]. This is achieved by incorporation a thin ZnTe or Ge buffer layer before CdTe growth, followed by multiple cycles of thermal annealing. This approach is effective for IR detector technology, where CdTe layers serve solely as lattice-matched substrates for the subsequent growth of HgCdTe, and the device operates in the lateral direction. However, the addition of buffer layers creates a barrier for charge carriers in vertically operating devices, such as X-ray detectors or solar cells, where the photon-generated charge carriers traverse vertically across the heterointerface.

We investigated the direct growth of thick CdTe layers on (211) Si substrates without the use of buffer layers. To achieve thick epitaxial single crystal CdTe, we employed a specially designed Si substrates pretreatment technique, as detailed previously [16]. Subsequently, we utilized these layers to fabricate X-ray, gamma ray detectors in a p-CdTe/n-CdTe/n^+-Si heterojunction diode structure [16]. Nevertheless, the performance of the detector was constrained by crystal defects. Dislocations that extend into the p-n junction contribute to a significant device dark current, thereby substantially degrading device property [17]. Therefore, it is imperative to reduce these dislocations to enhance device property.

In our previous work, we explored post-growth thermal cycle annealing of CdTe/Si and observed enhanced crystallinity through X-ray rocking curve and photoluminescence measurements [18, 19]. While the annealing process effectively reduced dislocations in thin layers, its effect was less prominent in thick layers. Additionally, the improvements in the gamma detection properties of the detector were limited.

In this work, we explored two dislocation reduction approaches for thick CdTe epilayers. Firstly, we examined the impact of in-situ annealing during the growth process to identify the optimal initial CdTe layer thickness before the onset of annealing that produces high-quality thick layers. Secondly, we investigated post-growth pattering of islands on the CdTe/Si, followed by annealing and regrowth. The aim was to reduce dislocations on the islands by guiding them toward the edges, facilitating their escape and achieving high-quality selective growth of thick layers on the islands.

Here, we discuss the properties of CdTe crystals and suggest the most suitable technique for growing the thick CdTe layers needed in the development of X-ray, gamma ray detectors.

2 Experimental details

CdTe layers were grown on (211) Si substrates in a vertical-type MOVPE reactor with a rotating heater/susceptor. The growth was performed using dimethylcadmium (DMCd) and diethyltelluride (DETe) precursors, maintaining a DETe/DMCd flow rate ratio of 3. The details of the growth process have been reported elsewhere [15]. In summary, (211) n-type Si substrates underwent chemical cleaning and etching before being placed in a dedicated horizontal quartz-tube chamber, alongside with clean GaAs pieces. The substrates were heated above 800 °C in a hydrogen environment maintaining a temperature gradient between Si and GaAs. This resulted a clean passivated Si surface. Following the treatment, the Si substrates were promptly transferred to the MOVPE growth chamber for CdTe growth. This pretreatment step was essential for achieving epitaxial growth.

We investigated two techniques detailed below to reduce dislocation density in the epilayer. All epilayers in this study were characterized using double crystal X-ray rocking curve (DCRC), and 4.2 K photoluminescence (PL). Dislocation density was estimated by subjecting the samples to dislocation decorative etching using Everson solution [20], and counting the triangular pits formed on the surface using an optical microscope.

2.1 Study of in-situ annealing

The samples were prepared as follows: Initially, a thin CdTe nucleation layer was grown at 350 °C for 10 min. Subsequently, the substrate temperature was raised to 450 °Cand CdTe layers of various thicknesses (buffer layers) were grown by varying the growth time from 30 to 60 min. In-situ annealing was applied to investigate the impact of annealing on the initial buffer layer thickness. The annealing temperature was varied from 500 to 600 °C, number of cycles one or two, and duration per cycle was kept fixed at 5 min. DETe precursor was introduced into the growth chamber

during annealing to maintain a Te-environment. Then final CdTe growth occurred at 450 °C to make overall CdTe thickness of approximately 12 μm, as in Fig. 1a. A limited number of samples with similar thicknesses were also grown without subjecting the in-situ annealing. Finally, all CdTe/Si samples were cut into several 6 mm × 6 mm pieces for various characterizations.

2.2 Study of post-growth pattering, annealing and regrowth

In this study, initial thin CdTe epilayers of varying thicknesses (0.4 ~ 5 μm) were grown on Si substrates, followed by patterning using photolithography to form islands measuring 60 × 60 μm^2, with a 20 μm gap between the islands. Subsequently, ex-situ thermal annealing was applied at 500 °C for 5 min, in a flowing hydrogen environment. This annealing condition was optimized in a separate study [19]. Following annealing, the samples were re-introduced into the MOVPE growth chamber and the final CdTe growth was carried out at temperatures varying from 350 to 500 °C. The schematic representation of sample structure is presented in Fig. 1b.

3 Results and discussion

3.1 In-situ annealing: effect of buffer layer thickness

All CdTe epilayers grown on the (211) Si substrates exhibited a single crystalline structure with growth orientation parallel to the substrate. The XRD pattern revealed only CdTe (422) peak, indicating the absence of twinned regions in the grown crystal. Figure 2 shows DCRC FWHM values from the CdTe (422) peaks as a function of buffer layer thickness (growth time). Following the buffer layer growth, the samples were subjected to in-situ annealing at 550 °C, in a Te-environment for 1 or 2 cycles, with a fixed annealing duration of 5 min per cycle. Subsequently, the final layer growth occurred at 450 °C. For comparison, the XRD DCRC value of a sample without in-situ annealing is also presented in the figure. The results reveal an improvement in the DCRC values after annealing, where better outcomes observed when annealing commenced at the later stage of buffer layer growth. However, samples, apart from the 30 min buffer layer growth, exhibit poor crystallinity during 2-cycle annealing. This could be attributed to surface roughening caused by CdTe etching due to the elevated sample temperature. It is probable that the actual surface temperature exceeds the set value with an increase in the number of annealing cycles.

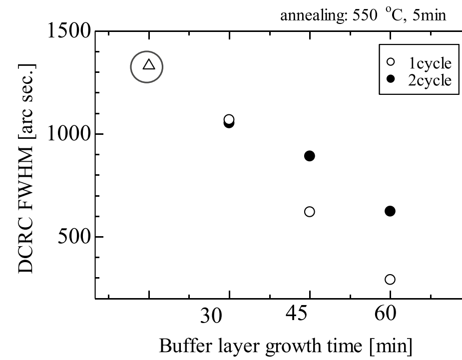

Fig. 2 DCRC FWHM values of the CdTe layer as a function of the buffer layer thickness at which annealing was initiated. The triangular point enclosed within a circle corresponds to the unannealed value

We further examined the effect on annealing temperature using a fixed buffer layer thickness. Figure 3 shows DCRC FWHM values of the samples as a function of annealing temperature, with the buffer layers grown for 60 min before initiating the annealing. The

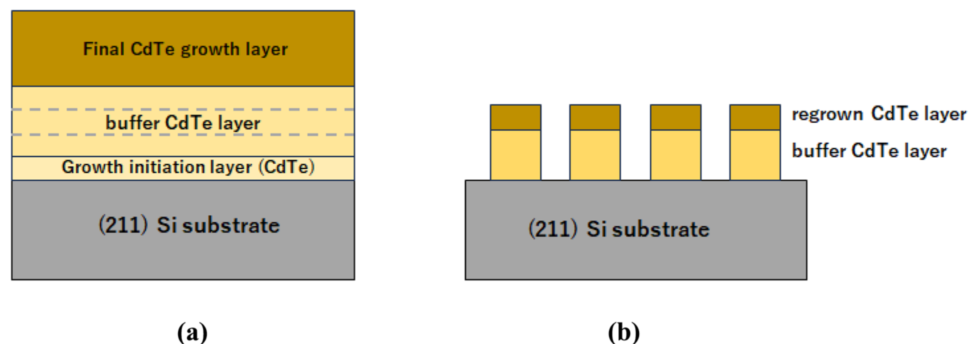

Fig. 1 Schematic diagrams of the sample structure studied: **a** in-situ annealing during growth **b** post-growth patterning, annealing and regrowth

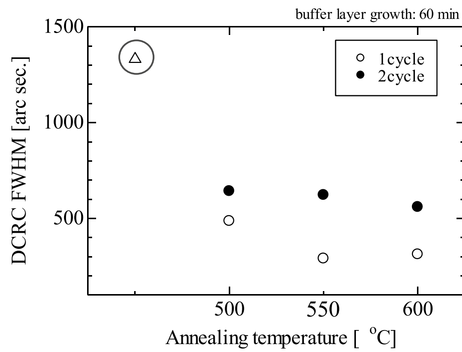

Fig. 3 DCRC FWHM values of the CdTe layer as a function of annealing temperatures. The annealing commenced after growing the buffer layer for 60 min. The triangular point enclosed within a circle represents the unannealed value

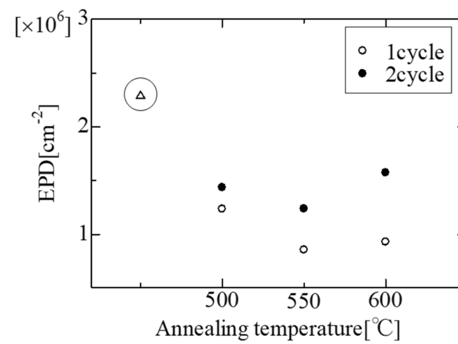

Fig. 5 EPD values of CdTe samples as a function of annealing temperature and annealing cycles. The triangular point enclosed within a circle corresponds to the EPD of the unannealed sample

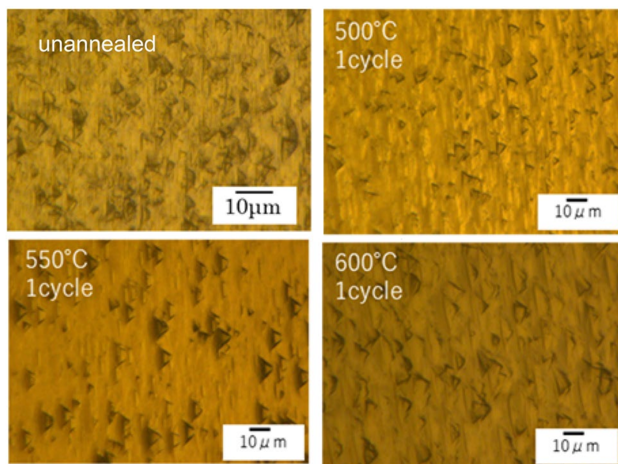

Fig. 4 Optical images of sample surfaces after undergoing an Eversion dislocation-revealing etch: **a** as-grown sample, **b**–**d** samples subjected to single-cycle annealing at different temperatures after growing the buffer layer for 60 min

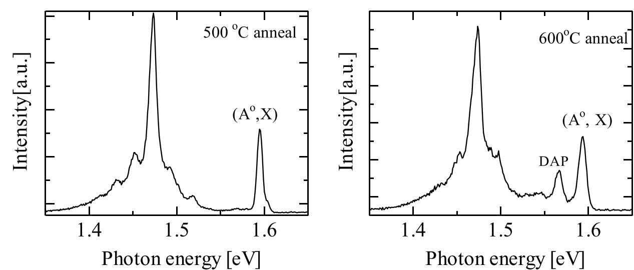

Fig. 6 4.2 K photoluminescence spectra of 500 and 600 °C, single-cycle in-situ annealed samples

annealing cycle was set either 1 or 2, and the duration per cycle was fixed at 5 min. The results suggest that a single-cycle annealing at 550 °C is optimal for enhancing crystallinity.

Figure 4 presents the surface morphology of Everson etched samples prepared through single-cycle, in-situ annealing at different temperatures. The surface morphology of a sample prepared without in-situ annealing is also included for comparison. Triangular pits corresponding to the CdTe (211)B face are clearly visible in the images. Based on this observation, we counted the pits on the surface and plotted them as a function of annealing temperature, as shown in Fig. 5. A notable reduction in the etch pit density (EPD) values was observed in the annealed samples compared to the unannealed one. The lowest EPD value, 9.5×10^5 cm^{-2}, was achieved in the sample annealed at 550 °C. This indicates that thermal annealing effectively facilitated the motion of threading dislocations, activating their interactions in a way that resulted in the coalescence or annihilation of adjacent dislocations. As a result, their surface density decreased, as confirmed by lower etch pit counts. Similar reductions in threading dislocation density have been reported in various studies after thermal cycle annealing [5, 10, 21]. On the other hand, increasing the annealing cycle to two resulted in a higher pit density compared to the single-cycle anneal. This increase could be attributed to the elevated surface roughness, as discussed above. Nonetheless, the pit densities of the 2-cycle annealed samples remained lower than those of the unannealed samples.

The crystal properties were further examined by low-temperature (4.2 K) PL measurement, using a 488 nm semiconductor laser as the excitation source. Figure 6 shows the PL spectra of samples annealed at 500 and 600 °C. The (A°,X) peak at 1.593 eV becomes

sharper in the 500 °C annealed sample, indicating improved crystallinity. In contrast, an additional broad peak appears at 1.565 eV in the 600 °C annealed sample, likely attributed to donor-acceptor pair (DAP) transition involving a cadmium vacancy- related acceptor center [22]. This may be due to cadmium leaving the sample surface due to increased surface temperature.

3.2 Post-growth patterning, annealing and regrowth

CdTe thin buffer layers of various thicknesses were grown on (211) Si substrates at temperatures ranging from 350 to 400 °C. Growth times were varied from 10 to 60 min at each temperature to achieve CdTe epilayers of various thicknesses. Subsequently, squared islands were patterned on these CdTe/Si buffer layers using photolithography. Thee patterned samples were subjected to ex-situ annealing at 500 °C for 5 min, followed by the regrowth of subsequent CdTe layers at temperatures from 325 to 500 °C. The objective was to reduce the dislocation density on the islands and achieve high-quality selective growth of thick layers. Figure 7a presents a representative patterned sample used in this study, where the growth was performed at 400 °C, 10 min, resulting in an approximate CdTe buffer layer thickness of 2 µm. XRD measurement performed (not presented here) before pattering showed that the epilayers were (211) oriented, parallel to the Si substrate. Shown in Fig. 7b is the morphology of the sample after a 500 °C, 5 min anneal, followed by CdTe regrowth at 400 °C. The result reveals that CdTe growth occurred not only on the islands but also between them, resulting in a rough and uneven sample surface. Samples with varying buffer layer thicknesses (ranging from 0.4 to 5 µm), subjected to

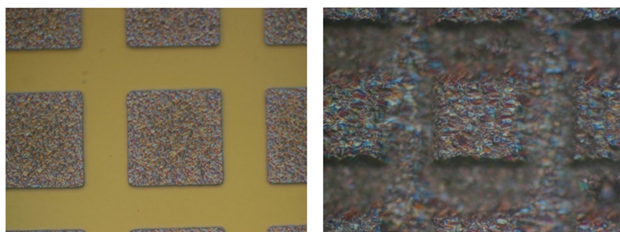

Fig. 7 Optical image of a post-growth patterned sample (left) and after regrowth (right). The sample on the left is approximately 2 µm thick, whereas it measures 10 µm after regrowth (right). The yellow portion in the left figure represents bare Si

annealing and regrowth at various growth temperatures also exhibited similar results. It was observed that the surface roughness increased with the buffer layer thickness. This suggests that the investigated growth temperatures and the buffer layer thickness (islands' height) are excessive, necessitating further optimization of growth conditions to achieve selective epitaxy exclusively on the CdTe islands.

Separate study was performed to assess the impact of island patterning and annealing on dislocation reduction. The dislocation density of the patterned and annealed samples was examined using defect-decorating etch. The results indicated that etch pit density on the islands was nearly an order of magnitude lower than on the unpatterned flat area of the wafer. This suggests that patterning and annealing facilitate dislocation interactions, leading to their annihilation or coalescence onto a single dislocation. Additionally, it aids in gliding dislocations towards the sidewalls of the islands in patterned samples, facilitating their escape and, consequently, reducing their densities at the island surface. The detailed results are reported elsewhere [19].

4 Conclusion

We investigated dislocation density reduction techniques for MOVPE-grown thick CdTe layers grown directly on (211) Si substrates, using in-situ cycle annealing during growth and post-growth patterning, annealing, followed by regrowth.

In-situ single-cycle annealing applied during the later stage of growth resulted in improved crystallinity compared to annealing at the early growth stage. The lowest etch pit density (EPD) value, 9.5×10^5 cm^{-2}, was achieved for a 12 µm thick sample annealed with a single cycle at 550 °C for 5 min, with the annealing initiated after growing the CdTe buffer layer for 60 min.

Post-growth pattering and ex-situ annealing in a hydrogen environment was found to be effective in dislocation reduction, where nearly an order of magnitude reduction in EPD was achieved compared to unpatterned samples of similar thicknesses. However, selective growth on these patterned and annealed samples to achieve higher thicknesses resulted in a very rough surface, rendering it unsuitable for detector applications. At current stage, the in-situ annealing technique appears to be the preferable choice for detector development.

Author contributions

All authors contributed to this work.

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Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Declarations

Conflict of interest The authors have no conflicts to disclose.

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