



Understanding the coexistence of two bipolar resistive switching modes with opposite polarity in Cu_xO ($1 \leq x \leq 2$)-based two-terminal devices

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ABSTRACT

In this work, we have fabricated and tested the resistive switching behavior of non-volatile nature in a number of devices with mainly two architectures: (1) W tip/ Cu_xO /Pt/Ti/ SiO_2 /Si and (2) Cu contact pad/ Cu_xO /Pt/Ti/ SiO_2 /Si. The device type (1) showed coexistence of two bipolar resistive switching modes, commonly known as eight-wise (8w) and counter-eight-wise (c8w), in their current–voltage (I - V) characteristics. We report considerably high ON/OFF ratio of 10^5 and stable retention time 15×10^3 s. The formation and annihilation of metallic Cu nanofilaments were argued as the plausible reason behind the observed resistive switching events. The onset of quantized conductance steps in the typical conductance plots (in units of quanta of conductance $2e^2/h$, where e and h are electronic charge and Planck's constant, respectively) – a phenomenon usually observed in narrow conductive channel – was exploited to provide an “indirect” proof for formation of metallic Cu-based filaments or channels during switching. On the contrary, in device type (2), we observed only “regular” bipolar switching. The operating voltage was less than 1 V in both the devices – suggesting its potential low-power applications. We assessed the underlying conduction mechanism in depth and also theoretically estimated the lateral size of the tiny conductive nanofilaments formed during the switching events. Copper being a cost-effective and widely available substance, our results indicate that Cu_xO -based cells can be a feasible and useful route for non-volatile resistive memories.

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1 Introduction

In order to effectively store and process data, development of different types of non-volatile memories (NVMs) with novel material and architecture is paramount. Significant progress, both in theory [1] as well as in experiments [2], has been made in recent years to realize this objective. The quest for realizing the fundamental limit in complementary metal–oxide–semiconductor (CMOS)-based electronics has pushed physicists and engineers to certain obvious limitations [3] such as further miniaturization (difficulty in achieving length scales sub 20 nm), high operating voltage (~ 12 V), low endurance ($< 10^6$), and low programming speed (μ s to write and ms to erase), among others. The reportedly increasing interest for realizing next generation NVMs is perceived to have overcome some of those bottlenecks [4, 5]. There is an urgent need for an appropriate, non-charge-based memory technology to find a suitable alternative in order to go beyond von Neumann computing. Ferroelectric random-access memory (FeRAM) [6], phase-change random-access memory (PCRAM) [7], and resistive random-access memory (RRAM) [8, 9] are the prominent emerging NVM technologies. Among them, RRAM is considered to be very useful due to its remarkable features such as excellent scalability, low operational voltage (< 3 V), high endurance, simple structure, ease of fabrication, and process compatibility with existing CMOS [10–14]. RRAM works based on the principle of resistive switching (RS) wherein the resistance of the device can be toggled between different and distinct states. Unlike conventional MOS transistors, RRAM is a two-terminal device. A thin layer of oxide (typically a few tens of nm thick) material is sandwiched between two metal contacts. Furthermore, RRAM devices can modulate and retain their internal state variable(s) whenever needed [15–17]. Ability to form 3D stacking has made RRAMs an effective tool for extremely high-density data storage applications [18]. RS-based memory cell has been reported for a variety of materials, such as transitional metal oxides (e.g., HfO_2 [19], TiO_2 [20], WO_x [21], NiO [22], Ta_2O_5 [23]), graphene oxide [24], organic compounds [25], inorganic perovskites [26], organic–inorganic hybrid polymer [27], metal sulfide [28], Mott insulators [29], ferroelectrics [30], layered materials such as hexagonal boron nitride [31] and transition metal dichalcogenides [32], and other chalcogenide materials [33].

Some not-so-conventional materials such as protein [34], glucose [35], polyoxometalates [2], and egg albumen [36] also showed stable and non-volatile RS phenomena. Typically, one can observe two states in RRAMs – a high resistance state (HRS) and a low resistance state (LRS). They can be assigned to binary “0” and “1” levels, respectively. Switching from HRS \rightarrow LRS is known as SET process and that from LRS \rightarrow HRS is called RESET process. Situations wherein SET and RESET happen in the same polarity of bias voltage are called “unipolar” RS [37]. If SET and RESET happen in opposite bias polarity, the switching is named “bipolar” RS [38]. In general, the switching mechanism in RRAM is explained in terms of formation and rupture of narrow conductive filaments (CFs) or paths inside the dielectric oxide matrix kept between two electrical contacts. There are, in general, two prominent divisions for RRAM cells: valence change memory (VCM) and electrochemical metallization (ECM) memory. The widely accepted mechanism under which the VCM works is the electric field-induced movement of oxygen ions in the nanoscale and the follow-up redox process in the sublattice. Here, under external electric stimuli, oxygen ions get removed from the oxide matrix resulting in oxygen vacancy (OV) formation. Oxygen vacancies carry positive charge relative to the lattice, and they trap electrons under the applied voltage. These vacancies align on application of the field, thereby forming the CFs to switch the device from HRS to LRS. This is SET process. During RESET process, oxygen ions recombine with vacancies causing rupture of CFs which bring the device back to HRS. On the other hand, in case of ECM cells, the formation and rupture of CFs happen due to the electrochemical redox reaction that occurs at the electrodes. When a positive voltage is applied to the active electrode (anode), it undergoes oxidation to form metal ions. Under the applied electric field, these metal ions migrate towards the inert electrode (cathode) through the insulating matrix. After getting reduced at this electrode (cathode), these metal ions accumulate there as neutral metal atoms which eventually result in the gradual formation of tiny CFs. This will drive the device to LRS, which corresponds to the onset of the SET process. When the polarity is reversed (negative voltage applied to the active electrode), the as-deposited metal atoms at cathode undergo oxidation to form metal ions causing rupture of the CFs. This will RESET the device back to HRS [2, 14, 39].

In this work, we investigated the RS phenomena in RRAM cells fabricated using thin films of variants of oxide of copper (Cu_xO with $1 \leq x \leq 2$). We fabricated two types of devices with architectures: (i) W tip/ $\text{Cu}_x\text{O}/\text{Pt}/\text{Ti}/\text{SiO}_2/\text{Si}$ and (ii) sputter-deposited Cu contact pad/ $\text{Cu}_x\text{O}/\text{Pt}/\text{Ti}/\text{SiO}_2/\text{Si}$. Hereafter, we will use acronyms W tip- Cu_xO for device type (i) and Cu- Cu_xO for device type (ii). Apart from being an abundantly available metal, Cu is nontoxic and relatively inexpensive, and most importantly it offers a high degree of compatibility with the modern semiconductor process industry [40]. Resistive memories based on Cu_xO can offer a promising alternative owing to its cost effectiveness and facile fabrication. They also exhibit remarkably high ON/OFF ratio, stable and repetitive switching, long endurance, and retention metrics, and more importantly the capability to accommodate a variety of top and bottom metal contacts [41–46]. Unlike many conventional binary oxides, one can exploit variety of deposition techniques such as thermal oxidation [40], sputtering [41, 45], solution processing [44], atomic layer deposition [42], and pulse laser deposition [45] for obtaining smoother and sub-100 nm thickness Cu_xO thin films. In general, one can find two stable oxide phases of Cu – cupric oxide (CuO) and cuprous oxide (Cu_2O) – both being p-type semiconductor having band gap (E_g) of 1.7–2.2 eV [44]. Therefore, the current–voltage characteristics in Cu_xO -based devices are governed by the injection and transport of hole carriers. In general, both phases of Cu_xO are found while depositing its thin film. These above cited properties can be used to tailor the band gap and carrier mobility of Cu_xO film, using which one can control its resistive switching behavior. Additionally, by adjusting oxygen partial pressure of the CuO and Cu_2O , the switching parameters can be effectively engineered. For W tip- Cu_xO cells, we observed two distinct bipolar resistive switching (BRS) modes that appeared in *opposite bias polarities*. Similar switching behavior was also observed in a number of cells made from variety of oxides in the past [47–50]. In such situations, one can switch the device in both polarities in such a way that the same device can SET in positive voltage and RESET in negative voltage, and then SET in negative voltage and RESET in positive voltage. Strikingly, for Cu- Cu_xO devices, only *regular* BRS was observed, wherein SET happened only on positive polarity and RESET only on negative polarity of bias voltage. Details of both these

types of switching events have been elucidated in the subsequent sections.

2 Experiments

The two different types of Cu_xO -based RRAM devices, as mentioned above, were fabricated using DC magnetron reactive sputtering technique. In the first set of devices, the functional oxide layer of Cu was sputtered on Pt-coated SiO_2/Si substrate wafer in the presence of regulated oxygen pressure. Tungsten metal (W) probe tips of 25 μm diameter were used as the top electrode (TE). Platinum (Pt) acted as the bottom electrode (BE). Titanium (Ti) layer was used for good adhesion between the top Pt layer and the bottom SiO_2/Si wafer substrate. The argon and oxygen flow rates inside the sputter chamber during oxide layer deposition were kept around 15 sccm and 10 sccm, respectively, which resulted in a chamber pressure of 4×10^{-2} mbar during deposition. The substrate temperature during sputter deposition was maintained at 200 °C. The schematic of the W tip/ $\text{Cu}_x\text{O}/\text{Pt}/\text{Ti}/\text{SiO}_2/\text{Si}$ device is shown in Fig. 1(a) and its optical image in Fig. 1(b). Second, we fabricated another set of devices with pure copper (Cu) metal as TE deposited on the same $\text{Cu}_x\text{O}/\text{Pt}/\text{Ti}/\text{SiO}_2/\text{Si}$ heterostructure using the DC magnetron sputtering with shadow masks having patterned holes of 300 μm diameter, as shown in Fig. 1(c) and 1(d). We performed charge-based current–voltage (I – V) measurements on these memory cells using Keithley 2614B dual-channel source/measure unit (SMU) in fully open-air conduction. The investigation on surface morphology, atomic composition, and oxidation states of the sputter-deposited Cu_xO film was carried out using field-emission scanning electron microscopy (FESEM Gemini Ultra 55) and X-ray photoelectron spectroscopy (XPS Axis Ultra), respectively.

3 Results and discussion

3.1 Structural characterization

Figure 2(a) shows a cross-sectional scanning electron micrograph of the Cu_xO thin film deposited on Pt-coated Si wafer. The thickness of the Cu_xO film was estimated to be around 75 nm. The XPS data, as shown in Fig. 2(b), demonstrate binding energy

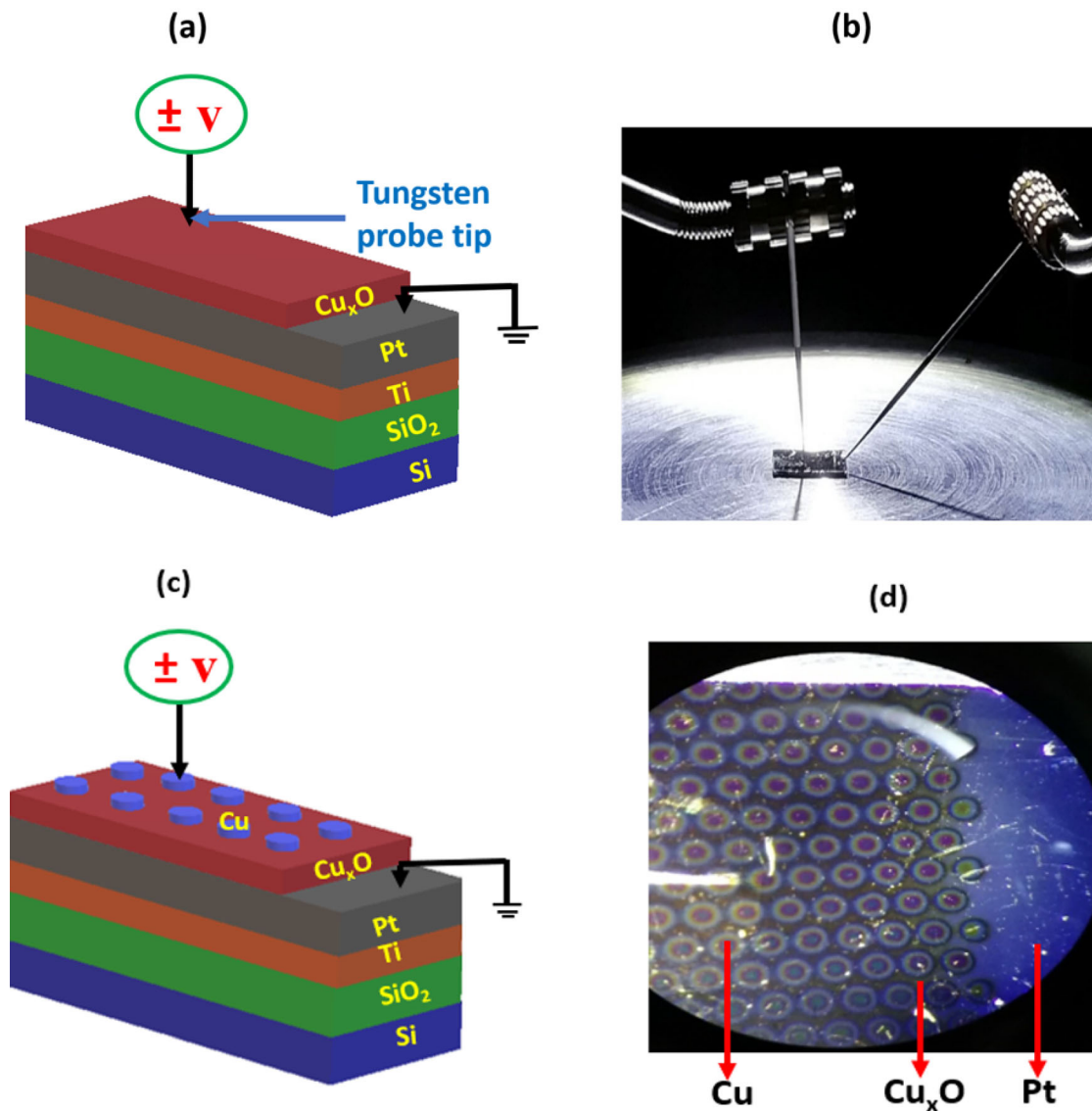


Fig. 1 **a** Schematic representation of the biased W tip/Cu_xO device with Pt as BE and tungsten probe tip (of 25 μm dia) as TE (M–I–M configuration), **b** Optical image of probed W tip–Cu_xO device used for electrical characterization. **c** Schematic diagram of

the biased Cu–Cu_xO device, **d** Optical image of Cu–Cu_xO devices wherein Cu metal pads were deposited on Cu_xO/Pt/Ti/SiO₂/Si by DC magnetron sputtering using shadow mask technique. These Cu metal pads act as TE and Pt as BE

peaks of Cu 2p_{3/2} and Cu 2p_{1/2} – an indicative of the presence of Cu₂O and CuO phases, respectively [51]. R. Ebrahim et al. [41] found one more peak for metallic Cu phase in addition to these two oxide phases. However, in our device, we did not observe the presence of metallic phase of Cu, and therefore, the initial LRS could not be found in our charge transport data. The Cu 2p_{3/2} peaks centered at binding energy values of 932.3, 933.9, 941.1, and 944 eV indicate the presence of Cu₂O phase and the single peak at 933.9 eV showed the presence of CuO phase in the oxide matrix [51–53]. The peaks at 941.1

and 944 eV are the satellite peaks. The onset of CuO phase in the Cu_xO thin film gradually shifts the position of Cu 2p_{3/2} peak towards higher binding energy values (932.3 to 933.9 eV). Additionally, the Cu 2p_{1/2} peaks at 952.1, 953.8, and 962.2 eV indicate the presence of CuO phase. The two Cu2p_{3/2} peaks centered at 932.3 and 933.9 eV represent the Cu¹⁺ and Cu²⁺ phases, respectively. The area under the peak centered at 932.3 eV is larger than that at 933.9 eV. This difference in area implies that the Cu₂O (Cu¹⁺) phase is more predominant over CuO (Cu²⁺) phase [51–53].

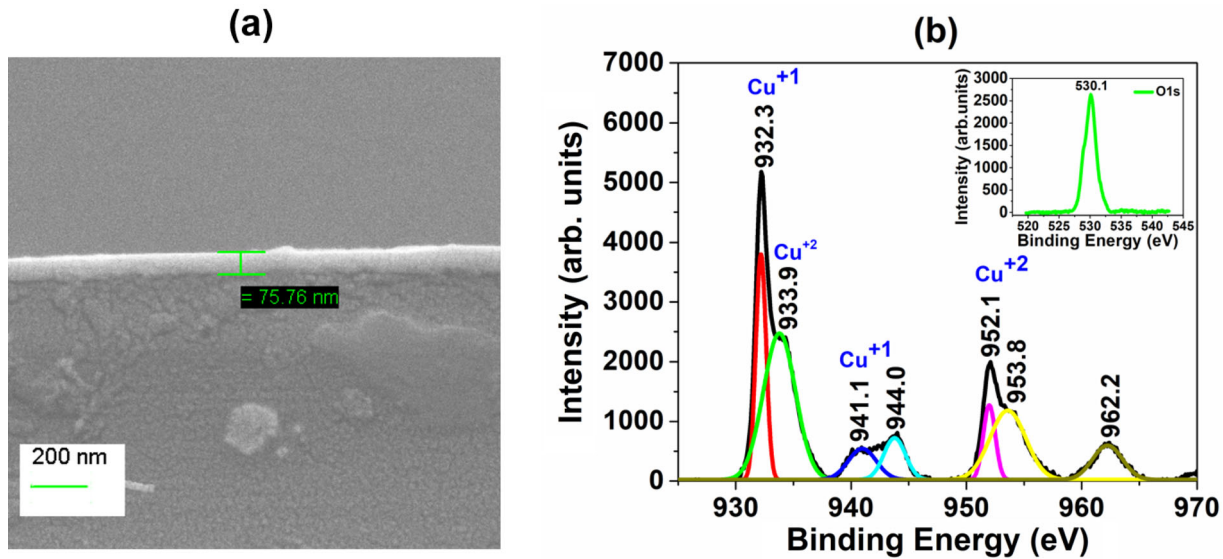


Fig. 2 **a** Cross-sectional SEM image of Cu_xO thin film grown on Pt-coated Si substrate using DC magnetron reactive sputtering at 200 °C. Thickness of the film is ~ 75 nm. **b** XPS spectra of the

sputtered Cu_xO thin film showing the Cu^{+1} and the Cu^{+1} peaks. Inset image depicts O1s peak showing the presence of oxide phases

3.2 Electrical transport measurement

The I - V characteristics of the W tip- Cu_xO device were studied by sweeping the device through DC bias voltage applied between the top (W tip) and the bottom (Pt) electrodes. We observed very robust, repetitive, and uniform switching between two distinct resistance (or current) levels in this metal-insulator-metal (M-I-M) configuration, as shown in Fig. 3. All measurements were performed at room temperature and at ambient condition. During measurements, a compliance current (I_c) of 500 μA was prefixed in order to protect the device from permanent dielectric breakdown. The device remained in a high insulating state with an initial resistance of 66.5 M Ω . An electroforming process was required to create defects in the oxide and push the device into the switching regime. This could SET the device to the switching mode from HRS to LRS, as can be seen in Fig. 3 (a).

On sweeping the W tip- Cu_xO memory cell, using DC bias from 0 to 5 V, we observed an abrupt change in current (transition from HRS to LRS) at a bias of 3.34 V, while keeping with $I_c = 500 \mu\text{A}$. This drives the cell into the *electroforming* process which happens across the bulk of the oxide matrix. Post this forming process, a negative voltage sweep of 0 V to -2 V (with a compliance current of 10 mA) was sourced to the device, which RESET (transition from LRS to HRS)

the device at voltage—0.75 V to a new HRS lesser than the resistance found before forming process. The device could now be cycled repeatedly between the HRS and the LRS. For all our W tip- Cu_xO memory cells, SET process occurred at positive polarity of bias voltage and RESET process at negative polarity (applied at the TE). This indicates the onset of *regular* BRS behavior. The semi-logarithmic I - V graph of BRS characteristics observed in W tip- Cu_xO devices is shown in Fig. 3 (b).

Once this RESET was attained, we gradually increased the positive bias at the top W tip (from 0 to 1 V, $I_c = 500 \mu\text{A}$) again, as shown in Fig. 3 (b). We observed that the current was initially very low ($\sim 10^{-9}$ A), indicating the HRS of the device. However, it started increasing with increase in voltage which is shown by arrow-1, and at some threshold value of the bias, the current shot up abruptly, driving the cell into the SET process, as indicated by arrow-2, in Fig. 3 (b). Owing to the prefixed compliance current, even with further increase in bias voltage, the current remained constant thereon, as marked by arrow-3. Then the current decreased with decrease in voltage by maintaining the already obtained LRS (arrow-4). When the bias voltage polarity at TE was reversed, the device maintained its LRS (arrow-5) till the threshold voltage at which the device switched back from LRS to HRS (which we can call RESET process), as indicated by arrow-6.

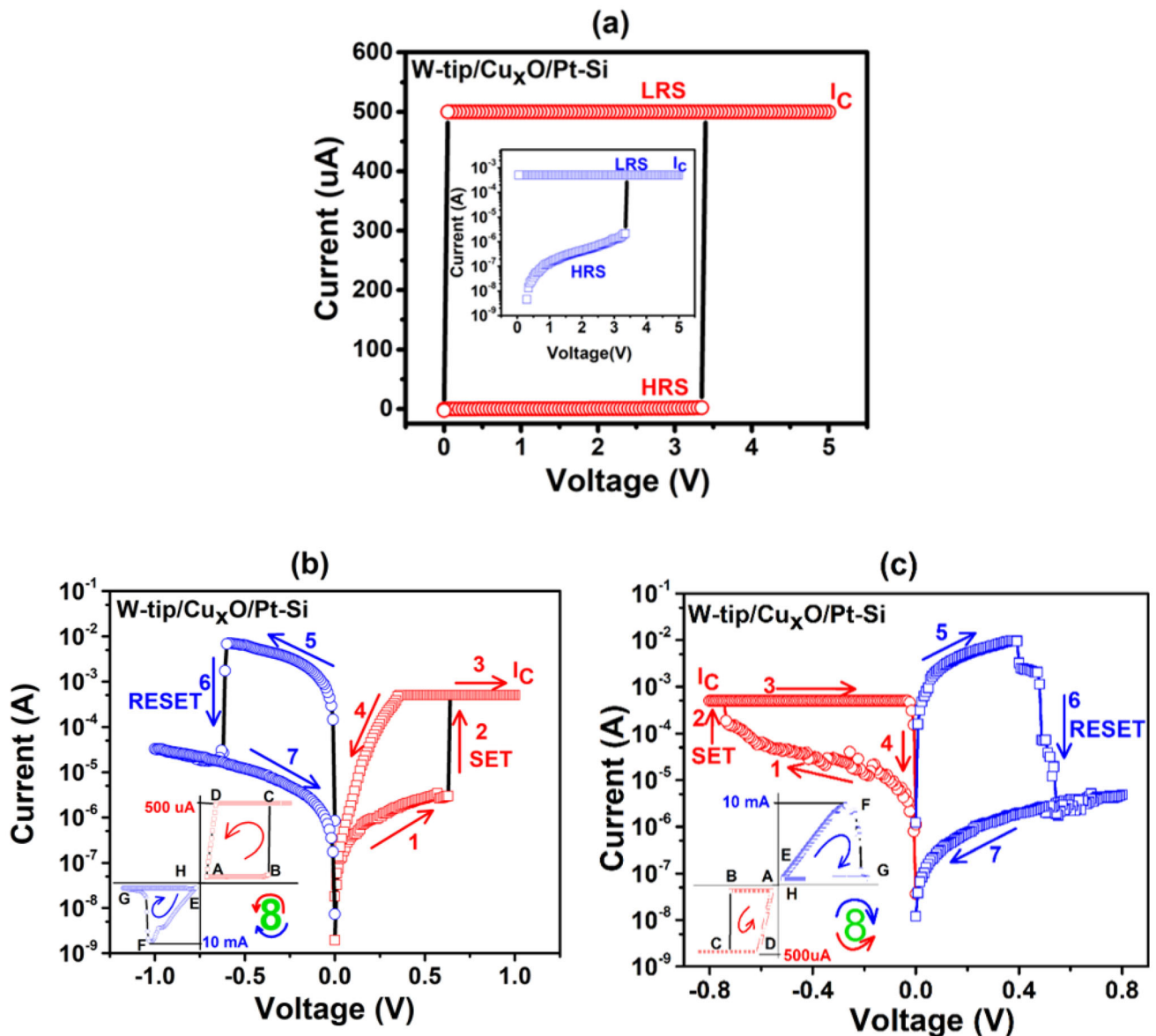


Fig. 3 Results obtained from electrical characterization of W tip-Cu_xO devices. **a** Electroforming process with a compliance current of 500 μ A. Inset image shows corresponding semi-logarithmic plot **b** I - V plot (semi-logarithmic) of 8w BRS. The numbers 1 to 7 with the arrows represent one switching cycle with SET process under positive bias voltage and RESET process under negative bias voltage applied at the top W electrode. Inset image shows the corresponding normal I - V plot with SET and RESET in the upper (ABCD, in red) and lower (EFGH, in blue) halves, respectively,

When the voltage decreased to zero the current also decreased by maintaining the cell in the same HRS, as can be seen with arrow-7. This one SET process and one RESET process constitute a full RS cycle for the RRAM device. It is noteworthy that apart from this regular BRS events, we also observed another

which resemble the drawing direction of handwritten ‘8’. **c** I - V plot (semi-logarithmic) of c8w BRS. The numbers 1 to 7 with the arrows represent one switching cycle with SET process under negative bias and RESET process under positive bias voltage applied at the top W electrode. Inset image shows the corresponding normal I - V plot with SET and RESET in the lower (ABCD, in red) and upper (EFGH, in blue) halves, respectively, which resemble the opposite drawing direction of handwritten ‘8’

peculiar switching behavior which we, hereafter, call *reversed* BRS – implying that we could observe an opposite hysteresis loop with SET process at negative bias polarity and RESET process at positive polarity (at TE). So, the device showed two distinct BRS modes in both positive and negative bias polarities.

This switching pattern is similar to the ones reported in Ref. [47–50]. Interestingly, Y. Sharma et al. reported a number of switching modes with both unipolar and bipolar nature in amorphous LaHoO_3 -based memory cells [54]. Contrary to that, we observed only two distinct BRS modes that appeared in opposite polarity. The appearance of two BRS modes in both polarities and the absence of unipolar switching in our $\text{W tip-Cu}_x\text{O}$ cells can, therefore, be termed as “two coexisting BRS modes” [48].

In order to examine the above-mentioned RS behavior, a negative voltage sweep was sourced into the device. We observed a change in resistance from HRS to LRS (SET) at a bias of -0.57 V. A positive voltage sweep could RESET the device at bias of 0.65 V. This reversed BRS behavior is shown in Fig. 3 (c). The compliance current was kept the same ($I_c = 500 \mu\text{A}$) in both the regular and reversed BRS. The switching process in both regular and reversed polarities happened in a range of ± 0.3 V to ± 0.6 V which confirms the coexistence of two BRS modes in opposite polarities. The RESET process was initiated by relatively a high current of 10 mA in both regular and reversed BRS. These switching modes are commonly called eight-wise (8w) and counter-eight-wise (c8w) BRS, respectively [47–50, 55]. The I - V plot of regular BRS (SET under positive bias and RESET under negative bias applied at TE) resembles the drawing direction of handwritten “8,” as shown in the inset image of Fig. 3 (b) with SET and RESET processes in upper (ABCD, in red) and lower (EFGH, in blue) halves, respectively. This is called 8w BRS. Similarly, the I - V plot of reversed BRS (SET under negative bias and RESET under positive bias applied at TE) shows the opposite drawing direction of handwritten “8,” as shown in the inset image of Fig. 3 (c) with SET and RESET processes in lower (ABCD, in red) and upper (EFGH, in blue) halves, respectively. This switching scenario is known as c8w BRS. In a nutshell, controlled application of voltage at TE and appropriate compliance current resulted in two kinds of BRS events in $\text{W tip-Cu}_x\text{O}$ devices. The I - V plots for 8w and c8w BRS are shown in Fig. 3 (b) and 3 (c), respectively, wherein numbers “1” to “7” represent one full switching cycle. Inset shows the corresponding normal I - V plots. In both cases, once the switching happened the device maintained its states even after the removal of bias – implying non-volatility of the memory cells. In this way, we could switch the device for a large number of cycles, and it

showed repetitive and reliable RS behavior. Figure 4(a) depicts the first 110 switching cycles. We performed these charge transport measurements on nearly ten $\text{W tip-Cu}_x\text{O}$ memory cells fabricated at different slots and observed similar switching behavior in all. We found that the switching voltage varied only in the small range of 0.33 V– 0.58 V in almost all cells, as can be seen in Fig. 4(a). Obtaining such different switching windows is beneficial for them to be useful for practical device applications [2]. In regular BRS, we could observe the resistance change from 10.8 M Ω to 179Ω , which yields ON/OFF ratio $\sim 10^5$. This is several order magnitude higher than the value reported by R. Ebrahim et al. [41]. Figure 4(b) shows the distribution of resistances at HRS and LRS for first 110 cycles. Inset figure shows the variation in resistance at LRS (in a zoomed-in scale).

Retention characteristics were studied by setting the device to LRS and applying a read voltage of 100 mV to keep the cell at that resistance state (binary ON) for 15×10^3 s, followed by resetting the device to HRS and observed the resistance state (binary OFF) for same duration and with the same read voltage. The device was found to retain its two distinct resistance states for 15×10^3 s without undergoing any noticeable change/drop in current. This is an indication that the Cu_xO -based cells can be explored for fabricating non-volatile memory for long-term data storage application. The retention characteristics of the device is shown in Fig. 5 (a).

With a view to analyzing the exact charge transport mechanism underlying our observed RS, we redrew I - V characteristics in Log–Log scale. As can be seen in the linear fit of the logarithmic I - V plot (shown in Fig. 5 (b)), initially the current directly follows the voltage applied at the TE (Ohmic transport as given by $J \propto V$). Contrary to the linear behavior of current density in the low-bias regime (< 0.152 V), we observed a sharp increase in current as we ramped up bias voltage further (> 0.152 V); the current follows $J \propto V^2$ law [2]. The slope of the Log I -Log V plot changes from 1 to 2 as the bias increases from very low to high values. This transport model carries a reminder of the space-charge-limited current (SCLC) mechanism. In the regime of sufficiently low applied bias voltage (at the top W electrode tip), the number of thermally generated free charge carriers is abundantly higher in the oxide matrix than the injected

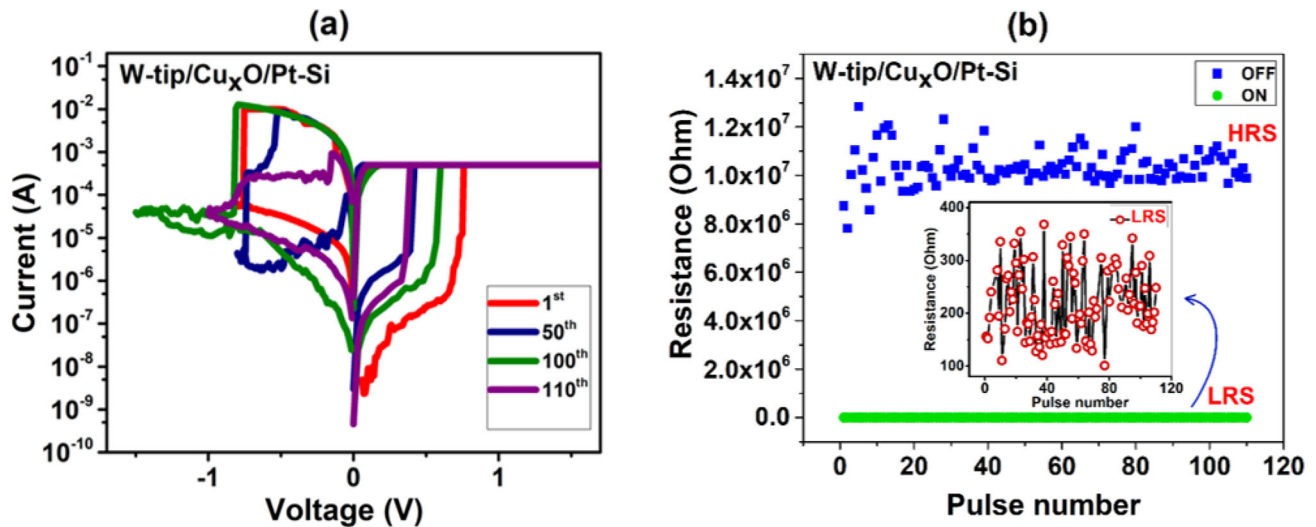


Fig. 4 **a** I - V curves showing repetitive sweeping cycles of bipolar nature in W tip- Cu_xO devices for first 110 cycles. **b** Distribution of resistances at HRS and LRS for 110 cycles. Inset figure shows the variation in resistance at LRS

carriers from the electrode. Here, the current directly depends on the applied bias and the conductivity of the bulk oxide film follows straight Ohm's law, and the slope of $\text{Log } I$ - $\text{Log } V$ plot is 1. Beyond a threshold voltage, thermally generated carriers were dominated by the injected excess carriers, resulting in a conduction process controlled mainly by shallow traps, as given in the equation as follows [40, 56]:

$$J = \frac{9\varepsilon_r\varepsilon_0\mu V^2}{8L^3} \left(\frac{N_c}{N_t} \right)^{\frac{E}{kT}}, \quad (1)$$

where ε_r is the static dielectric constant of the oxide material, ε_0 is the permittivity of free space, μ is the hole carrier mobility, V is the applied bias voltage, L is the film thickness, N_c is the effective density of states in the valence band, N_t is the number of shallow traps, E is the effective trapping potential, and T is the working temperature. Further increase in current indicates the existence of deep traps which were distributed around trap-level energies. The increase in the applied bias leads to the formation of a space-charge region by occupying the existing trap centers by the injected carriers. The conduction process then changes from trap-assisted to trap-filled event. With the further increase of voltage, the transport becomes completely trap free [56] and subsequently the slope of the $\text{Log } I$ - $\text{Log } V$ plot reaches the value 2.

Many research reports – some directly and some indirectly – suggest the filament theory as the

possible mechanism that drives the RRAM between two distinct electrical resistance states. The most prominent “direct” evidence for the filament formation includes *in situ* transmission electron microscopy [57] and detection of local enhanced conductivity [58, 59]. Another alternative way – though “indirect” – could be the observation of “quantized conductance” in the electrical conductance plot in *ballistic* transport regime. The quantization of electrical conductance in the units of $2e^2/h = (12.9 \text{ k}\Omega)^{-1}$ (where e is the electronic charge and h the Planck constant) is a signature of narrow and short (length scales comparable with conduction electrons' Fermi wavelength) one-dimensional quantum wires or transport channels [60, 61]. Such systems (discovered in late 80 s) are historically known as quantum point contacts (QPCs). The conductance quantization event is interesting not only because it offers rich physics of charge flow and resistive switching, but also it is capable of playing a major role in multilevel memories, quantum information processing, and neuromorphic devices. In RRAM devices, the main transport mechanism is believed to be formation and rupture of nanoscale conductive filaments embedded in an insulating matrix (between two metal electrodes or electron reservoirs). Such nanofilaments in RRAMs resemble typical QPCs. One can now naturally expect quantum size effects—particularly the quantization of electrical conductance, for these filaments. In other words, RRAMs having resistance of the order of 12.9 k Ω or less will tend to have filaments or extended

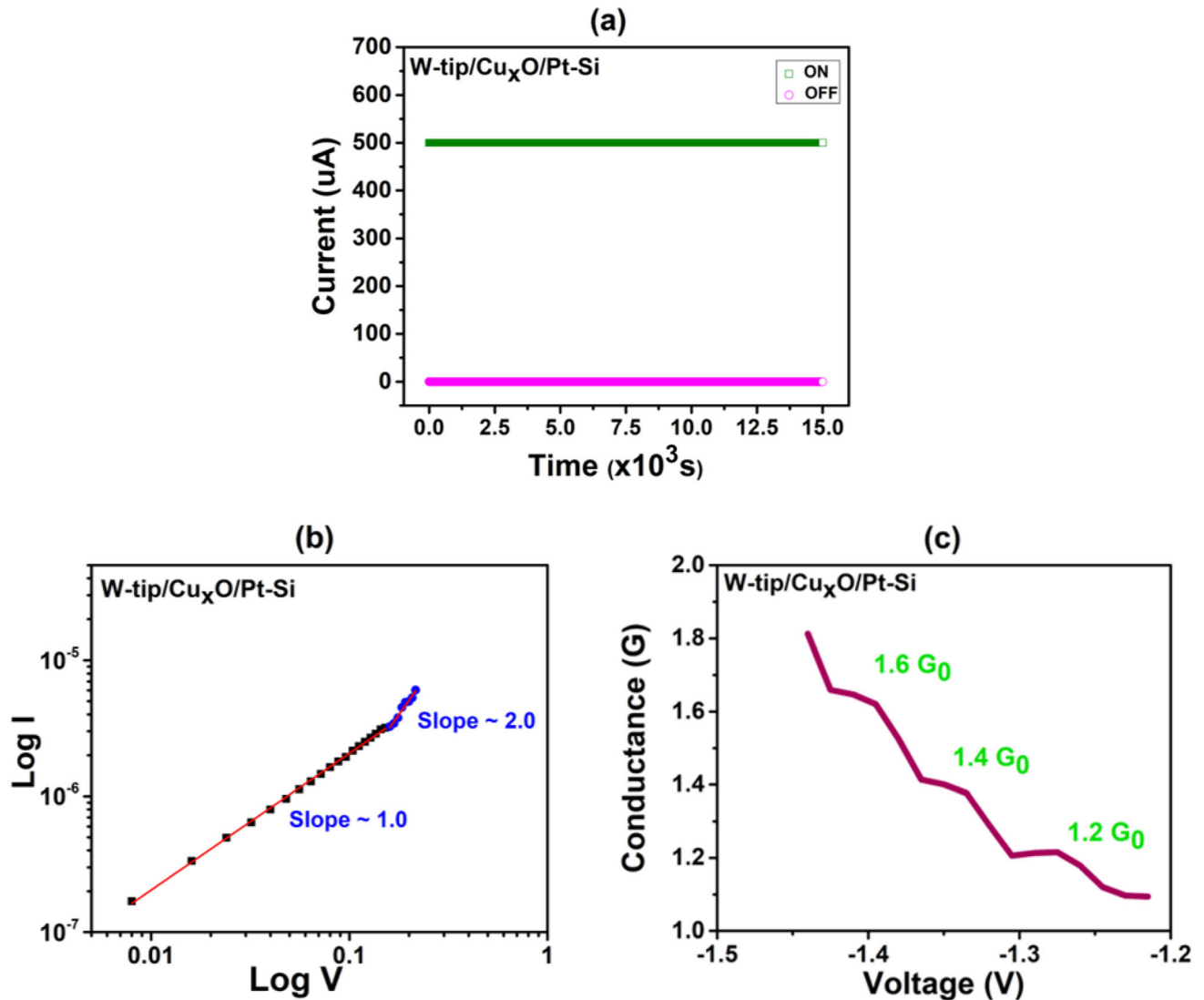


Fig. 5 **a** Time retention characteristics of the resistance states of W tip–Cu_xO device for 15 × 10³ s read at 100 mV **b** Linear fit of Log *I* vs Log *V* curve for HRS with slope of 1 in the low voltage regime and 2 in the high voltage regime, confirming SCLC

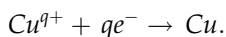
chains, as narrow as a single Cu ion or atom. From our charge transport data, the electrical conductance (*G*) was calculated using $G = I/V$, where *I* is the current through the device and *V* is the voltage applied to electrodes. Conductance was then recorded in units of $G_0 = 2e^2/h$ and plotted as a function of bias voltage *V* applied between TE and BE of our W tip/Cu_xO-based RRAM cells, as shown in Fig. 5 (c). In the past, onset of such quantized plateaus, at conductance values of integer multiple of G_0 [62–64], half-integer multiple of $0.5G_0$ [65, 66], or sometimes even mix of both the levels [65, 67, 68], have been reported for a number of RRAM systems. Furthermore, J.

conduction. **c** Conductance quantization steps in the conductance–voltage (*G*–*V*) plots implying the presence of narrow filamentary conductive channels within the oxide matrix which are capable of facilitating repetitive sweeps between HRS and LRS

J. T Wagenaar et al. observed conductance steps around $0.1G_0$ and $0.3G_0$ in Ag₂S thin-film-based device [63]. In all of these findings, the observed conductance plateaus have been attributed to creation (during SET) and annihilation (during RESET) of conductive nanofilaments inside the switching layer. A typical *G*–*V* plot, as can be seen in Fig. 5 (c), of our W tip/Cu_xO-based devices shows plateaus around conductance values $1.2G_0$, $1.4G_0$, and $1.6G_0$. It is noteworthy that in most of our conductance plots, we did not observe plateaus either at normal integer or at half-integer value of G_0 . There is also a problem with the reproducibility of these conductance steps.

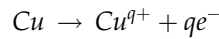
The reason behind this could be the difficulty in controlling the width of the narrow bridge-like atomic constriction (unlike in a well-defined conventional QPC) between the two electron reservoirs, or the possibility of multiple such channels contributing to total conductance of the device at the same time. Therefore, before making the quantization of conductance a useful tool for building multilevel memories, we believe that further work on the device architecture is necessary. This will eventually enable us to use them in future nanodevices in new types of computer architecture.

Taking the onset of quantized conductance steps in our transport data as basis, we explain the RS processes in our Cu_xO -based RRAMs using the concept of formation and rupture (or dissolution) of metallic CFs connecting the top (W tip) and bottom (Pt) electrodes through the dielectric matrix. A. Mehonic et al. [68] argued that the impossibility of maintaining large difference in chemical potentials ($\Delta\mu$) between the two electron reservoirs (TE and BE) can be treated as a characteristic of metallic filaments-based ECM memory cells. Their findings serve as an incentive for us to build our argument around metallic (Cu) filaments formed and ruptured during the RS event (the chemical potential values of W and Pt are very close – 9.75 eV and 9.74 eV, respectively). The electrochemical formation of Cu metal filaments in the active switching layer during SET process and its dissolution during RESET process can be explained through 8w BRS, as elucidated above. The processes underlying the switching in 8w BRS are shown in Fig. 6(a). Here, step (1) shows the initial HRS of the device. The positive voltage applied to the TE pushes the Cu^{q+} ions ($1 \leq q \leq 2$) of oxide matrix towards the BE (cathode) and starts forming the Cu nanofilaments through the electrochemical reduction process, as in the following:



This causes accumulation of Cu atoms at the bottom Pt electrode which will subsequently facilitate gradual formation of CFs towards the top (as shown schematically in Fig. 6(a), step (2)). Further increase in positive bias will finally result in formation of the complete channel connecting the two electrodes (step (3) in Fig. 6(a)). This Cu nano-channel reduces the oxide resistance locally and SET the device from HRS to LRS. This is device ON state. The negative voltage

with relatively high compliance current (10 mA) applied to the TE initiates the joule heating and also the electrochemical oxidation process, as shown in the following:



This dissolves the previously formed Cu nanofilaments from the BE. These Cu ions will drift away from the filament causing its rupture, as we can see in step (4) of Fig. 6 (a). This will RESET the device from LRS to HRS. This is device OFF state. It is important to note that in this switching cycle (which was named 8w BRS beforehand), both the formation and rupture of CFs started from the BE.

During the reversed c8w BRS event, exactly the opposite of what is explained in Fig. 6(a) happens. Step (1) of Fig. 6 (b) shows the HRS. When a negative bias was applied to the top W probe and positive to bottom Pt electrode, Cu ions within the Cu_xO matrix would move towards the TE whereon it undergoes reduction. Thus, filaments of Cu atoms will start growing, as shown in step (2) of Fig. 6 (b). With further increase in bias, this filament connects the TE with the BE; the device will switch from HRS to LRS (step (3) of Fig. 6 (b)). On reversal of the bias polarity, the Cu atoms of the filament undergo oxidation to form ions. These copper ions will move away from the filament causing its rupture. During this reversed c8w BRS, both the growth initiation and rupture of the filament began at the TE. Thus, the regular 8w and reversed c8w BRS observed in our Cu_xO thin-film-based RRAMs can be explained on the basis of formation and dissolution of metallic nanofilaments made of Cu atoms.

Below we present a model to roughly estimate the size of these Cu filaments. Let us consider that the shape of the nanofilaments formed within the Cu_xO solid electrolyte is cylindrical. The energy needed to form the Cu filament, experimentally is given as follows:

$$E_{\text{experimental}} = \sum_{V=0}^{V_{\text{SET}}} (\Delta V \cdot \Delta I) t_d, \quad (2)$$

where V_{SET} is the SET voltage (0.38 V), ΔV is the step voltage (30 mV), ΔI is the current difference ($\Delta I = I_{\text{max}} - I_{\text{min}}$), I_{max} is the current at LRS (filament formation current), I_{min} is the leakage current at the HRS (as shown in Fig. 7), t_d is the time between two data points (100 μs).

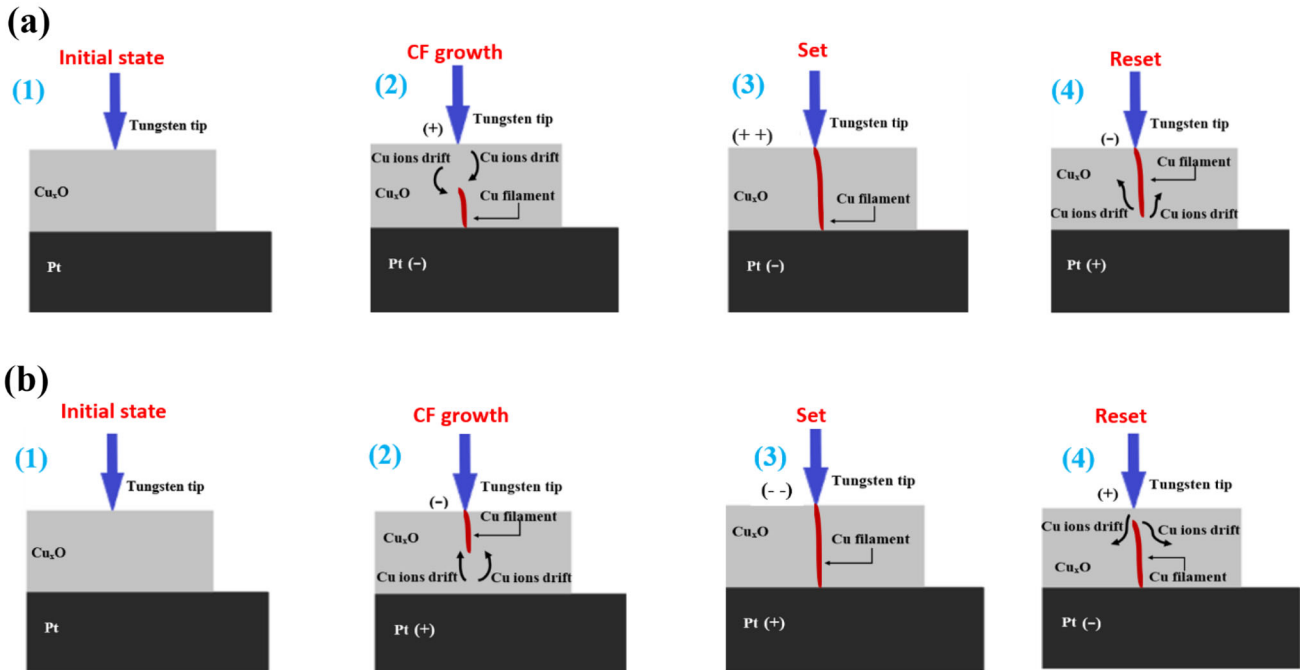


Fig. 6 Resistive switching mechanism for a 8w BRS observed in W tip–Cu_xO device. Step (1) Initial HRS, step (2) Application of positive voltage to TE and negative voltage to BE initiates growth of conductive filament (or channel) from the BE. The filament is formed of Cu atoms which are accumulated at BE via reduction of Cu ions from the Cu_xO matrix. Step (3) With increased voltage, the filament starts growing and finally connects the TE and BE (SET process). Step (4) On gradual reversal of bias polarity Cu atoms of filament near the BE get oxidized to form ions and move away from the filament which then results in rupture of the filament

(RESET). **b** c8w BRS observed in W tip–Cu_xO device. Step (1) Initial HRS, step (2) Application of negative voltage to TE and positive voltage to BE initiates filament growth from the TE. Here, the Cu filament is formed via congregation of Cu atoms at TE by reduction of Cu ions from the Cu_xO matrix. Step (3) With increased voltage, the conductive filament starts growing and connects the TE to the BE (SET process). Step (4) Under reversed voltage Cu atoms in the filament near TE get oxidized to form ions and move away from the filament which results in rupture of the filament (RESET)

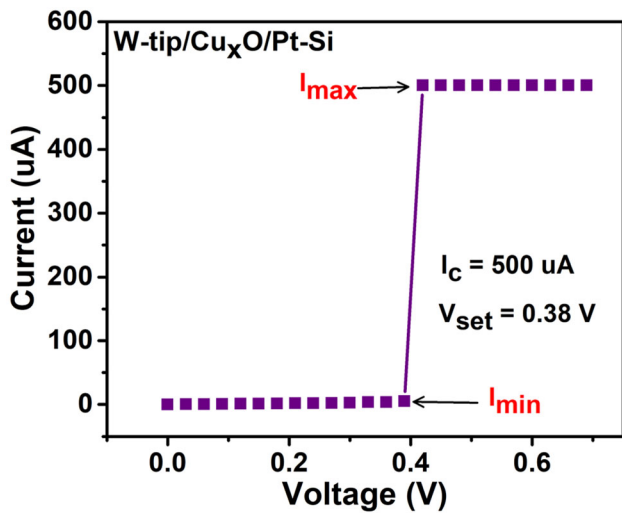


Fig. 7 Typical current–voltage (*I*-*V*) characteristics in the switching regime

The theoretical expression which represents the energy to form the filament is given as follows [69]:

$$E_{Theoretical} = J\phi V_{SET}t_d, \tag{3}$$

$$J = ne\mu_{Cu} \frac{V_{SET}}{L}, \tag{4}$$

$$\phi = \frac{\pi D^2}{4}, \tag{5}$$

where, *J* is the current density, ϕ is the cross-sectional area of the filament, *n* is the electron density in the bulk [70], *e* is the electronic charge, μ_{Cu} is the field effect mobility ($0.05 \times 10^{-4} \text{ m}^2/\text{Vs}^{35}$) [71], and *L* is the length of the filament ($\sim 75 \text{ nm}$).

The filament diameter can be calculated by using the equation as follows:

$$D = \sqrt{\frac{4L \sum_{V=0}^{V_{SET}} (\Delta V \cdot \Delta I)}{ne\pi\mu_{Cu} V_{SET}^2}} \quad (6)$$

We can obtain the resistivity of the cylindrically shaped Cu filament using the equation:

$$\rho_{Filament} = \frac{R_{LRS} \phi}{L} \quad (7)$$

The cylindrical diameter of the Cu nanofilament was calculated to be around 115 nm with a resistivity of 1.4 $\mu\Omega$ cm, which is in corroboration with the reported literature [72, 73]. These estimated values suggest that the conductive channels were formed (during the SET process) and ruptured (during the RESET process) during RS due to oxidation and reduction of Cu ions. This is yet another indirect proof in support of metallic filamentary model for our W tip–Cu_xO cells.

It is important to note that we observed two *coexisting* BRS modes are somewhat similar to the *complementary* RS reported in the past for a number of memory cells [74–76]. The complementary RS is envisaged as an effective route to suppress the unintended sneak (or leakage) current in a 3-dimensional crossbar array of memories that mainly arises due to parasitic paths around neighboring cells [75]. The only difference between the two is that while observing the two distinct coexisting BRS modes, the SET and RESET happened to occur in opposite polarities, whereas in complimentary RS, it happens in the same polarity of applied bias. Additionally, the complementary RS has been usually demonstrated in a slightly complicated device structure composing of two anti-serially stacked bipolar resistive switches [74–76]. In contrast, we have observed the two coexisting BRS modes in a fairly simple metal–insulator–metal architecture. Therefore, it would be interesting to investigate if our observed coexisting BRS modes presented in this work could also be exploited in order to get rid of the sneak current problem in high-density crossbar memory.

Next, let us discuss the RS observed in the cells having structure Cu contact pad/ Cu_xO/Pt/Ti/SiO₂/Si devices. For brevity, we named it Cu–Cu_xO device, as already described in Fig. 1 (c) and (d). In this case, Cu metal acts as the TE and Pt acts as BE.

We observed that the *I*–*V* characteristics of Cu–Cu_xO devices were different from those of earlier W tip–Cu_xO cells. Here, the device showed only

“regular” 8w non-volatile BRS. The device which was initially at HRS changed its state to LRS under a positive voltage applied to the top Cu electrode. The compliance current was set at 500 μ A. The forming voltage was found to be 4.8 V, which is slightly higher than the former device (with W tip as TE). It could be owing to the interface effect which gave rise to more space charge and finally resulting in a large Schottky barrier at metal–insulator interface [77]. The electroforming process is shown in Fig. 8 (a) and its semi-logarithmic counterpart is put as inset image therein. RESET occurred at negative polarity of bias (–0.31 V) applied to the top Cu electrode. The device showed stable regular BRS with SET and RESET voltages less than ± 1 V. The semi-logarithmic *I*–*V* graph in Fig. 8(b) shows 8w bipolar switching in Cu–Cu_xO devices. It is worth taking note of the fact that we observed two coexisting BRS modes (8w and c8w) in opposite bias polarities in the W tip–Cu_xO, and normal regular BRS (8w) in the Cu–Cu_xO cells. It is because, in the former, the switching appears to be a bulk phenomenon and, in the latter, it is an interface event [77] (as Cu contact pads were sputtered on the oxide layer). Also, in Cu–Cu_xO cells, there is a likelihood that the sputtering can locally change the stoichiometry of the Cu_xO matrix, and we conjecture that the switching could be based on orientation of oxygen vacancy sites – a characteristic of EVM memory. Further study on Cu–Cu_xO cells is underway in our group and will be presented as a separate work. It would also be interesting to observe the nature of the switching with application of varied set of top and bottom electrodes at different device operation conditions.

4 Conclusion

In summary, the RRAM based on Cu_xO thin film deposited using DC magnetron reactive sputtering was fabricated and tested using (i) 25 micron diameter size W tip, and (ii) Cu metal contact pads as TEs. The Pt-coated Ti/SiO₂/Si wafers acted as the BE for the both structures. Coexistence of two BRS modes at fairly low switching voltage for more than 110 cycles was observed in the W tip–Cu_xO cells. The resistance ratio was significantly higher ($\sim 10^5$) compared with that published elsewhere [41]. To the best of our knowledge, we also presented the first ever retention metric on Cu_xO-based RRAMs ($\sim 15 \times 10^3$ s). From

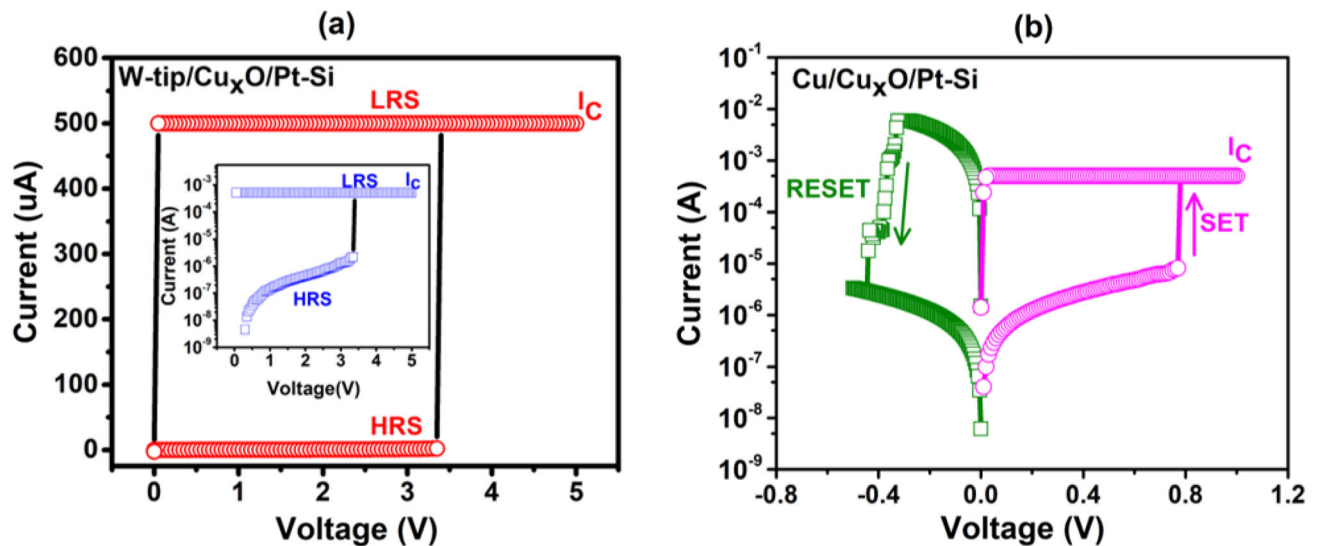


Fig. 8 Current–voltage data obtained from electrical characterization of Cu–Cu_xO devices. **a** Electroforming process with compliance current 500 μ A. Inset figure represents the semi-logarithmic plot **b** I – V plot (semi-logarithmic) of bipolar resistive

the XPS and I – V analysis, we conclude that the RS occurred under electric stimuli due to the reduction and oxidation of Cu ions which eventually helped us build the filamentary model for RRAM operation. The same was further confirmed with the help of resistivity calculation of the Cu nanofilaments. Creation and annihilation of nanometer-size conductive paths or filaments within the oxide layer, which played a pivotal role in observing RS, were accessed with the help of quantization of conductance phenomenon. The underlying transport mechanism was attributed to SCLC. On the other hand, the Cu–Cu_xO devices exhibited only regular 8w non-volatile BRS events. The switching occurred at a low operating voltage (< 1 V). The high retention, low switching voltage, and consistent switching cycles demonstrate Cu_xO-based resistive memory as a potential candidate for stable, low power, highly scalable, and long-term data storage applications.

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switching. SET and RESET processes occurred for opposite polarity of voltages, implying that the device exhibits bipolar resistive switching

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