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Au–Ag binary alloys on n-GaAs substrates and effect of work functions on Schottky barrier height

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ABSTRACT

In this study, I investigated the effect of work function (ϕ_m) of Au_xAg_{1-x} (x = 0, 0.22, 0.37, 0.71 and 1) on the Au–Ag/n-GaAs Schottky diode (SD) parameters. Ag, Au metals and three alloys with different compositions deposited on n-GaAs substrates by the thermal evaporation method. Surface morphologies of the samples were investigated by an atomic force microscope (AFM). Elemental compositions of Schottky contact metals were conducted by energy dispersive X-ray spectroscopy (EDX). Current–voltage (I–V) and capacitance–voltage (C–V) measurements were performed at room temperature. SD parameters such as barrier height (Φ_{b0}), ideality factor (n), series resistance (R_s), and interface state density (D_{it}) of the SD's were calculated from the obtained I–V and C–V data. Experimental results showed that all calculated SD parameters depend on the alloy composition. The lowest mean barrier height value was found as 0.789 ± 0.022 eV for Au/n-GaAs SDs and the highest value was determined 0.847 ± 0.008 eV for $Au_{0.71}Ag_{0.29}$/n-GaAs SDs from I–V measurements. Weak dependencies of barrier height to ϕ_m existed and gap state parameter (S) determined as 0.0526. The S value was close to the Bardeen limit (S = 0) and indicates that the Fermi level was strongly pinned in Au–Ag/n-GaAs SDs. Also, main SD parameters like series resistance (R_s), ideality factor (n), reverse bias barrier height ($\Phi_b{}^{RB}$), doping density (N_d) and density of interface states (D_{it}) were calculated via using different methods from I–V and C–V measurement results. Also, to determine the leakage current mechanism Poole–Frenkel emission (PFE) and Schottky emission (SE) models applied on reverse bias I–V data.

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1 Introduction

Barrier formation mechanisms of metal–semiconductor contacts have been a major research topic since the first discovery of these contacts [1–4]. To accurately identify the current flowing through the contact and determine the operating conditions of the devices, the basic parameter, barrier height (Φ_b), must be defined correctly. The first attempt was realized by Schottky to understand the rectifying behavior of metal–semiconductor contacts [5]. Schottky and Mott subsequently proposed a model for barrier formation and calculating the barrier height [5–7]. According to the Schottky–Mott rule [7], under the ideal condition, the factors affecting this barrier height was an electron affinity of the semiconductor (χ_s) and the work function of metal (ϕ_m), and it was simply expressed as follows;

$$\Phi_b = \phi_m - \chi_s \quad (1)$$

Since the Schottky–Mott rule is rarely verified experimentally, it can be concluded that; interface dipoles do not disappear and play a major role in determining the properties of the metal–semiconductor interface [8]. The ϕ_m value of the metal depends on two components; volume term and surface dipole term, which starts just below the surface of the metal and represents where all bulk properties are the same. Both dipole terms strongly correlate with surface charge distribution and depend on the condition of the surface [9]. Moreover, it was commonly known that, when metal and semiconductor are brought into contact without any interface layer, the atomic sites and charge distributions change, so that the contribution of the surface dipole changes. Louie et al. overcome this situation using the metal's electronegativity instead of the function of the metal [10]. Besides, known that the presence of states at the interface has a significant effect on the formation of barrier height and investigated in many studies [2, 7, 8, 11–16].

Although the Schottky–Mott rule provides accurate estimation of band bending in a semiconductor, the validity of the proposed model, due to the presence of states at the interface between the metal and the semiconductor and the "Fermi level pinning" caused by these finite states, is a matter of discussion especially for some semiconductors [2, 17]. According to this model, if the thin insulating layer exists between a semiconductors and a metal, interface states of semiconductor are occupied by the electrons, create an additional space charge region, and create the potential difference. This potential difference reduces the effect of metals work function on barrier height [17]. Experimentally observed barrier height has a very limited relation to the results of this theory [8, 14, 18]. Few models were proposed to reveal the formation of barrier height in a metal semiconductor contact [2, 11, 19]. Some of these models associate the independence of the barrier height from the ϕ_m with the fermi level pining mechanism caused by high density interface states [2]. Some other models are closely interested in interfacial chemistry and address the interaction of interfacial dipole with bond polarization [11]. However, all proposed models haven't yet emerged to explain the properties of metal–semiconductor contacts precisely, are not complete and usually change with the substrate, metal, substrate cleaning method, metal deposition method, etc. [9]. It is possible to determine the diode parameters (tuning) during the production of diodes to serve a specific purpose. It is sufficient to use metals or semiconductors with different work functions [9, 13, 20, 21].

GaAs has high thermal strength, high electron mobility and high resistance to radiation damage. It also has a direct band gap that allows efficient absorption of light emission and absorption, allowing transistors to operate at very high frequencies, reducing the noise at which higher frequencies tend to reduce electrical signal distortion in electronic circuits. Also, ternary and quaternary alloys created from GaAs utilizing elements like Al, In, P, and SB have properties that complement those of GaAs, which allows adaptability. GaAs is an important substrate material for devices, which is used in both micro- and optoelectronic applications. Also, GaAs is a suitable substrate for a basic component for high-speed and low-power electronics. On the condition that the properties of the semiconductor remain the same (assuming the effect of interface states to be invariant), modifications in the composition of metal should be expected to change the barrier height. Studies using metals with different business functions have shown that, electrical parameters are closely related to these metals [9, 22]. Especially Au and Ag metals are preferred because of their good conductivity properties and good contacts with semiconductor substrates [23–25]. Both Au and Ag have

very similar properties such as conductivity, molar heat capacity, crystal structure, atomic and covalent radius. The miscible in all portions and known as good contact properties with GaAs.

In this study, the effect of modification in the ϕ_m of Schottky contact metal was investigated depending on the composition of alloys. For this purpose, electrical measurements (current–voltage and capacitance–voltage) were performed at room temperature on produced 20 Schottky barrier diodes (SDs) which it was fabricated by using two metals (Ag, Au) and three different alloys on n-GaAs. The characteristic diode parameters of SDs have been determined and compared with each other. The pinning position of the Fermi level and density of interface states (D_{it}) have been determined and the validity of the Schottky–Mott rule for the Au–Ag/GaAs was tested.

2 Experimental procedures

The n-type GaAs substrate used in this study was grown by the LEC method and Te-doped with a carrier concentration of 2–5 × 10^{17} cm^3. To remove organic contaminations on GaAs substrate was cleaned with some solvents (acetone, methanol, trichloroethylene, deionized water) 5 min using ultrasonic agitation in each step. Then, GaAs substrate was immersed in an $HCl:H_2O$ (1:1) etching solution to eliminate the thin native oxide layer on the surface, rinsed with de-ionized water (18 MΩ) and high purity nitrogen gas used for drying. After the etching process, the GaAs substrate was inserted into the metal deposition chamber immediately.

The Ohmic contacts and transfer length method (TLM) patterns were built by thermal evaporation of Au–Ge alloy (wt% 12), on the non-polished side of the substrate with a thickness of 200 nm, at 2 × 10^{-6} Torr base chamber pressure and thermally annealed at 350 °C for 2 min. in flowing high purity (5 N) nitrogen gas in a tube furnace. TLM method [26] was used to characterize the electrical contacts, with gaps of 0.25, 0.50, 0.75 mm between 0.7 × 3.5 mm pads. Specific contact resistance (ρ_c), contact resistance (R_c), and the effective length (L_{eff}) derived from the measured I–V data and the calculated total resistance versus gap spacing by TLM and values was 9.899 × 10^{-6} Ωcm^2, 0.510 Ωcm and 0.770 µm, respectively.

The substrate was divided into five parts and the area of each part was approximately 1 cm^2. Each part was immediately inserted into the vacuum chamber of NVTS-400 to form Schottky contacts by thermal evaporation of metals and alloys. The Au_xAg_{1-x} alloys made at tungsten crucibles, using high purity Au (4N5) and Ag (5 N) parts, repeating the melt-cooling cycle at least five times and under vacuum. Alloy composition (x = 0, 0.22, 0.37, 0.71 and 1) was verified by EDX measurements and given in Table 1. Schottky contact metals/alloys thermally evaporated through a tungsten shadow mask on the front side of the wafers with a diode area was 0.785 mm^2. Electrical characteristics of Au–Ag/n-GaAs SDs studied from dc current–voltage (I–V) measurements (measured with the HP4140B picoammeter) and frequency dependent capacitance–voltage (C–V) measurements (measured with Agilent E4980A LCR meter) in the dark and 300 K. The forward and reverse bias I-V measurements evaluated using the standard thermionic emission theory, and Poole–Frenkel and Schottky emission theory. C–V measurement results were also evaluated using diode capacitance, and single frequency approximation for interface state density distribution model. All measurements and calculations were performed with our SeCLaS-PC program [27, 28].

3 Results and discussions

3.1 Work functions and surface morphology of binary Au–Ag alloy

The work function was one of the most basic properties of material surfaces and it directly affects the electrical properties of metal–semiconductor contacts. Although the work functions of metals are well documented for various elements, information about the work functions of alloy surfaces and their dependence on composition is limited [29]. Segregation, especially in alloys, makes it difficult to determine of the work function of the alloys [30]. Generally, Gelatt and Ehrenreich's model was used for determine the work function of the alloy [31–34] in the experimental studies. According to this method, the work function of an alloy in the form of A_xB_{1-x} was,

Table 1 Composition, work function, characteristics diode parameters and standard deviations of the Au–Ag/n-GaAs SDs

	Ag		Au		ϕ_m (eV)	n	$\Phi_b^{(IV)}$ (eV)	I_0 ($\times 10^{-11}$A)
	(wt%)	(at%)	(wt%)	(at%)				
Au/n-GaAs	0.0	0.0	100.0	100.0	5.22 [41]	1.171 ± 0.022	0.789 ± 0.022	41.27 ± 19.30
$Au_{0.71}Ag_{0.29}$/n-GaAs	18.28	29.00	81.72	71.00	5.07	1.158 ± 0.019	0.847 ± 0.008	3.670 ± 1.306
$Au_{0.37}Ag_{0.63}$/n-GaAs	51.23	63.48	48.77	36.52	4.96	1.188 ± 0.022	0.832 ± 0.004	6.412 ± 1.078
$Au_{0.22}Ag_{0.78}$/n-GaAs	66.32	78.24	33.68	21.76	4.65	1.238 ± 0.022	0.825 ± 0.010	8.776 ± 3.947
Ag/n-GaAs	100.0	100.0	0.0	0.0	4.30 [41]	1.255 ± 0.027	0.802 ± 0.006	20.68 ± 4.573

$$\phi_m = x\phi_{m,A} + (1-x)\phi_{m,B} + x(1-x)\left[\frac{(\phi_{m,A}-\phi_{m,B})(\rho_A/\rho_b)-1}{x(\rho_A/\rho_b)+(1-x)}\right] \quad (2)$$

where ρ_A and ρ_B are total densities of states $\phi_{m,A}$ and $\phi_{m,B}$ are the work functions, and of metal A and B, respectively. The density of states at Fermi level depends on electronic specific heat constant $C_e = (1/3)\pi^2\rho k^2 T$. C_e values of Au and Ag are 0.948 and 0.645 mJmol^{-1} K^{-2}, respectively [31]. Contrary to the model proposed by Fain et al. [31], since these electronic specific heat constant values were not close to each other, so work functions could not show a linear variation. When the work functions were considered as 5.22 eV and 4.30 eV for Au and Ag [34], respectively, obtained work functions of alloys were given in Table 1 with the corresponding atomic composition.

The grain size of Schottky contact metals and the condition of the surface of this metal/alloy play an important role in determining the electrical properties [32, 33]. Atomic force microscopy was used to examine the surface morphology of the Au–Ag Schottky contacts on n-GaAs. Figure 1 shows the AFM images of the Au/n-GaAs and Ag/n-GaAs SDs. As shown in Figure, the surface morphology of the SDs was fairly smooth. Root mean square (RMS) roughness of films was found from 20 × 20 µm image area and values were 45.9 nm for Au, 37.8 nm for $Au_{0.71}Ag_{0.29}$, 46.2 nm for $Au_{0.37}Ag_{0.63}$, 29.5 nm for $Au_{0.22}Ag_{0.78}$ and 26.1 nm for Ag. A correlation was not observed between the RMS values of the alloys and metals. However, relatively high RMS values are the result of the island-type metallization process observed during the metallization process [34–36]. The phenomenon of island formation of metals is typically observed between low and high surface energy materials. To minimize the total surface energy of the system, the metals/alloys agglomerates to minimize its surface area and exposes more surface area of the low surface energy materials (surface energies were determined as 0.86 J m^{-2}, 1.51 J m^{-2} and 1.97 J m^{-2} for GaAs, Ag and Au, respectively) [37].

3.2 Forward bias I–V characteristics of the Au–Ag/n-GaAs SDs

The semi-logarithmic forward and reverse I–V characteristics of one Au–Ag/n-GaAs SDs are shown in Fig. 2. As can be seen in Fig. 2, the rectifying properties of the SD depend on the alloy composition and therefore they depend on the work function. These experimental plots analyzed by using thermionic emission theory, assuming the barrier was homogeneous. According to the theory, the flowing current through the diode in the forward bias region (for $V \geq 3kT/q$) is as follows [7, 38];

$$I = I_0 \exp(qV/nkT) \quad (3)$$

and

$$I_0 = AA^*T^2 \exp(-q\Phi_b^{IV}/kT) \quad (4)$$

where I_0, V, n, k, T, A^*, A, q, and Φ_b^{IV} are the saturation current at zero bias, the applied bias voltage, the ideality factor, the Boltzmann constant, the temperature in Kelvin, the effective Richardson constant (8.16 Acm^{-2} K^{-2} for n-GaAs), the effective diode area, the electron charge, and the barrier height, respectively.

In Eq. (4), n is a dimensionless parameter and it is an indicator for the deviation from the theory (ideally equals unity). The experimental values of the n and the Φ_b were determined from slopes and intercepts of the linear regions of the forward bias ln$I$-V plots by using Eqs. (3 and 4). Other calculations and all least square fittings were performed via our computer

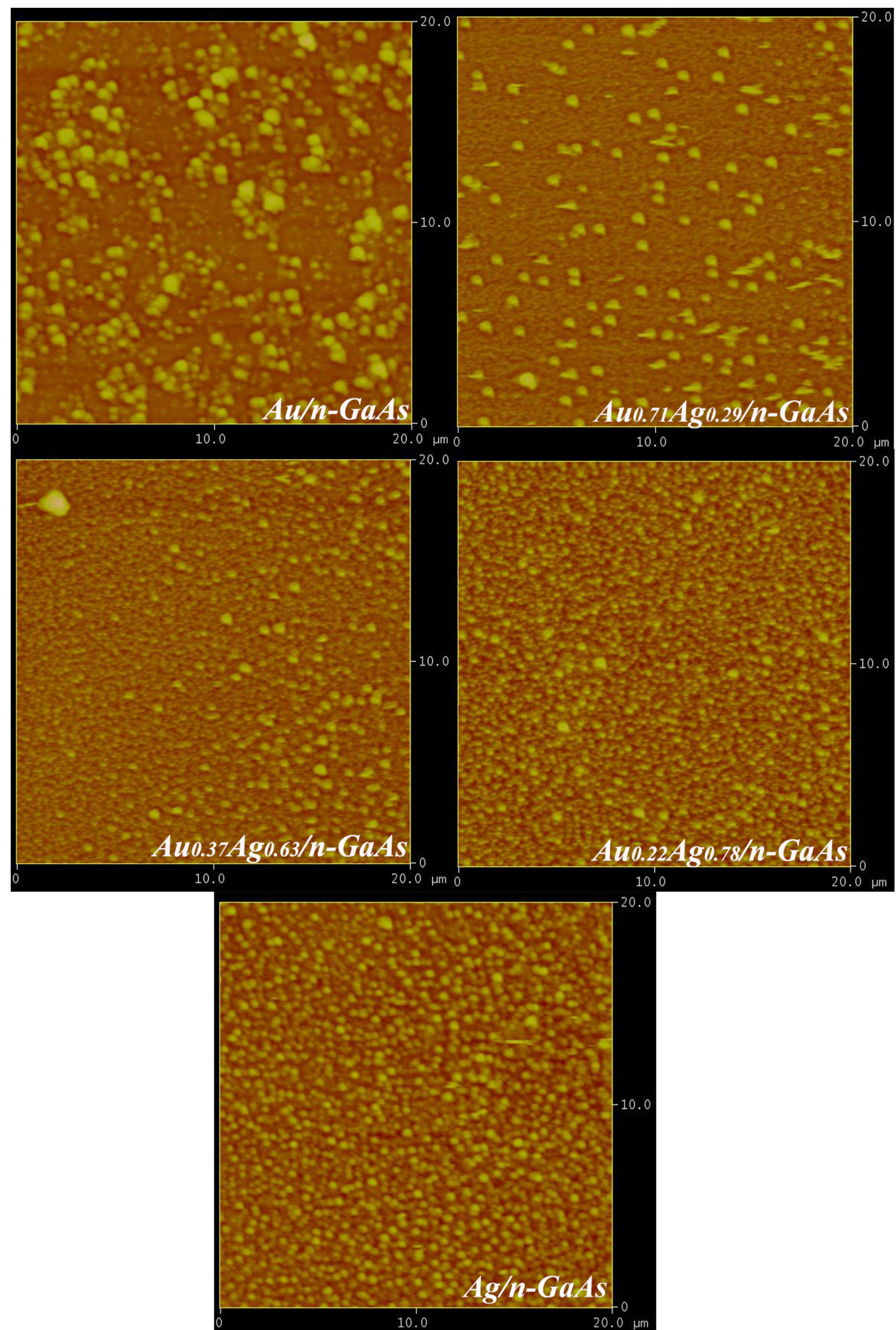

Fig. 1 AFM micrographs of the Au–Ag Schottky contacts to n-type GaAs

program SeCLaS-PC. The values of the Φ_b and n of the Au–Ag/n-GaAs SD varied with alloy compositions (Table 1). As can be seen in Table 1, the ideality factors of Au–Ag/n-GaAs SDs were higher than the 1. This high value of the ideality factors was generally attributed to the existence of a thin oxide layer between metal and semiconductor, surface preparation techniques, Fermi level pinning, and homogeneity of the surface of the semiconductor [33, 39].

Ideally, when the metal and semiconductor are combined to form a contact, the boundary between the metal and the semiconductor is assumed sharp, but in a real situation is different. As stated in previous studies, even if the metallization process was carried out at room temperature, solid-state reactions occur between the metal and the semiconductor [34, 36, 39, 40]. This was more clearly seen in Au/GaAs SDs. Gallide phases formed at the interface

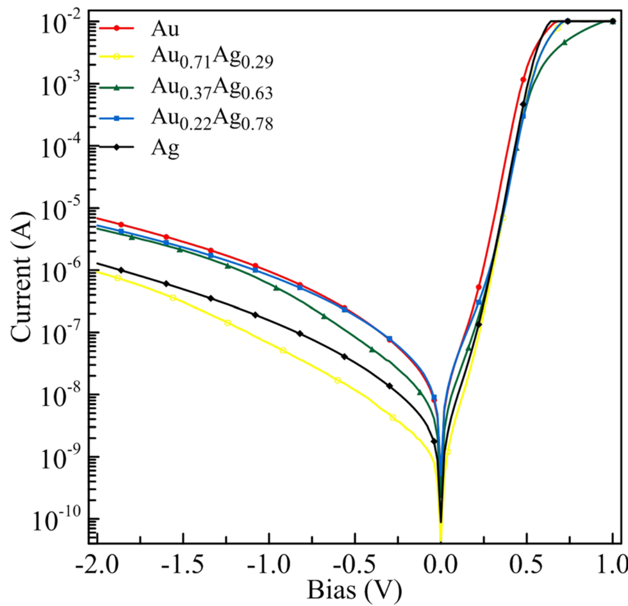

Fig. 2 The semi-logarithmic I–V characteristics for the Au–Ag/n-GaAs SDs. Only one plot is shown here for each set, representing the best value for the average results obtained from the measurements

were known and have a significant effect on both the n and the Φ_b^{IV} [40]. In this study, similar results were obtained for n and the Φ_b^{IV} and these values vary depending on the contact metal/alloy. The ideality factor of SDs decreases when the ratio of silver increased in the alloys. The possible reason for this change may be silver prevents the formation of the gallide phases.

It was a well-known method to incorporate very thin barrier metal films to allow metals of such diffusive nature to make better contact with semiconductors or to achieve diffusion in a controlled manner.

The obtained mean value of barrier height and ideality factor for twenty Au/n-GaAs SDs was 0.789 ± 0.022 eV and 1.171 ± 0.022, respectively. These values are considerably lower than the expected barrier height value. However, many studies have obtained different values for the barrier height of these SDs [21, 42–47]. For example; Tunhuma et al. found these values 0.85 eV and 1.10 for Au/n-GaAs SDs at room temperature [44]. Özdemir et al. found these values 0.742 eV and 1.247 and, Korucu et al. found that 0.79 eV and 1.034 for Au/n-GaAs SDs around the room temperature [45, 46].

The electrical parameters of the diodes depend on the method of cleaning of the substrates [48], the metallization method [49], the etching method [33, 50], etc. Tsukamato et al. worked on photocatalytic properties of alloy (Au–Ag)/TiO_2 junctions [20]. They founded that the work function of the Au–Ag alloy lies at the level intermediate between the monometallic Au and Ag and calculated theoretical energy-band diagram of alloy/TiO_2 junction. According to their results, barrier heights change from 0.2 to 1.3 eV for Ag/TiO_2 and Au/TiO_2, respectively. The alloy/TiO_2 junction, therefore, creates a barrier that is larger than Ag/TiO_2 but smaller than Au/TiO_2. This theoretical calculation does not take into account many parameters that have significant effects on the height of the barrier, such as the presence of interface states, inhomogeneity, interface compounds, doping density, etc. and defines the parameters in an ideal state. However, it is expected/founded to be compatible with the parameters obtained from the experiments. Therefore, it would be more appropriate to evaluate our diodes, which are prepared in identical form and built on the same substrate with the approach that they are consistent among themselves.

When this information was taken into consideration, the change in barrier heights depending on the ϕ_m was given in Fig. 3. Here, the data related to Au/n-GaAs SD not taken into consideration when evaluating the relationship between metal's ϕ_m and Φ_b values (please see inset in Fig. 3). The expected barrier height values could not be observed due to

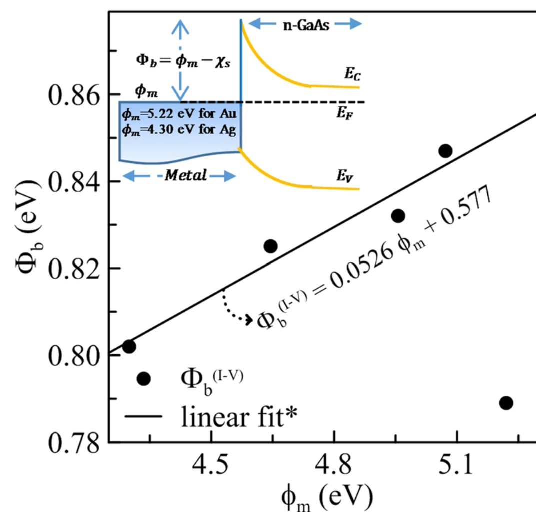

Fig. 3 The-least squares fit the Au–Ag/n-GaAs SDs Φ_b^{IV} and calculated ϕ_m data. * The data of Au/n-GaAs SDs do not include fit range. Insert shows that energy band diagram of Au–Ag/n-GaAs SDs

alloying behavior. This behavior causes the AuGa compounds to change the interface chemistry of the Au-GaAs interface as a result of some Ga out-diffusion and solid-state reactions with Au, and the remaining As atoms make the semiconductor highly doped [40, 51, 52]. The exact alloying mechanism that causes the degradation of the SDs was not very clear. This will result in significant field emissions along the barrier and increase the flow through it [51].

This behavior is also observed in studies on AlGaN or GaN substrates [34]. In this study, although there is no annealing process, Ga migration due to solid-state reactions also observed on the contact surface by EDX measurements.

On the other hand, the presence of a small amount of Ag prevents this diffusion and prevents the gallide phases to occur at the interface [35, 36]. There are many examples in the literature (especially in SD on ternary and quaternary semiconductor substrates) where a thin layer of metal barrier is used to prevent these diffusion/out-diffusion processes [53].

According to the Cowley-Sze's model, barrier height is affected by the density of states at the interface between the metal and the semiconductor and causes a deviation from the Schottky–Mott rule [2]. As mentioned earlier, the slope of linear fit in Φ_b versus ϕ_m graph was an indicator of Fermi level pinning and called as "interface behavior parameter" or "gap states parameter" (S) of the semiconductor [2, 8]. Here, if S = 0 state is called a "Bardeen limit" if the S = 1 state is called the "Schottky limit" [54]. S parameter was determined as 0.0526 and close to the Bardeen limit, in our study. Therefore, surface states or interface states stabilize the Fermi level of the metal–semiconductor system and, depending on the characteristic parameters of the metal, thus Fermi level remains unchanged. In this case, the relationship between the density of the interface states and the S parameter known as a Cowley − Sze equation and given as follow [2],

$$S = \frac{d\Phi_b^{IV}}{d\phi_m} = \left(1 + \frac{q^2\delta D_{it}}{\varepsilon_i}\right)^{-1} \quad (5)$$

where ε_i and δ are permittivity of the interfacial layer and thickness of the interfacial layer, respectively [2, 39, 54, 55]. Assuming the ε_i=5 ε_0 and δ= 5 Å, we calculate D_{it} = 1.801 × 10^{11} eV^{-1} cm^{-2} from S according to the Eq. (5), which has a good agreement with the later results and literature [56].

The downward curvature in I–V curves at relatively high forward bias voltage region arises from the series resistance (R_s), of the semiconductor bulk between the depletion region and Ohmic contact. The R_s values of Au–Ag/n-GaAs SD were calculated using two different methods developed by Cheung's [57] and Norde [58] obtained from the forward bias current equations (Eqs. 3–4).

It is well known that the forward bias I–V plots are linear in the semi-logarithmic scale but these plots deviates from ideality. This deviation arises from the R_S, the interfacial layer and the interface states. Especially, at sufficiently high voltages, downward curvature region in the forward bias I–V plots arises from the series resistance of the neutral region of the semiconductor bulk between the depletion region, interfacial layer and Ohmic contact [59]. According to the Cheung and Cheung theory, the barrier height, as well as other diode parameters such as n and R_s was also could be determined using Cheung's functions;

$$dV/d\ln(I) = nkT/q + IR_S \quad (6)$$

and

$$H(I) = IR_S + n\Phi_b \quad (7)$$

the y-axis intercept and slope of a plot of $dV/d(\ln I)$ versus I gives nkT/q. Also, a plot of $H(I)$ versus I give a straight line with the y-axis intercept equal to $n{\Phi_b}^{Ch}$ (not plotted here) The slope of this plot also provides a second determination of R_s, which can be used to check the consistency of Cheung's approach. The obtained R_S, n and ${\Phi_b}^{Ch}$ of the SDs were given in Table 2. These serial resistance values were consistent with the literature [49, 60, 61].

Another model for determining R_S and barrier height values was proposed by Norde. This model modified by Bohle and it is based on determining the minimum point of the Norde function in case of n = 1 [58, 62]. Unlike the Cheung method, in this method the Norde function was applied to all forward bias region of I–V characteristics. According to the Norde's method, Norde function $(F(V))$ were expressed as in Eq. (8) and where $I(V)$ and γ was a bias dependent current value obtained from the I–V plots and dimensionless integer larger than ideality factor ($\gamma > n$), respectively,

$$F(V) = V/\gamma - kT/q\ln(I(V)/AA^*T^2) \quad (8)$$

and

Table 2 Mean characteristics diode parameters and standard deviations of the twenty (for each set) Au–Ag/n-GaAs SDs obtained from Cheung functions and Norde plots

Schottky Diodes	Rectification ratio (at ± 0.5 V)	Cheung				Norde	
		n	R_S (Ω)	$\Phi_b{}^{Ch}$ (eV)	R_S (Ω)	$\Phi_b{}^N$ (eV)	R_S (Ω)
Au/n-GaAs	20,016.10	1.163 ± 0.059	31.33 ± 10.34	0.785 ± 0.033	31.24 ± 10.47	0.704 ± 0.018	29.66 ± 10.66
$Au_{0.71}Ag_{0.29}$/n-GaAs	37,464.52	1.128 ± 0.022	14.02 ± 4.35	0.856 ± 0.010	13.81 ± 4.23	0.741 ± 0.005	13.61 ± 3.46
$Au_{0.37}Ag_{0.63}$/n-GaAs	25,628.88	1.186 ± 0.044	36.28 ± 11.77	0.824 ± 0.015	36.08 ± 12.04	0.743 ± 0.007	33.31 ± 12.27
$Au_{0.22}Ag_{0.78}$/n-GaAs	12,615.84	1.236 ± 0.041	9.37 ± 4.59	0.820 ± 0.012	8.92 ± 4.69	0.742 ± 0.009	9.33 ± 3.98
Ag/n-GaAs	99,532.42	1.224 ± 0.041	4.37 ± 2.66	0.809 ± 0.012	3.87 ± 2.66	0.719 ± 0.008	5.98 ± 1.65

$$R_S = \frac{kT(\gamma - n)}{qI_{\min}} \tag{9}$$

and also barrier height ($\Phi_b{}^N$) given by the

$$\Phi_b^N = F(V_{\min}) + V_{\min}/2 + kT/q \tag{10}$$

where $F(V_{\min})$ was a minimum point value of $F(V)$, $V_{\min}$ and $I_{\min}$ corresponding voltage and current values. The plots of $F(V)$ versus V for the Au–Ag/n-GaAs SDs using [58, 62]. Mean values of $\Phi_b{}^N$ and R_s of twenty Au–Ag/n-GaAs SD were summarized in Table 2.

As can be seen from Table 2, mean Φ_b and R_s values of SD for each set were found to be consistent with the Cheung's approach and Norde's method. The difference between the some parameters (Φ_b and R_S) may be attribute to nature of methods and difficulties in implementation. Such as, while the Cheung functions (Eqs. 6, 7) are applied only to the nonlinear region of the forward bias, the Norde function (Eqs. 8) is applied to the entire forward bias region. Furthermore, the deviation from thermionic emission theory or the failure to determine the exact value of $F(V_{\min})$ plots may cause such a inconsistency [63].

R_s values of intimate metal–semiconductor contacts without any desired interfacial layer must only arise from the bulk. The higher values of R_s may arise from the contribution of the native oxide layer on the semiconductor surface to the neutral region series resistance plus imperfect Ohmic contact. However, in the process of making Ohmic contacts and SD it has contributed to contact resistance in the alloys resulting from solid-state reactions [49].

If there are interface states that exist between metal and semiconductor and in equilibrium with semiconductor, the ideality factor of the SD will be greater than unity because of these conditions [17]. The density of these states (D_{it}^{IV}) expressed as the following equation;

$$D_{it}^{IV} = 1/q[\varepsilon_i/d(n(V) - 1) - \varepsilon_s/w] \tag{11}$$

Here, d and ε_s are the interfacial layer width and permittivity of the semiconductor, respectively. The depletion layer width was determined from the C–V measurements at a high frequency. Also, $n(V)$ is the ideality factor depending on the bias voltage and given by $n(V) = (q/kT)[V/\ln(I/I_0)]$. In an n-type semiconductor, the energy of the interface states E_{ss} concerning the top of the conduction band (E_c) at the surface of the semiconductor is given by

$$E_c - E_{ss} = q\phi_e - qV \tag{12}$$

where $q\phi_e = \Phi_b^{IV} + (1 - 1/n)qV$. The interface state density distribution profile of the s for Au–Ag/n-GaAs SDs was obtained from the experimental I-V plots and was shown in Fig. 4. For all Au–Ag/n-GaAs SDs there was a slight exponential increment seen in D_{it}^{IV} from the nearly mid-gap towards the bottom of the conductance band. The existence of metallic-like phases causes a smooth transition between the metal and GaAs substrate and homogenous charge distribution at the interface [44, 52, 64, 65]. When the amount of Ag increased in the alloy, the diffusive nature of Au also deteriorates and Ag prevents the formation of gallide phases. Because, Ag tends to form less gallide phase than Au. Therefore, the Au content in the alloy creates a smaller amount of gallide phase (with GaAs substrate) and density of interface states increases. These

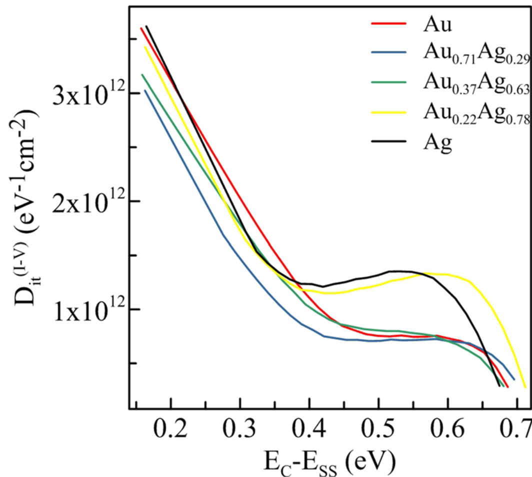

Fig. 4 D_{it}^{IV} versus E_C–E_{SS} plots for Au–Ag/n-GaAs SDs

increasing D_{it}^{IV} values with the Ag content support our proposed approach for interface chemistry by a Ga out-diffusion.

3.3 Reverse bias I–V characteristics of the Au–Ag/n-GaAs SDs

Reverse bias I–V characteristics could also be used to determine some parameters of the fabricated Au–Ag/n-GaAs SDs. Figure 2 reveals that the reverse current (I_R) of the Au–Ag/n-GaAs SDs increases with increasing bias, but is not saturated. Different mechanisms cause a leakage current and become effective. The reverse current conduction mechanism of Au–Ag/n-GaAs was investigated based on the Poole–Frenkel emission (PFE) and Schottky emission (SE) models [38, 66]. The reverse bias current as a function of the negative bias can be written as

$$I_R = I_{0R}\exp(\beta_{SE}V^{1/2}/kTd^{1/2}) \quad (13)$$

here

$$I_{0R} = AA^*T^2(-\Phi_b^{RB}/kT) \quad (14)$$

where I_{0R}, β_{SE} and $\Phi_b{}^{RB}$ are reverse saturation current, SE field-lowering coefficient and reverse bias barrier height ($\Phi_b{}^{RB}$), respectively. The theoretical values of field lowering coefficients given by

$$\beta_{PF}^* = 2\beta_{SE} = [q^3/\pi\varepsilon_s\varepsilon_0]^{1/2} \quad (15)$$

where β_{SE} is the field-lowering coefficient of SE [67]. According to Eq. (15), the theoretical values of the field lowering coefficients ($\beta_{PF}{}^*$) for the Au–Ag/n-GaAs SDs were determined as 4.412×10^{-5} eVm$^{1/2}$ V$^{-1/2}$. Mean values of $\Phi_b{}^{RB}$ and β_{PF} values of twenty Au–Ag/n-GaAs SD were summarized for each set in Table 3. As can be seen from Table 3, values of experimental slope for the Au–Ag/n-GaAs SDs are changes from 1.375 ± 0.068 to 1.560 ± 0.209 eVm$^{1/2}$ V$^{-1/2}$, which were closely matched with the theoretical slope of SE. Thus, the dominating charge conduction mechanism for the Au–Ag/n-GaAs SDs is assumed the SE.

3.4 C–V characteristics of the Au–Ag/n-GaAs SD

The bias-dependent C–V characteristics of the Au–Ag/n-GaAs SDs were measured at dark and room temperature. Figure 5 shows a plot of C^{-2} as a function of bias voltage for the Au–Ag alloy (at.% 0–100) on n-GaAs SDs at sufficiently high frequency (1 MHz or above). The main purpose of these C–V measurements was to reveal the properties of the space charge region of SDs. The relationship between the capacitance of the space charge region and the applied reverse voltage (V_r) in metal–semiconductor contacts given as follows [7, 12],

$$1/C^2 = \frac{2(V_{bi} - kT/q - V_r)}{A^2qN_d\varepsilon_s} \quad (16)$$

where V_{bi} was the built-in potential and N_d was the doping concentration of the GaAs substrate. According to Eq. (16) ($1/C^2$) versus V_r plots give a straight line with the slope were equals to $2/q\varepsilon_sN_d$ and intercepts the x-axis equals to V_0 (Fig. 5). Here; V_0 is related with the built-in potential V_{bi} by the equation $V_{bi} = V_0 + kT/q$ and barrier height were given by equation [7],

$$\Phi_b^{CV} = V_{bi} + V_n \quad (17)$$

where V_n is the potential difference between the bottom of the conduction band and the Fermi level in the neutral region of n-GaAs and $V_n = (kT/q)\ln(N_c/N_d)$, where N_c is the effective density of states in the conduction band of GaAs and its value was calculated from the $N_c = 2(2\pi m^*/kT/h^2)^{3/2}$, and $m^* = 0.063m_0$, and found 4.573×10^{17} cm^{-3} for GaAs at 300 K. The values of $\Phi_b{}^{CV}$ and N_d for the Au–Ag/n-GaAs SDs were given in Table 4. In Table 4, the barrier heights obtained by the C–V method of the SDs were changed between the 1.035 ± 0.022 and 0.912 ± 0.013 eV. These obtained barrier height values are higher than obtained from I–V measurements

Table 3 Mean characteristics diode parameters and standard deviations of the twenty (for each set) Au–Ag/n-GaAs SDs obtained from reverse bias I-V plots

Schottky diodes	Model	β_{PF} (× 10^{-5} eVm$^{1/2}$ V$^{-1/2}$)	Φ_b^{RB} (eV)	I_0 (× 10^{-8} A)
Au/n-GaAs	Schottky emission	1.450 ± 0.160	0.671 ± 0.022	5.507 ± 9.509
$Au_{0.71}Ag_{0.29}$/n-GaAs	Schottky emission	1.502 ± 0.122	0.715 ± 0.024	0.939 ± 1.036
$Au_{0.37}Ag_{0.63}$/n-GaAs	Schottky emission	1.540 ± 0.198	0.704 ± 0.026	1.305 ± 0.888
$Au_{0.22}Ag_{0.78}$/n-GaAs	Schottky emission	1.375 ± 0.068	0.677 ± 0.036	6.832 ± 10.02
Ag/n-GaAs	Schottky emission	1.560 ± 0.209	0.711 ± 0.040	1.848 ± 3.170

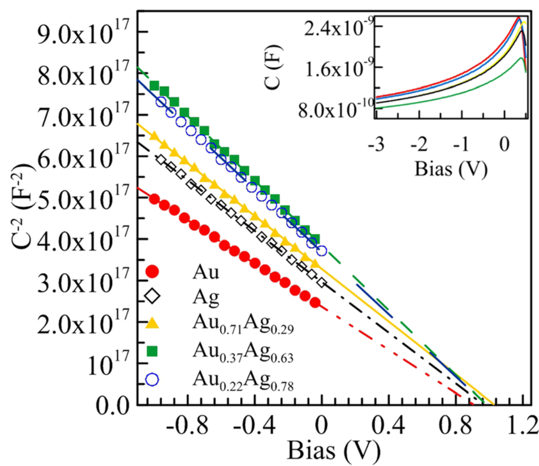

Fig. 5 The C^{-2} versus reverse bias characteristics for the Au–Ag/n-GaAs SDs. Only one plot is shown here for each set, representing the best value for the average results obtained from the measurements. Inset shows C–V characteristics for the Au–Ag/n-GaAs SDs at 1 MHz

from C–V measurements [33, 34]. Arulkumaran et al. prepared Au/n-GaAs and Ag/n-GaAs SDs and barrier height values varied from 0.82–0.93 eV and from 0.75 to 1.05 eV, respectively [47]. Also, barrier heights found here were reasonable agreement with a value of 0.97 eV from C–V characteristics of Au/n-GaAs and Ag/n-GaAs of nearly the same doping concentration [15].

Although the same parameter was measured, the difference between the Φ_b^{CV}'s can be attributed to the existence of lateral inhomogeneity [69]. The source of this lateral inhomogeneity was potential fluctuations at the interface. These fluctuations generally attributed to the thickness of the contact metal, non-uniform distribution at the interface, dislocations, packing errors in the crystal and a thin native oxide layer at the interface, irregularities in the atomic scale on the semiconductor surface, and defects in bulk,

Table 4 The obtained characteristics diode parameters and standard deviations of the Au–Ag/n-GaAs SDs from the C-V measurements

Schottky diodes	N_d (× 10^{17} cm^{-3})	V_{bi} (V)	Φ_b^{CV} (eV)
Au/n-GaAs	9.103 ± 0.836	0.909 ± 0.012	0.912 ± 0.013
$Au_{0.71}Ag_{0.29}$/n-GaAs	8.288 ± 0.789	1.032 ± 0.022	1.035 ± 0.022
$Au_{0.37}Ag_{0.63}$/n-GaAs	6.939 ± 0.413	0.998 ± 0.025	1.001 ± 0.025
$Au_{0.22}Ag_{0.78}$/n-GaAs	6.886 ± 0.672	0.976 ± 0.007	0.980 ± 0.007
Ag/n-GaAs	8.097 ± 1.235	0.959 ± 0.013	0.963 ± 0.013

corresponding to each alloy composition. The difference between the Φ_b^{CV} and Φ_b^{IV} may be attributed to the lateral inhomogeneity at the interfaces [68]. This lateral inhomogeneity can cause potential fluctuations at the interface. Capacitance is not sensitive to this potential fluctuations but the dc current across the interface depends exponentially on. Any lateral variation in the barrier height causes the current to flow preferentially through the barrier minima. Therefore, the values of barrier height obtained from I–V measurements are lower than those obtained and so on [69, 70]. These potential fluctuations affect the dc current and the capacitance measurements in different ways. Diode capacitance was caused by the displacement of the charge carriers in the space charge region due to the ac frequency signal. This displacement was observed near the boundaries of the space charge region. Therefore, the capacitance of the diodes depends on this space charge region and causes the barrier height to be measured only as an average value. The dc current flowing through the

diode preferably tends to flow only where the Φ_b^{CV} was the lowest.

Besides the I-V measurements, using a single-frequency approximation method [71] on the conductance measurements results, allows the estimation of the D_{it}. This method was one of the reliable ways to determine the density of interface states. According to this method, D_{it}^{CV} can be found using the following formula,

$$D_{it}^{CV} = \frac{2}{qA} \frac{(G_m)_{max}/\omega}{((G_m)_{max}/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2} \tag{18}$$

where G_m ω are measured conductance and angular frequency of ac signal, C_m is measured capacitance. C_{ox} is the capacitance of oxide layer in accumulation region of C–V curves, $(G_m)_{max}$ conforms to maximum G–V curve and C_m is the capacitance of the diodes corresponding to $(G_m)_{max}$. Also, the series resistance of the equivalent circuit is [71, 72],

$$R_s = \frac{G_m}{G_m^2 + w^2 C_m^2} \tag{19}$$

This method was applied on C–V and G–V measurement results in the frequency range from 200 Hz to 2 MHz Fig. 6 depicts the changes in D_{it}^{CV} with the frequency, both axes are log scale. D_{it}^{CV} values of Au–Ag/n-GaAs SDs strongly depend on frequencies and decrease at lower and higher frequency range. This "U" type behavior of the interface states has a minimum value that varies from diode to diode.

This minimum value and sufficiently constant D_{it}^{CV} values appear at relatively high frequencies attributed to the excess capacitance. This excess capacitance because of interface states which is in equilibrium with the semiconductor that can easily follow the ac signal [73]. D_{it}^{CV} values of Au–Ag/n-GaAs SDs are same order as those reported by some authors [56].

The frequency dependent series resistance values of Au–Ag/n-GaAs SDs estimated according to Eq. (15) using the measured capacitance and conductance values in the frequency range from 200 Hz to 2 MHz at room temperature and plotted in Fig. 7. This plot indicates that when the frequency decreased, interface states cannot follow the ac signal and each state produces an excess capacitance and conductance and becomes a resistive point for charge carriers and increases exponentially. Inset in Fig. 7 shows that series resistance gives a peak depending on the frequency in the wide negative bias range and the second peak appears after 0 V.

4 Conclusion

In this study, Au–Ag/n-GaAs SDs fabricated by thermal evaporation method and investigated the effect of the work function of metals on SD's parameters. TLM results indicate that Ohmic contact resistance was very low and EDX results indicates

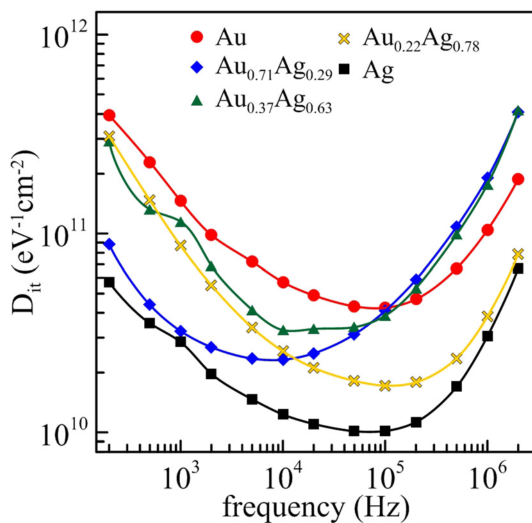

Fig. 6 Mean D_{it}^{CV} values versus ac signal frequency plots of the Au–Ag/n-GaAs SDs

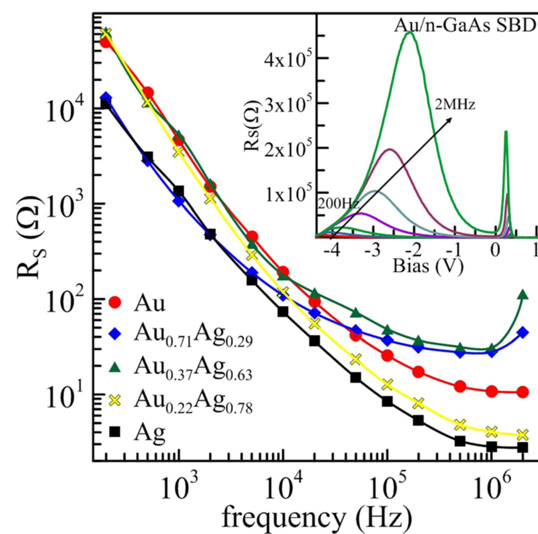

Fig. 7 Mean R_S values versus frequency plots of the Au–Ag/n-GaAs SDs. Inset shows bias dependent R_S values of one of the Au/n-GaAs SD

that the alloy's percentage (x) by weight values were 0.22, 0.37 and 0.71. Also, AFM images showed that smooth contacts were made. Au_xAg_{1-x} (x = 0, 0.22, 0.37, 0.71 and 1) alloys were used for fabricating SDs by following the same cleaning procedure with using the n-type GaAs substrate and then, characterized by various methods and techniques. Also, characteristic parameters of SDs have been determined and compared with each other.

The lowest mean barrier height of about 0.789 ± 0.022 eV in Au/n-GaAs SDs and the highest mean barrier height 0.847 ± 0.008 eV in $Au_{0.71}$-$Ag_{0.29}$/n-GaAs SDs were observed (from I–V measurements). Φ_b values of Au/n-GaAs SDs were lower than the expected value and, explained by the presence of the gallide phases at the interface. It was observed that the Ag was prevented the Au diffusion into the GaAs substrate or out diffusion of Ga. Furthermore, it was found that an almost linear relationship between Schottky barrier height and metal work function (with $\Phi_b^{IV} = 0.0526\phi_m + 0.577$). The gap states parameter (S) was found as a 0.0526 and, close to the Bardeen limit (S = 0). In summary, the Fermi level pinning model proposed by Cowley and Sze applies not only to metal-GaAs contacts but also to alloy-GaAs contacts, and indicates that Fermi level was strongly pinned 0.577 eV below the conduction band in our SD's. In addition, from this dependency, the density of states was determined as 1.801×10^{11} eV^{-1} cm^{-2}. This interface state density value was in the same order of magnitude with the $D_{it}{}^{IV}$ values (calculated from I-V measurement result) and $D_{it}{}^{CV}$ values (calculated from C-V measurement result).

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Declarations

Conflict of interest All the authors declared that they have no conflict of interest.

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