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The effect of thermal annealing on Ti/*p*-Si Schottky diodes

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ABSTRACT

Ti/*p*-Si Schottky barrier diodes (SBDs) have been prepared by metal evaporating method. The effect of low annealing temperature on electrical parameters such as series resistance (R_s), ideality factor (n) and barrier height (Φ_b) of Ti/*p*-Si Schottky diodes was investigated with the help of current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) characteristics. Schottky diodes have been annealed at temperatures from 50 to 200 °C for 1 min in N_2 atmosphere. Φ_b, R_s and n were determined using Cheung and Norde functions in current–voltage characteristics. The Schottky barrier height of the as-deposited contact is found to be 0.747 eV (*I*–*V*), 1.038 eV (*C*–*V*), 0.622 eV [H(*I*)–*I*] and 0.786 eV [F(*V*)–*V*] and ideality factor as 1.3 (*I*–*V*) and 3.55 [$dV/d(\ln I)$–*I*]. It has been seen that the barrier height, ideality factor and series resistance have changed with increasing annealing temperature up to 200 °C.

1 Introduction

Schottky diodes, which are used in many applications in semiconductor technology, have been the focus of extensive theoretical and experimental studies in recently. The thermal stability and repeatability of Schottky contacts properties and formation of a quality Schottky barrier are fundamental conditions for the development of many advanced devices [1–7]. Schottky barrier height controls the current flow through metal–semiconductor (MS) interfaces and is significant to the efficient operation of each semiconductor device. Therefore, any mechanism affecting the Schottky diode will also affect the performance of the devices with which it is located.

Electronic characteristics of Schottky diodes such as barrier height, series resistance and ideality factor are investigated to examine the performance of Schottky contacts. The effects of factors such as annealing [8–13], radiation [14], temperature [7, 15–17] and pressure [5, 18, 19] on diode parameters are investigated. At the same time, in order to examine the performance of Schottky diodes, an interface layer between semiconductor and metal was formed and diode parameters are examined [20–24]. Many researchers have used variety metals to form Schottky contacts to *p*-type Si, e.g., Mn [5], Cu [6], Ni

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[7], PtSi [17], Zr [25], Ti [26], Al [27], Ag [28], Sn [29]. Wang et al. [8] investigated the thermal annealing properties of Gr/Si Schottky diode. They found that the values of diode parameters such as barrier height, ideality factor and series resistance decreased after annealing. Five days after annealing, they examined the *I–V* characteristic again and compared it with the results before and after annealing and found that the diode parameters increased [8].

Mo/SiC Schottky contact fabricated by facing targets sputtering system was thermally annealed at a temperature range of 300–400 °C for 10–30 min [30]. Electrical parameters of Mo/SiC Schottky diode were found from forward current–voltage characteristic curve using Cheung and Norde functions. Increase in the ideality factor with annealing temperature and time, but a slight decrease in SBH was reported by Hong et al. [30]. They found that there is a series resistance in proportion to annealing temperature and time, a decrease in the values calculated from the Cheung method but an increase in the values calculated from the Norde method [30]. Yıldırım et al. [31] annealed the Ni/GaAs Schottky contact at 600 °C and 700 °C and examined the temperature-dependent current–voltage properties. They found that as the annealing temperature increased, the barrier height values first increased and then decreased. But they calculated that the ideality factor increased with the increase in annealing temperature [31]. In another study on annealing, the effects of annealing time and temperature on the electrical properties and material quality of diodes were investigated [32]. From the *I–V* properties, they found a better ideality factor and less leakage current in reverse bias that when the annealing temperature rises up to 500 °C for a duration of 30 min [32].

The electrical properties of Schottky barrier diodes that change with the effect of annealing are of great attention for scientifically and technologically [13]. Only a few studies focused on analysis of the thermal stability properties of SBD, which is complementary and important to their electrical performance [8–13]. For this reason, it is essential to study SBD thermal stability behavior to achieve Si-based SBD for a variety of electronic applications.

In this paper, the electrical properties of Ti/*p*-Si Schottky contacts have been examined for the effects of low annealing temperatures using *I–V* (current–voltage) and *C–V* (capacitance–voltage) characteristics. The effect of thermal annealing dependency of main parameters obtained by different methods was investigated.

2 Experimental details

In this work, a *p*-Si semiconductor with the (100) orientation and polished on one side was used. The RCA cleaning procedure [3, 17] was used to clean the Si semiconductor. Then, the semiconductor is immediately placed inside the deposition chamber. Ohmic contacts are produced by evaporation of Al on the back of the substrate when vacuum was decreased by 10^{-5} Torr. The ohmic contact thickness formed on the semiconductor is approximately 1500 Å. A low resistance ohmic contact was formed by a temperature treatment at 570 °C for 3 min in N_2 flowing in the next process. The Schottky diodes were produced by evaporation of Ti dots with diameter of about 1 mm and a thickness of about 1500 Å. Ti/*p*-Si diode has been annealed at temperatures from 50 to 200 °C for 1 min in N_2 atmosphere. The current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics of Ti/*p*-Si/Al Schottky diode were obtained by using a Keithley 487 picoammeter/voltage source and HP model 4192A LF impedance analyzer at room temperature.

3 Results and discussion

The *I–V* plots of Ti/*p*-Si Schottky diodes are shown in Fig. 1. All the forward bias and reverse bias *I–V* graphs of the Ti/*p*-Si Schottky diodes with 50 °C steps in the 0–200 °C annealing temperature range are shown in the same graph (Fig. 1). *I–V* plots were investigated accordingly TE (thermionic emission) theory and current is determined by relationship [33]

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{qV}{kT}\right)\right]. \quad (1)$$

Here, n is the ideality factor, V is the applied voltage, k is the Boltzmann constant, T is the temperature in Kelvin, q is the electronic charge and I_0 is the saturation current and is given by

$$I_0 = AA^* \exp\left(-\frac{q\Phi_b}{kT}\right) \quad (2)$$

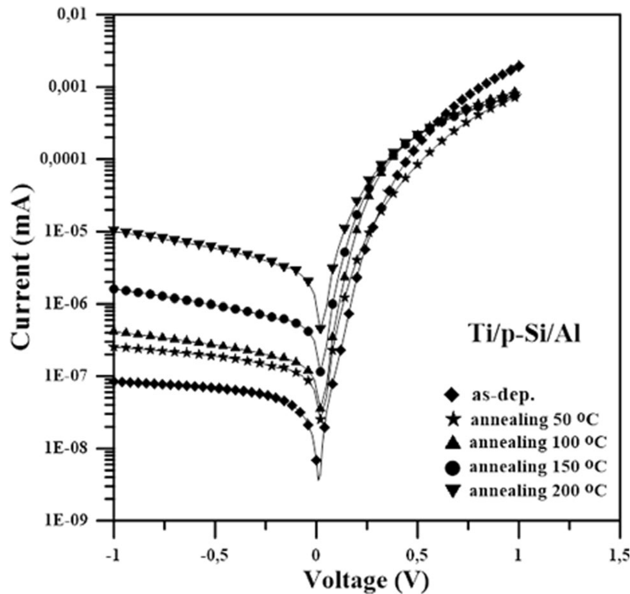

Fig. 1 The semi-log forward and reverse bias current–voltage characteristics of Ti/*p*-Si Schottky diode as a function of annealing temperature

where A is diode area (7.85×10^{-3} cm^2), A^* is the Richardson constant (p-type Si = 32 A/cm^2 K^2 [7]), Φ_b is BH (barrier height) and is defined:

$$\Phi_b = \frac{kT}{q}\ln\left(\frac{AA^*}{I_0}\right). \quad (3)$$

n can be defined as:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right). \quad (4)$$

Φ_b and n values of the Ti/p-Si Schottky diode were determined using Eqs. (3) and (4), respectively. The experimental values of Φ_b and n for unannealed sample were obtained to be 0.747 eV and 1.3 from Fig. 1, respectively. If the ideality factor $n > 1$, it expresses the deviation from the ideal diode. The higher values of the ideality factor can be assumed to be caused by the effects of the interface states, series resistance, and the interfacial thin natural oxide layer and the barrier inhomogeneities at metal–semiconductor interface [3, 29, 34]. Also, the image-force effect, tunneling and recombination–generation may be possible mechanisms that could lead to an ideality factor value greater than unity [5, 25]. Shahryari et al. [35], by examining the I–V properties of Ti/p-Si diode, found the values of n, Φ_b and R_s at room temperature. They calculated n, Φ_b and R_s values as 2.88 and 2.07 [$dV/d(\ln I)$–I, I–V], 0.91 eV, 0.86 eV and 0.89 eV [F(V)–V, I–V, H(I)–I), 19.22 kΩ, 32 kΩ and 30 kΩ (F(V)–V, H(I)–I, $dV/d(\ln I)$–I], respectively. They defined the total series resistance as the substrate resistance, the resistance of the metal contact layers (Ti and Al) and the natural oxide layer, which is the sum of both superficial and interfacial layers [35].

Ti/p-Si Schottky diode annealed in the annealing temperature range 50–200 °C in steps of 50 °C. The experimental values of the barrier height and ideality factor obtained I–V measurements for the Ti/p-Si Schottky diodes change from 0.660 eV and 1.25 (at 50 °C) to 0.560 eV and 2.25 (at 200 °C), respectively. The calculated values of the barrier height (Φ_b) and ideality factor (n) are given in Table 1. The barrier height and ideality factor versus annealing temperature graphs for the Ti/p-Si Schottky diodes are demonstrated in Fig. 2. There is a decrease in Φ_b values after thermal annealing. In the studies in the literature, it was found that the barrier height decreased due to the increasing annealing temperature [15, 36, 37]. Aboelfotoh [15] examined the Ti/p-Si Schottky diode depending on annealing and temperature and calculated the ideality factor and barrier height by annealing at 673 K (400 °C), 773 K (500 °C) and 873 K (600 °C). For the unannealed and annealed at 873 K, the ideality factors were 1.13 and 1.09 and the barrier height values were 0.623 eV and 0.504 eV, respectively (at a temperature of 295 K). It was found that the barrier height decreases with increasing annealing temperature [15]. The reduction in BH may be due to the thermal generation of carriers on the semiconductor side [38]. Thermally produced carriers increase with increasing annealing temperature and neutralize immobile charges on the semiconductor side. Therefore, as the annealing temperature increases, the barrier height decreases. In the ideality factor calculated from the I–V characteristic, first decrease and then an increase were observed with the increase in the annealing temperature. Φ_b (barrier height) calculated from the I–V characteristic decreased with the increase in the annealing temperature. Similarly, Padma et al. [39] found that with increasing annealing temperature, n first decreased and then increased. Co/n-GaN SBD was investigated for the electrical properties at different annealing temperatures (400 °C and 600 °C) by Orak et al. [34]. They calculated that n and Φ_b first decreases and then increases with the effect of annealing. They found that R_s decreased with increasing annealing temperature [34].

Table 1 Annealing temperature-dependent values of various diode parameters determined from *I–V* measurement of Ti/*p*-Si Schottky barrier diodes

Parameters	Unannealed	50 °C	100 °C	150 °C	200 °C
From *I–V* characteristics					
Barrier height (eV)	0.747	0.66	0.655	0.605	0.56
Ideality factor	1.3	1.25	1.14	1.54	2.25
From Cheung's method					
dV/d(ln*I*) versus *I*					
Series resistance (Ω)	141.13	379.64	556.76	655.09	676.82
Ideality factor	3.55	4.25	3.20	3.36	3.63
H(I) versus I					
Series resistance (Ω)	152.83	389.13	574.10	669.24	687.54
Barrier height (eV)	0.622	0.612	0.597	0.587	0.576
From Norde method					
Series resistance (Ω)	3232.7	3037.7	1874.7	1205.8	1012.5
Barrier height (eV)	0.786	0.773	0.745	0.702	0.630

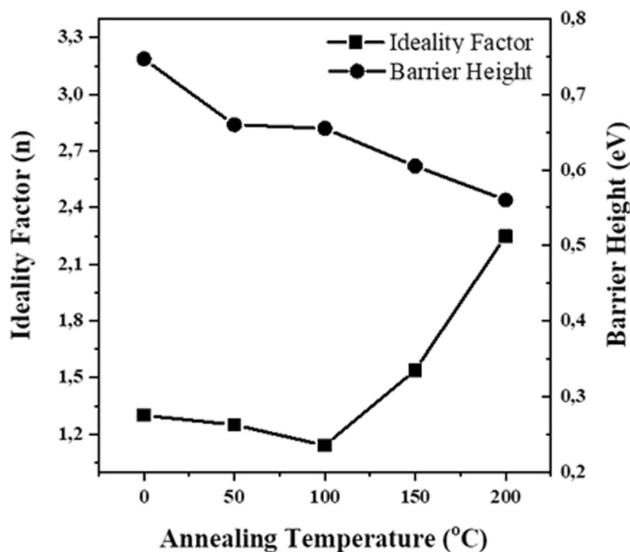

Fig. 2 The ideality factor versus annealing temperature and barrier height versus annealing temperature for the Ti/*p*-Si Schottky diodes

Methods for extracting information for n, Φ_b and R_s values of Schottky diodes were proposed by Cheung and Cheung [40] and Norde [41]. The Schottky diode parameters were calculated using functions of Cheung and Cheung [40]. Cheung's functions can be explained as follows:

$$\frac{dV}{d(\ln I)} = \frac{nkT}{q} + IR_s \quad (5)$$

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \quad (6)$$

$$H(I) = IR_s + n\Phi_b. \quad (7)$$

Experimental graphs of $dV/d(\ln I)$ vs I and $H(I)$ vs I for Ti/*p*-Si Schottky diode at distinct annealing temperatures are given in Figs. 3 and 4, respectively. Equation (5) gives a flat line for the data of nonlinear part of the semi-log forward bias *I–V* characteristics. Hence, the *y*-axis intercepts and slope of the plots of

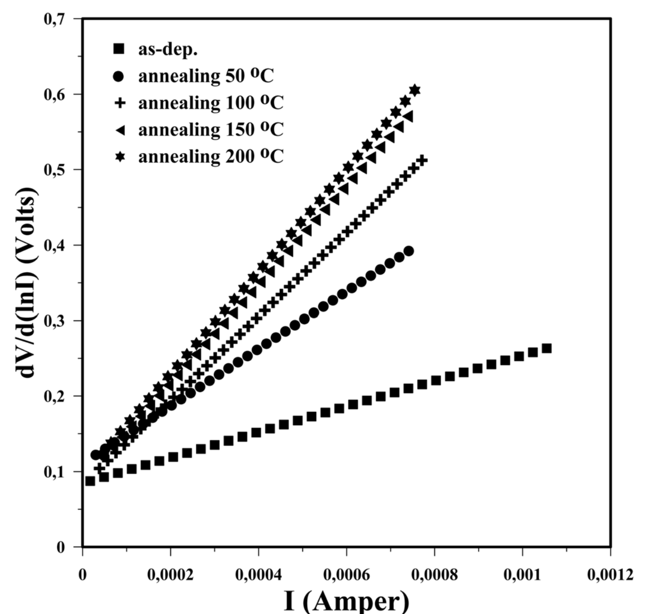

Fig. 3 Plots of $dV/d(\ln I)$ vs I (current) for different annealing temperatures

$dV/d(\ln I)$ vs I will yield R_s and n, respectively. The values of R_s and n from the $dV/d(\ln I)$ vs I graphs are determined to be 141.13 Ω and 3.55 for unannealed, 379.64 Ω and 4.35 for 50 °C, 556.761 Ω and 3.95 for 100 °C, 655.09 Ω and 3.36 for 150 °C, 676.82 Ω and 3.63 for 200 °C, respectively. As seen in Fig. 4, a graph of $H(I)$ versus I was plotted and the resulting graph is in the form of a straight line. The plot's fit equation is found (Eq. 7) and the R_s value is calculated from the slope of the equation, and using the value of ideality factor found from Eq. (5), the $n\ \Phi_b$ value is calculated from the point where the y-axis intercept. The estimated values of R_s and Φ_b from the graph of $H(I)$ vs I are determined to be 152.83 Ω and 0.622 eV for unannealed, 389.13 Ω and 0.612 eV for 50 °C, 574.10 Ω and 0.597 eV for 100 °C, 669.24 Ω and 0.587 eV for 150 °C, 687.54 Ω and 0.576 eV for 200 °C. The series resistance values calculated from $dV/d(\ln I)$ vs I and $H(I)$ vs I graphs increased with increasing annealing temperature. This increase in series resistance is attributed to that electrical compensation of the substrate dopants [40] or many kinetic processes can occur by annealing at the MS interface [42]. Defect generation, defect annealing, interdiffusion, contamination, compound formation, chemical reaction, interface roughening, etc. can form at surface layer of the semiconductor substrate or at MS interface during annealing [42].

The ideality factors obtained from the ln I–V graphs and the $dV/d(\ln I)-I$ graphs are very different from each other. n is determined from the linear regions and from the downward curvature region of the forward bias current–voltage plots of the same characteristics. There is the large difference between n values calculated from $dV/d(\ln I)$–I curve and ln I–V curve. This difference can be attributed to interface states, to existence of series resistance and the voltage drop across the interface layer [3, 39, 40].

Norde method [41] is used to find the values of Φ_b and R_s from forward bias I–V measurements. Norde functions:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^{*}T^{2}}\right). \quad (8)$$

$I(V)$ is current values obtained from the I–V curve, where γ is considered to be the first integer greater than ideality factor n. A graph of $F(V)$ vs V for the Ti/p-Si Schottky contact at different annealing temperatures is shown in Fig. 5. From the plot of $F(V)$ versus V, Φ_b value of Schottky diode can be identified as follows

$$\phi_b = F(V_{\min}) + \frac{V_{\min}}{\gamma} - \frac{kT}{q}. \quad (9)$$

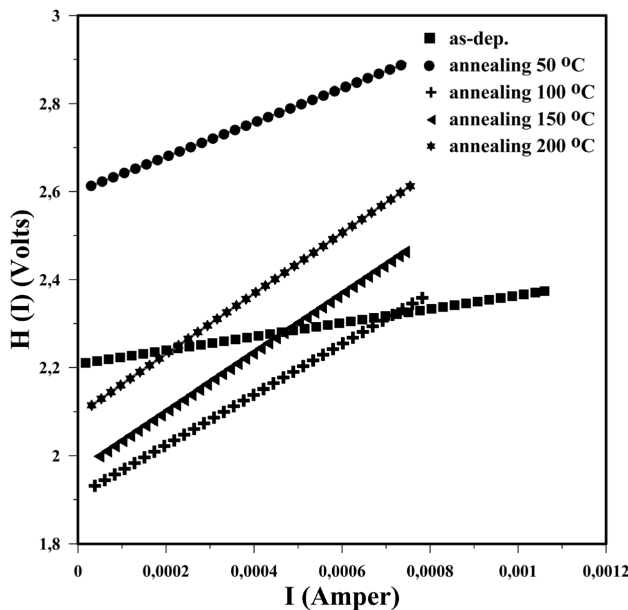

Fig. 4 Plots of $H(I)$ vs I (current) for different annealing temperatures

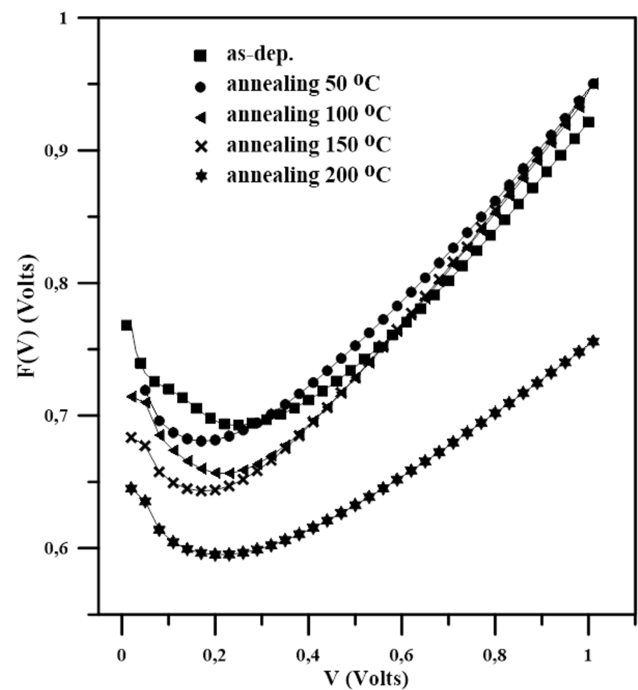

Fig. 5 Plots of $F(V)$ vs V for different annealing temperatures

Moreover, R_s (series resistance) of a Schottky contact is determined using Norde functions,

$$R_s = \frac{(\gamma - n)kT}{qI_{\min}}. \quad (10)$$

The values of $I_{\min}$ and $V_{\min}$ are the current and voltage values at the minimum point [$F(V_{\min})$] of the $F(V)$ graph. From the F(V)–V plot, values of R_s and Φ_b are determined as 3232.7 Ω and 0.786 eV for unannealed, 3037.7 Ω and 0.773 eV for 50 °C, 1874.7 Ω and 0.745 eV for 100 °C, 1205.8 Ω and 0.702 eV for 150 °C, 1012.5 Ω and 0.630 eV for 200 °C, respectively.

R_s and Φ_b calculated from Norde functions and Cheung's functions do not match with each other. Since these methods are applied to different parts of the forward bias I–V plot, the values found are different. Norde functions are valid to the entire forward bias I–V plot of the junctions, whereas Cheung's functions apply only to the nonlinear part of the forward bias I–V properties, namely the high voltage region.

For further study of the contact parameters, C–V characteristics of Ti/p-Si Schottky diodes are measured as a function of annealing temperature and the bias-dependent capacitance was analyzed at a fixed of 500 kHz. C–V plots of Ti/p-Si diode measured of different annealing temperatures are shown in Fig. 6. Figure 7 indicates a graph of $1/C^2$ as a function of reverse bias voltage at the different annealing temperatures. The depletion layer capacitance is determined by,

$$\frac{1}{C^2} = \frac{2(V_d + V)}{\varepsilon_s \varepsilon_0 q A^2 N_A} \quad (11)$$

where N_A is the carrier concentration, A is the diode area, ε_s is the dielectric constant equal to 11.7 for p-Si [43], q is the electron charge, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, V is the reverse voltage, V_d determined by extrapolation of the C^{-2}–V graph to the V-axis, is the diffusion potential. BH is given by

$$\phi_b = V_d + \frac{kT}{q} \ln\left(\frac{N_V}{N_A}\right). \quad (12)$$

Here, N_v is the state density in the valance band (for Si, $N_V = 1.04 \times 10^{19}$ cm^{-3}) [2, 44]. The carrier concentration of Si has been determined to be 3.36×10^{17}, 3.66×10^{17}, 3.52×10^{17}, 3.55×10^{17} and 3.34×10^{17} cm^{-3} at for unannealed, 50, 100, 150, 200 °C, respectively. The obtained Φ_b of Ti/p-Si Schottky diodes for unannealed and samples annealed at 50, 100, 150 and 200 °C is 1.038, 1.166, 1.237, 1.567 and 1.6 eV, respectively.

Figures 6 and 7 show capacitance–voltage and C^{-2}–V graphs of the Ti/p-Si Schottky diode,

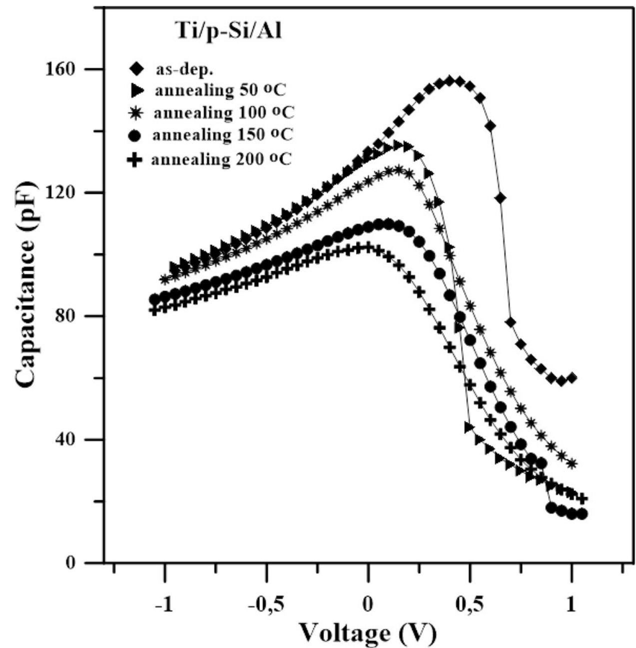

Fig. 6 Experimental reverse and forward bias capacitance–voltage characteristics of Ti/p-Si Schottky diode as a function of annealing temperature 500 kHz

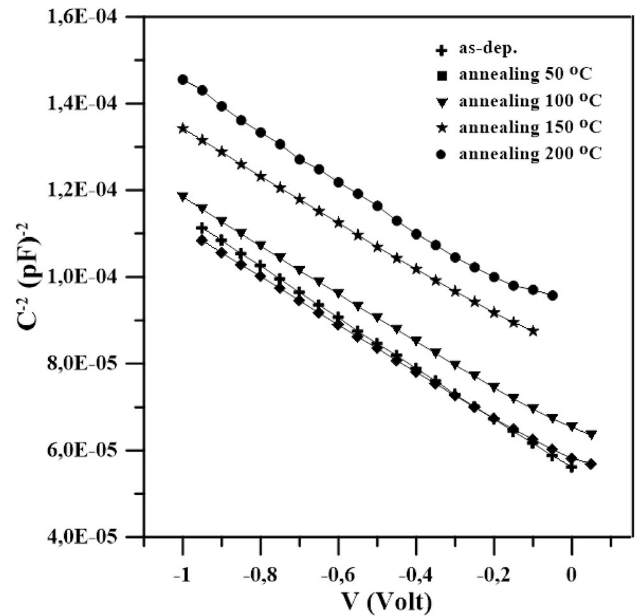

Fig. 7 The reverse bias C^{-2}–V characteristics of Ti/p-Si Schottky diode as a function of annealing temperature

respectively. With increasing annealing temperature, there has been a decrease in the capacitance values and this decrease can be observed in the forward bias region of the graphs (Fig. 6). These peaks are attributed to the distribution of deep states in the gap or to the series resistance and interface [3, 25]. The depletion region capacitance is difficult to measure as the diode is conducting under forward bias. However, the capacitance can be easily measured as a function of the reverse bias. The values of parameters such as Φ_b, E_f, N_a and V_d, were found from the reverse bias C^{-2}–V plot. These parameters calculated from C^{-2}–V plot are reported in Table 2. Φ_b increased with increasing annealing temperature. In his study, Aboelfotoh [15] found that the barrier height values obtained from C–V measurements increased with the increased annealing temperature. The barrier height values at 295 K of the sample which was not annealed and annealed at 873 K was found to be 0.507 eV and 0.582 eV, respectively [15]. Çakıcı et al. [12] annealed the Schottky diode at 100 °C and 200 °C and reported that the barrier height increased depending on the annealing temperature. Reddy et al. [45] calculated the barrier height values of the Schottky diode from the C–V graph and found them as 0.68 eV, 0.74 eV, 0.89 eV, 0.70 eV and 0.82 eV for the samples that were unannealed and annealed at 200, 300, 400 and 500 °C, respectively. Rao et al. [13] annealed the Schottky diode at 200, 300 and 400 °C and calculated the barrier height values from the capacitance–voltage characteristic. They found 0.83 eV, 0.92 eV, 0.96 eV and 0.78 eV for unannealed and annealed samples at 200, 300 and 400 °C, respectively [13]. In their study, Rao et al. [13] and Reddy et al. [45]. It was reported that the barrier height increased in samples annealed up to 300 °C and there was a decrease in samples annealed after 300 °C.

For Schottky diode having interface state in equilibrium with the semiconductor, the ideality factor n becomes greater than unity, and as proposed by Card and Rhoderick, the interface state density N_{ss} is given as [46]

$$N_{ss} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \quad (13)$$

where ε_i and ε_s are the permittivity of interfacial layer and semiconductor, respectively, δ is the thickness of the interfacial layer, W_D is the space charge width and $n(V) = [V/kT/q/ln(I/I_0)]$ is voltage-dependent ideality factor, respectively. The energy of interface states (E_{ss}) with respect to the top of the valence band at the surface of the p-type semiconductor is defined by

$$E_{ss} - E_v = q\Phi_e - qV. \quad (14)$$

Here, Φ_e is the effective barrier height and V is the applied voltage drop across the depletion layer. The energy distribution curves of N_{ss} are estimated from the experimental data of forward I–V characteristics. The plot of N_{ss} versus E_{ss}–E_v for Ti/p-Si Schottky diode is shown in Fig. 8 at different annealing temperatures. As can be seen from Fig. 8, there is an increase in the interface state density from the midgap to the top of the valence band. It is clearly seen from Fig. 8, interface state density decreases with increasing annealing temperature up to 150 °C and then slightly increases upon annealing at 200 °C.

Table 1 gives the estimated electrical parameters of Ti/p-Si Schottky diode by, Norde, I–V, and Cheung methods. As can be seen from Table 1, R_s values calculated in Cheung's functions changed with the effect of annealing, that is, the series resistance values increased. It was determined that R_s values acquired from the Norde function decrease with increasing annealing temperature. The barrier height values determined from the C–V measurements and the values determined from the I–V measurements are different from each other and Φ_b calculated from C–V is higher. The difference in the Schottky barrier height values may be attributed to the barrier

Table 2 Annealing temperature-dependent values of various diode parameters determined from C–V characteristics of Ti/p-Si Schottky diodes

Parameters	Unannealed	50 °C	100 °C	150 °C	200 °C
V_d (eV)	0.95	1.08	1.15	1.48	1.516
N_a (10^{17} cm^{-3})	3.355	3.66	3.52	3.55	3.34
E_f (eV)	0.088	0.086	0.087	0.087	0.088
Φ_b (eV)	1.038	1.166	1.237	1.567	1.6

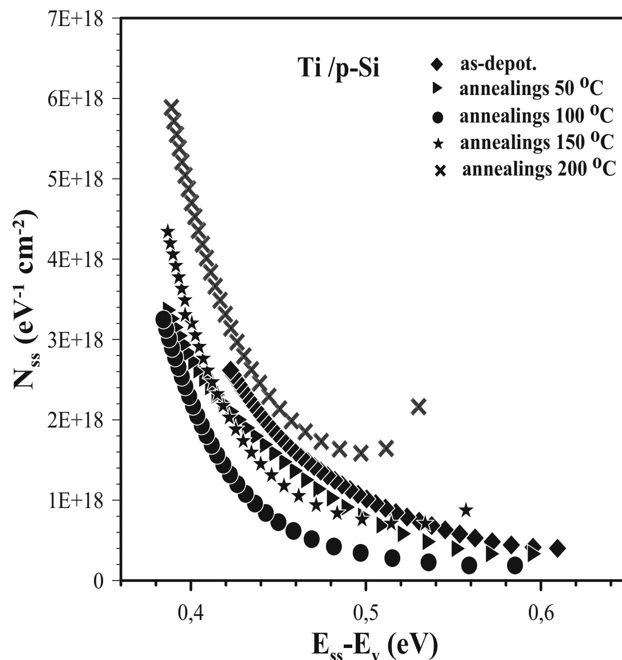

Fig. 8 The interface state energy distribution curves of the Ti/*p*-Si Schottky diode as a function annealing temperature

inhomogeneities and the effect of the image force or an interface layer in the Schottky barrier height at MS interface [3, 29, 36, 47, 48].

4 Conclusions

The electrical properties of Ti/*p*-type Si SBDs were investigated using *I*–*V* and *C*–*V* characteristics as a function of annealing temperature. The values of n and Φ_b and R_s changed with increasing the annealing temperature. The measurement results showed that the ideality factor of the unannealed and annealed at 200 °C diodes is 1.3 (*I*–*V*)/3.55 [$dV/d(\ln I)$–I] and 2.25 (*I*–*V*)/3.63 [$dV/d(\ln I)$–I], respectively. From the measurements, barrier height in unannealed and annealed diodes was calculated to be 1.038 eV(*C*–*V*)/0.747 eV(*I*–*V*) and 1.60 eV (*C*–*V*)/0.560 eV (*I*–*V*), respectively. Barrier height values were calculated with 4 methods (C^{-2}–V characteristics, *I*–*V* method, Cheung's function and Norde function) and the values found can be compared with each other. Further, the energy distribution of interface state density is determined from the forward bias *I*–*V* measurements and the calculated interface state density of the Ti/*p*-Si SBD decreases for the contact annealed at 150 °C and then increases after annealing at 200 °C. R_s values calculated from H(*I*)–*I* and $dV/d(\ln I)$–I plots were found to be close to each other. It was observed that the values of n before decreased and then increase with increasing the annealing temperature.

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