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Effect of atomic-layer-deposited HfO_2 thin-film interfacial layer on the electrical properties of Au/Ti/n-GaAs Schottky diode

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ABSTRACT

The electrical properties of Au/Ti/HfO_2/*n*-GaAs metal/insulating layer/semiconductor (MIS) contact structures were analyzed in detail by the help of capacitance–voltage (*C*–*V*) and conductance–voltage (*G*–*V*) measurements in the temperature range of 60–320 K. The HfO_2 thin-film layer was obtained by atomic layer deposition technique (ALD). The main electrical parameters such as ideality factor (*n*) and barrier height (Φ_{B0}) were determined for Au/Ti/*n*-GaAs and Au/Ti/HfO_2/*n*-GaAs diodes using current–voltage (*I*–*V*) measurement at 300 K. The values of these parameters are 1.07 and 0.77 eV for the reference (Au/Ti/*n*-GaAs) diode and 1.30 and 0.94 eV for the Au/Ti/HfO_2/*n*-GaAs MIS diode, respectively. An interfacial charge density value of Q_{ss}= 4.14×10^{12} Ccm^{-2} for the MIS diode was calculated from the barrier height difference of $\Delta\Phi = 0.94 - 0.77 = 0.17$V. Depending on these results, the temperature-dependent *C*–*V* and *G*–*V* plots of the device were also investigated. The series resistance (R_s), phase angle, the interface state density (D_{it}), the real impedance (Z′) and imaginary impedance (Z″) were evaluated using admittance measurements. The *C* and *G* values increased, whereas (Z″) and *Z* decreased with increasing voltage at each temperature. An intersection point being independent of temperature in the *G*–*V* curves appeared at forward-bias side ($\approx$1.4 V); after this intersection point of the *G*–*V* plot, the *G* values decreased with increasing temperature at a given voltage. The intersection points in total *Z* versus V curves appeared at forward-bias side ($\approx$1.7 V). The Nyquist spectra were recorded for the MIS structure showing single semicircular arcs with different diameters depending on temperature.

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1 Introduction

Thin-film technology has been widely used in the production of electronic devices from past to present and characterization of variety of them derived from traditional metal–semiconductor (MS) junction with Schottky barrier formation between metal and semiconductor [1, 2]. Schottky contacts based on group III–V semiconductors have been appeared especially in high-speed optoelectronic and electronic structures such as solar cells, field-effect transistors, high-electron mobility transistors and diodes [3–7]. Schottky diodes (SDs) are the simplest MS contact devices [8–13] the understanding of which has great technological importance in the electronics. At this point, since gallium arsenide (GaAs) is one of the most important materials for low-power and high-speed devices, a full understanding of the nature of the electrical characteristics of GaAs-based SDs is essential for its application. In general, in the literature, we find that mainly two parameters of a Schottky diode, ideality factor (n) and barrier height (BH), were evaluated and their dependence on temperature and voltage was discussed [14–18]. Biber et al. [12], Kahveci et al. [11] and Karabulut [13] have obtained an approximate value of zero-bias barrier height (Φ_{B0}) as around 0.76 eV at 300 K for Au/Ti/n-GaAs MS diode.

Recently, MS diodes have stayed popular in determining the electrical properties of interfacial thin-film layers produced by different methods [19, 20]. In fact, the performance of metal–insulator–semiconductor (MIS) diodes depends on formation of an insulator layer, active metal/semiconductor interface, the interface states distribution at semiconductor, insulator interface, series resistance and inhomogeneous barrier heights [21–28]. Therefore, the production of thin-film surfaces with different methods has gained importance for MIS diodes in recent years. In the literature, MIS diodes were formed by adding an interfacial layer to the MS contact interface by different deposition methods such as metal–organic chemical vapor deposition (MOCVD), sputtering, molecular beam epitaxy (MBE) and atomic layer deposition (ALD) technique [29–32]. Electrical behavior and capacitive characteristics of MS diode change with the presence of the interfacial thin-film layer.

Self-generated oxide layer or layer intentionally formed on semiconductor sample takes effect BH formation between metal and semiconductor. Reliability and performance of MIS diodes depend on this barrier formation and its effects on ideality of the diode behavior such as inhomogeneous barrier heights together with parasitic resistances and interface states distribution at an interfacial thin layer and semiconductor interface [31, 32]. The SiO_2 thin layer is generally used as the interfacial layer at the MS contact interface by different methods. Many studies have shown that the SiO_2 interface layer causes high leakage current. That is why the researchers started working on different interface layers to reduce leakage current of MIS diodes [33–35]. Due to the high leakage current problem of SiO_2 layer, high-dielectric materials have been a point of interest in Schottky-type and MIS diodes.

At this point, the high-dielectric materials such as HfO_2, ZrO_2 and TiO_2 attracted great interest in which the leakage current of metal/HfO_2/, metal/TiO_2/ and metal/Si_3N_4/ contacts on the semiconductor substrate is lower than the leakage current of metal/SiO_2/semiconductor diode, and high-dielectric layers dropping influence in leakage current of devices increased rectification rate (RR = I_F/I_R) or shunt resistance [36–45]. Recently, hafnium oxide (HfO_2) thin films have been received much attention because it can suppress the leakage current in insulating gate materials [46–51]. This film also shows high resistivity and dielectric constant at diode interface [46–49]. In addition, HfO_2 insulator layer has positive fixed charges; therefore, it is good suitable for n-Si sample. There is currently limited research focusing on the passivation of HfO_2 on n-Si sample for Si-based solar cells [52–54].

Active dangling bonds at Si semiconductor surface had still problems on passivation processes [32, 34]. Therefore, new materials alternative to SiO_2 and different deposition methods have been also point of interest. The quality of HfO_2 thin films depends on deposition method. In the literature, several deposition techniques have been used to grow this insulator layer on semiconductor. Among many possible deposition techniques for preparing ultrathin metal oxide films, ALD is very promising one because it can produce high-quality films with precise thickness control and near-perfect conformality owing to its adsorption-controlled deposition mechanism [32, 55–59]. One of the biggest advantages of ALD technique is ability to obtain highly reproducible, homogenous coatings, while deposition process does

not depend on source of substrates [60, 61]. Ritala et al. reported that HfO_2 gate dielectric is compatible with conventional poly-Si without needing a barrier layer [62].

MS and MIS diodes are crucial to indicate the electrical properties in wide range frequency and temperature to detail the interface homogeneity and nature transport mechanism [32–34]. The basic electrical properties of these diodes are extracted according to thermionic emission (TE) theory. Applying this theory, n and BH can be determined. There are some literature works on HfO_2/Si or HfO_2/GaAs diodes [13, 63–66]. Gullu et al. fabricated the In/HfO_2/Si diode, and Φ_{B0} and n for this type of diode were determined 0.79 eV and 4.22 at room temperature, respectively [63]. In addition, Turut et al. fabricated the diode with HfO_2 thin interlayer, and the values of these parameters for this diode were determined 0.91 eV and 1.11 at 280 K, respectively [67]. In this work, the electrical properties of the Al/Ti/HfO_2/GaAs Schottky diodes were analyzed by the admittance measurements in the temperature range of 60–320 K. The HfO_2 film layer of 10 nm was deposited on n-GaAs semiconducting sample by ALD method, and the Schottky contact (Au/Ti) was obtained using thermal evaporation method. The basic electrical parameters as Φ_{B0} and n were determined from TE theory implemented to the I–V measurements (300 K) of the Al/Ti/HfO_2/GaAs and Al/Ti/GaAs Schottky diodes. In addition, the diode parameters such as the phase angle, the capacitance C, conductance G, series resistance R_s, density of interface states D_{it}, real impedance Z' and imaginary impedance Z'' of Al/Ti/HfO_2/GaAs diode were investigated using admittance–voltage measurements with the change in temperature (60–320 K).

It has been investigated the effect of atomic-layer-deposited HfO_2 thin-film interfacial layer on the electrical properties of Au/Ti/n-GaAs Schottky diode. The HfO_2 thin-film layer at MS interface causes the barrier modification and semiconductor surface passivation. The barrier modification is an important process in the rectifying MS contacts. The MS Schottky contacts (SCs) play an important role in integrated device fabrication. The purpose of the BH modification can be both to increase the BH and to improve the rectification properties in MS SCs. The reduced BH decreases the voltage drop in forward bias while maintaining the rectification properties in reverse bias. Some authors [1, 2, 11–13, 66–68] reported that the low-barrier diodes allow as small signal zero-biased MS SCs and microwave mixers. In the microwave MS SC applications, the larger-barrier SCs must be used with a dc offset voltage. Furthermore, the increased barrier structures can be used for the gates of MESFETs, and the small-barrier SCs normally cause very large gate leakage currents. Moreover, the increased barrier devices and diodes are also useful in surface recombination studies and optical detectors such as solar cells and photodiodes. Moreover, the SCs and bipolar p–n junctions with high BH can be used in determination of minority-carrier lifetimes and carrier diffusion constants. The semiconductor surface passivation or the use of the HfO_2 thin film before Schottky metallization offers a number of potential advantages such as improvement in the impedance characteristics of the device or to protect the semiconductor surface from defective interfacial compounds. The surface passivation by the HfO_2 thin film can be designed to control the defective states originated from the deposition of Schottky metal and interfacial reaction during metallization. That is, the MIS diodes may be a sensitive probe useful to increase the quality of devices fabricated using the interfacial thin layer in establishing processes for minimizing surface states, surface damage and contamination, and actively tunable barrier heights [1, 2, 11–13, 66–68].

2 Experimental Procedure

The Au/Ti/HfO_2/n-GaAs MIS structure was fabricated by the process order of indium (In) back contact evaporation on the n-GaAs sample (2 Ω.cm resistivity and 7.43×10^{15} cm^{-3} carrier concentration), HfO_2 thin-film deposition on the n-GaAs sample. For the front contacts, the n-GaAs wafer was placed on a rotating table to get homogeneity. Ti (10 nm) Schottky contacts were made using the magnetron DC sputter system, and Au (90 nm) was evaporated as a top layer on the Ti/HfO_2/n-GaAs structure to protect the Ti metallic layer in high-vacuum system of about 10^{-6} Torr. [13, 67–69]. Before the deposition process, n-GaAs sample was chemically cleaned. For the ohmic contact, one side of the GaAs sample was deposited by elemental In evaporation process and post-annealing treatment was applied at 385 °C. The

contact resistivity of the In/n-GaAs structure was determined as 2.5×10^{-4} Ω cm [66, 70–72]. Then, 10-nm HfO_2 layer was deposited using a Savannah S300 ALD system [73–75].

The surface topography and roughness characterization for the deposited HfO_2 film and *n*-GaAs sample surface were performed using PARK system XE 100E atomic force microscopy (AFM). In Fig. 1a and b, the topography of the *n*-GaAs sample is presented as 3D and 2D AFM images, respectively. These images indicate the presence of smooth surface profile with root-mean-square (RMS) surface roughness value as 895 pm. Similarly, in Fig. 2a and b, topography of the HfO_2 layer is presented as 3D and 2D AFM images, respectively. As a result, 10-nm HfO_2 film was found in a uniform and homogenous surface profile where its RMS surface roughness value was observed as 1.19 nm. Finally, Au (90 nm)/Ti (10 nm) Schottky contacts were formed on HfO_2/*n*-GaAs structure by the DC sputtering method [13, 66, 67]. Au/Ti contact was preferred to obtain low-barrier formation, since work function of Au/Ti is smaller than Au. At this point, there are some works to analyze barrier height of Ti and Au/Ti Schottky contacts on n-InAlAs and these values were reported as 0.64 and 0.55 eV, respectively [76, 77]. In the current MIS structure, the Au thin film was used as a top layer to protect the Ti metallic layer on the GaAs substrate. In other words, Au was selected as the second layer to prevent oxidation and to promote current spreading, and to provide good smoothness to the contact [67, 75]. It is a common technique that Au over layer is deposited on top to enhance conductivity and prevents resistance problems [78].

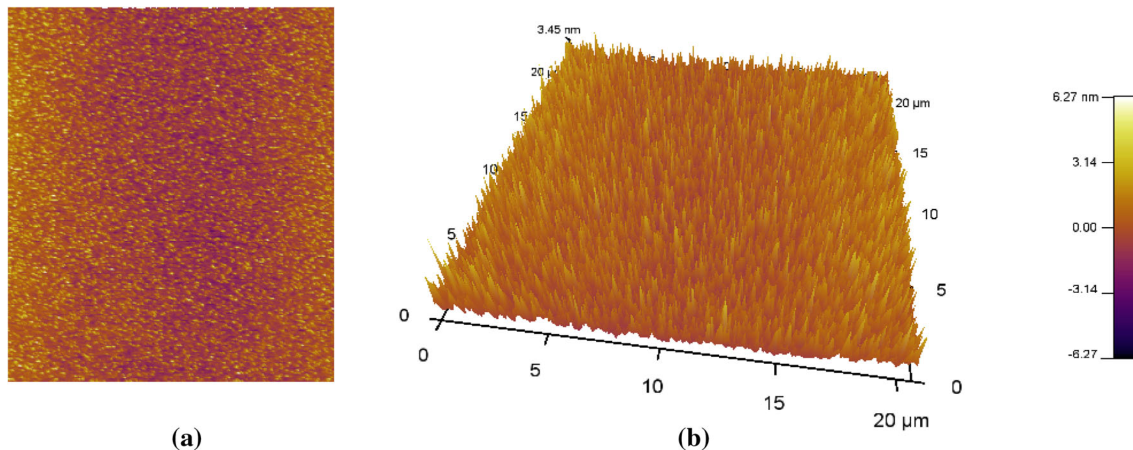

Fig. 1 (color online) **a** 2D and **b** 3D for the surface morphology of *n*-type GaAs substrate; the RMS value is 895 pM

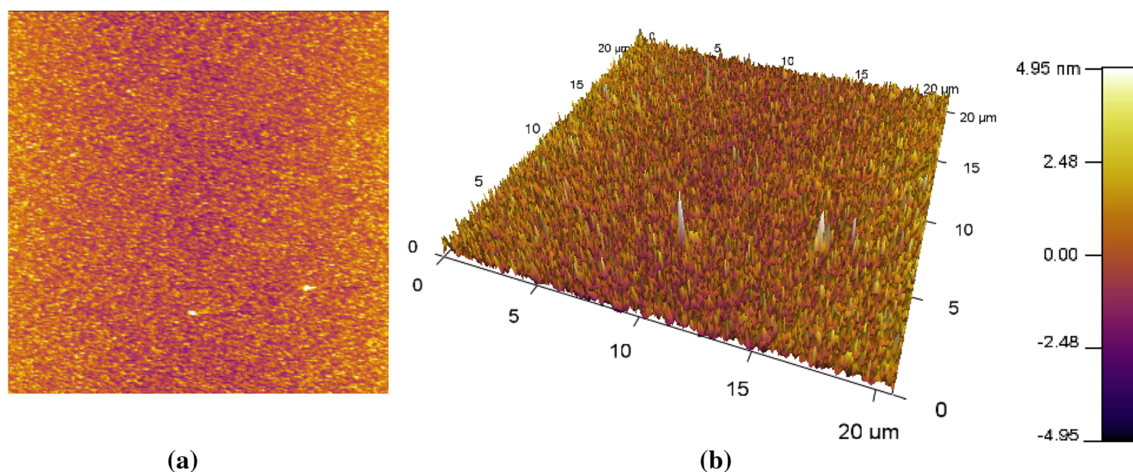

Fig. 2 (color online) **a** 2D and **b** 3D for the surface morphology of deposited 10-nm HfO_2 on *n*-type GaAs substrate; the RMS value is 1.19 nm

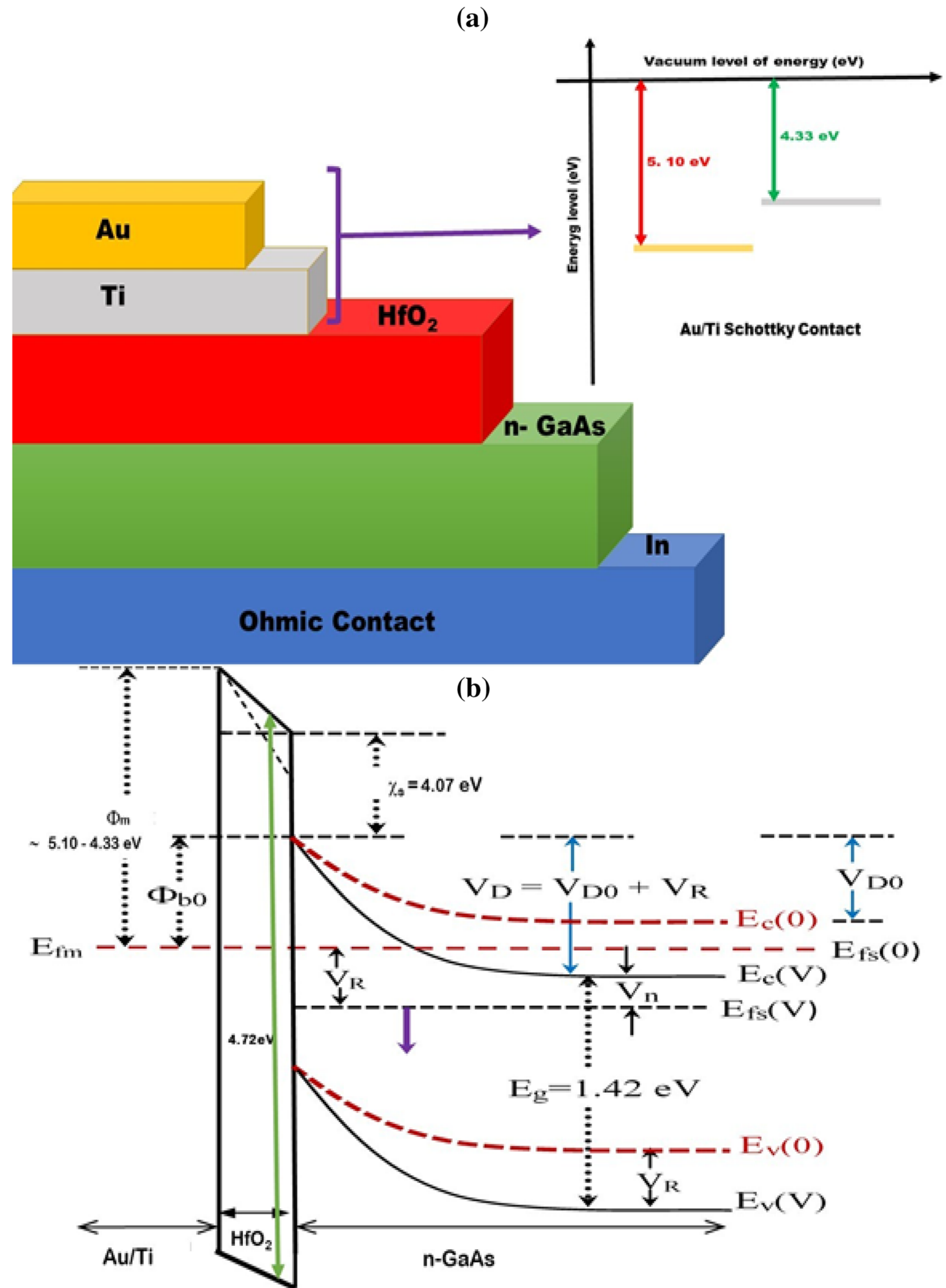

Fig. 3 (color online) **a** Schematic model of the Au/Ti/HfO_2/*n*-GaAs structure. **b** Energy-band diagram for a metal/insulating layer/*n*-semiconductor MIS structure at zero bias and under applied reverse-bias condition

Therefore, Au/Ti layer was preferred instead of one type metal contact such as Au or Ti.

The energy band diagram and schematic design structure for the Au/Ti/HfO_2/*n*-GaAs diodes are shown in Fig. 3a and b, respectively. In addition, the energy level of Au/Ti metal Schottky contact is shown in Fig. 3a, b shows energy-band diagram for Au/Ti/HfO_2/n-GaAs diode at under applied and zero-bias condition, where E_{fm} is the Fermi energy level, $_{M}$ is the work function of metal, V_n is the potential difference between Fermi energy level (E_{fs}) and the conduction band bottom (E_c), $_{bo} = V_{Do} + V_n$ is the effective barrier height at the zero bias, V_{Do} is the value at the zero bias of the surface potential, V_D is the value under the applied reverse bias of the surface potential and V_R is the voltage drop across the depletion region in the reverse-bias case. As shown in Fig. 3b, the electron affinity (χ_s) of n-GaAs is ∼ 4.07 eV, the thickness (δ) of the HfO_2 is 10 nm and the energy band gap of n-GaAs is ∼ 1.42 eV.

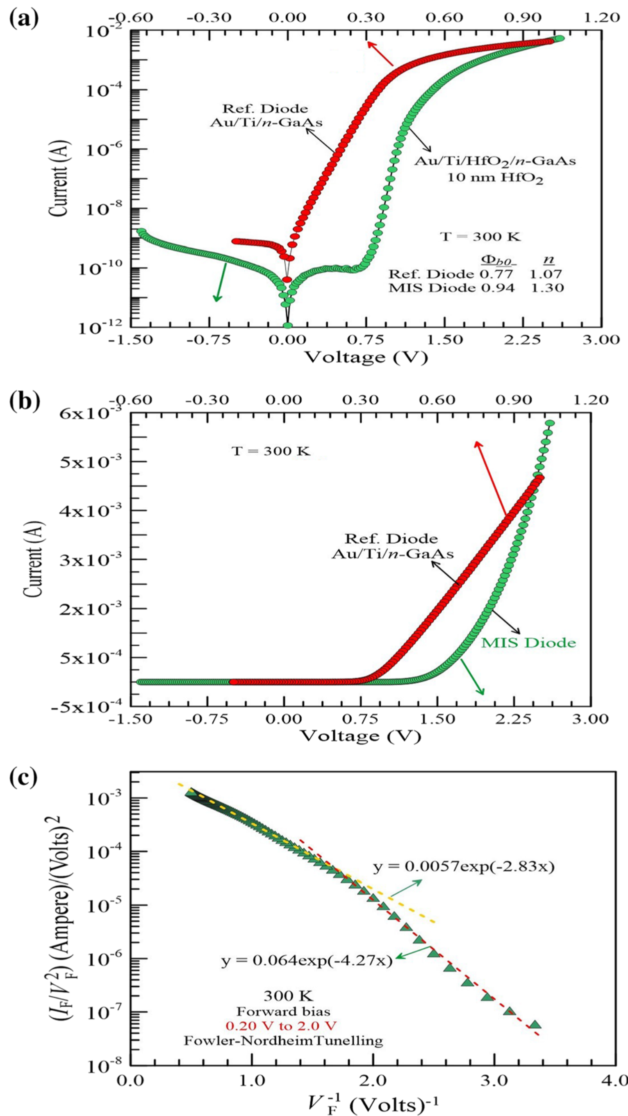

Fig. 4 (color online) **a** The semi logarithmic I–V; **b** the linear I–V plots of Au/Ti/n-GaAs and Au/Ti/HfO2/n-GaAs diodes at 300 K; **c** Fowler–Nordheim tunneling plot for Au/Ti/HfO_2/*n*-GaAs diode at 300 K

After the fabrication process, the current values were collected by a Keithley 487 Picoammeter voltage source. For the temperature-dependent measurements between 60 and 320 K, a Leybold–Heraeus closed-cycle helium cryostat was used and the temperature on the Au/Ti/HfO_2/*n*-GaAs MIS diode was adjusted using a Lake-Shore DCR-91C controller. In addition, the admittance measurements were carried out by a HP model 4192A LF impedance analyzer under dark conditions.

3 Results and discussion

As an initial step to determine basic electrical properties from *I–V* plots for a diode with and without interfacial layer (MIS diode), thermionic emission (TE) equation was used. For this type of diodes, it can be expressed as [13, 28, 34, 79]

$$I = I_s\left[\exp\left(-\frac{q(V)}{nkT}\right) - 1\right] \tag{1}$$

where I_s is the saturation current and it is defined as

$$I_s = SA^*T^2\exp\left(-\frac{q\Phi_{b0}}{kT}\right) \tag{2}$$

where $q\Phi_{B0}$ is the measured zero-bias barrier height from Eq. (2), which can be expressed as

$$q\Phi_{b0} = kT\ln\left(\frac{A^*ST^2}{I_s}\right) \tag{3}$$

where T is the absolute temperature, S is the Schottky diode area and A^* is the effective Richardson constant and it is 8.16 $Acm^{-2}K^{-2}$ for *n*-type GaAs. The equation of n can be written from Eq. (1) for $(V < 3kT/q)$

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \tag{4}$$

From Fig. 4 (a), Φ_{B0} and n values of the reference and MIS diodes were calculated as 0.77 eV and 1.07 and 0.94 eV and 1.30 using the intercept and slope of the linear part of the *I–V* curves at 300 K using Eqs. (3) and (4), respectively. Therefore, these results indicate that the MIS structure with HfO_2 film can be used for the barrier height modification. This interfacial film is a gate insulator for capacitor applications [79, 80]. The HfO_2 gate has a considerably high-barrier height for holes and electrons in the semiconductor, which can require relatively large band offsets at interfaces of MIS diode [81, 82]. Figure 4b shows the linear *I–V* plot of diode with and without interfacial HfO_2 thin film. As presented in this figure, the rectification ratio, turn-on voltage and leakage current values of Au/Ti/n-GaAs diode were determined as 1×10^6 ($RR = V_F/V_R$, at $V_R = -0.5$ V and $V_F = 0.5$ V), ∼ 0.3 V and 8.8×10^{-10} A at − 0.5 V, respectively. On the other hand, these values were found as 3×10^6 (at $V_R = -1.0$ V and $V_F = 1.0$ V), ∼ 0.68 V and 1.3×10^{-10} at − 1.0 V for Au/Ti/HfO_2/n-GaAs diode, respectively. Currently, the leakage current of Au/Ti/HfO_2/n-GaAs diode

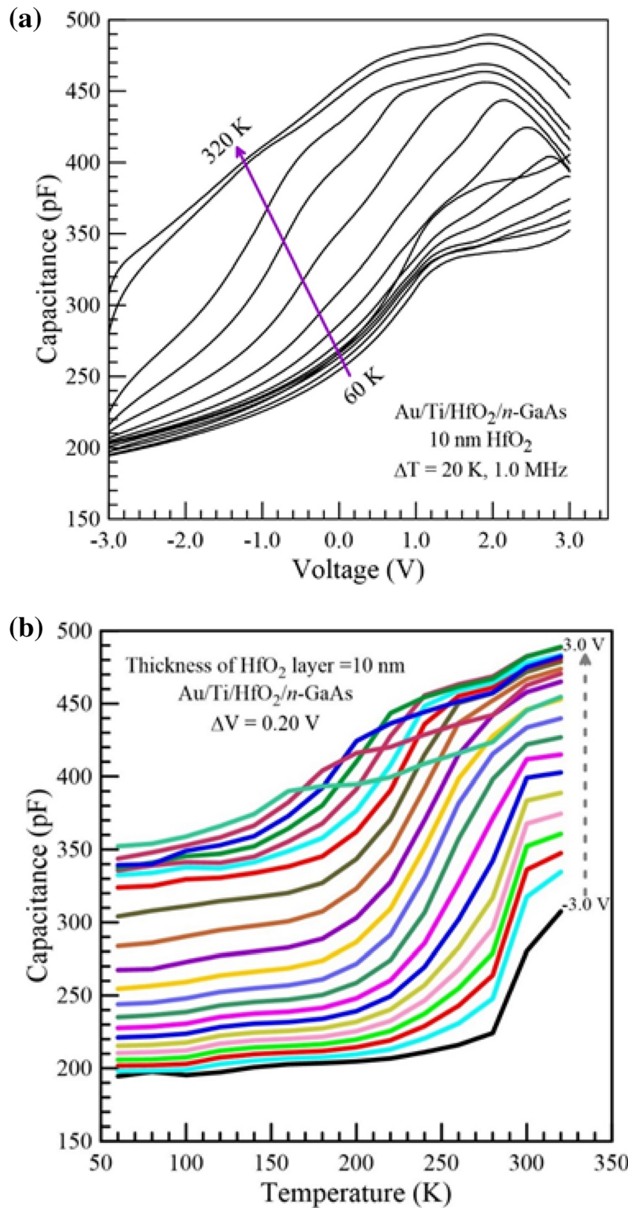

Fig. 5 (color online) **a** The temperature-dependent C–V plots of the Au/Ti/HfO_2/*n*-GaAs diode. **b** The voltage-dependent C–T plots of the Au/Ti/HfO_2/*n*-GaAs diode at 1000 kHz frequency

was 3.5×10^{-11} A at $-$ 0.5 V. Depending on these results, 10-nm HfO_2 increases RR and turn-on voltage of Au/Ti/n-GaAs diode while leakage current decreases. Similar results were shown in the literature [13, 66, 67].

As shown in Fig. 4, the Φ_{B0} value of the reference diode is lower than the value of Au/Ti/HfO_2/n-GaAs diodes. Kahveci et al. [11], Biber et al. [12] and Karabulut [13] have obtained an approximate Φ_{B0} value of 0.76 eV at 300 K for Au/Ti/n-GaAs MS diode. In addition, Biber et al. reported that n of Au/Ti/n-GaAs MS diode is 1.074 at 300 K [12]. The barrier height value in the literature ($\sim$ 0.76) is very close to the value ($\sim$ 0.77) that was found for the reference diode in this work. The higher than unity value of n is the indication of lateral inhomogeneity in the MIS diode [32, 45]. At room temperature, Au/Ti/HfO_2/n-GaAs MIS diode gives higher Φ_{B0} values than Au/Ti/n-GaAs MS diode. Thus, it is an obvious fact that HfO_2 interfacial layer causes the modification and increase in the Φ_{B0} that can be related to the free carriers having enough energy to pass over the barriers [32, 79]. In addition, the experimental result where the Φ_{B0} value of Au/Ti/HfO_2/n-GaAs diodes is higher than the value of the reference diode may be evaluated by the presence of the HfO_2 oxide layer and interface state charge Q_{ss} at the thin oxide layer/

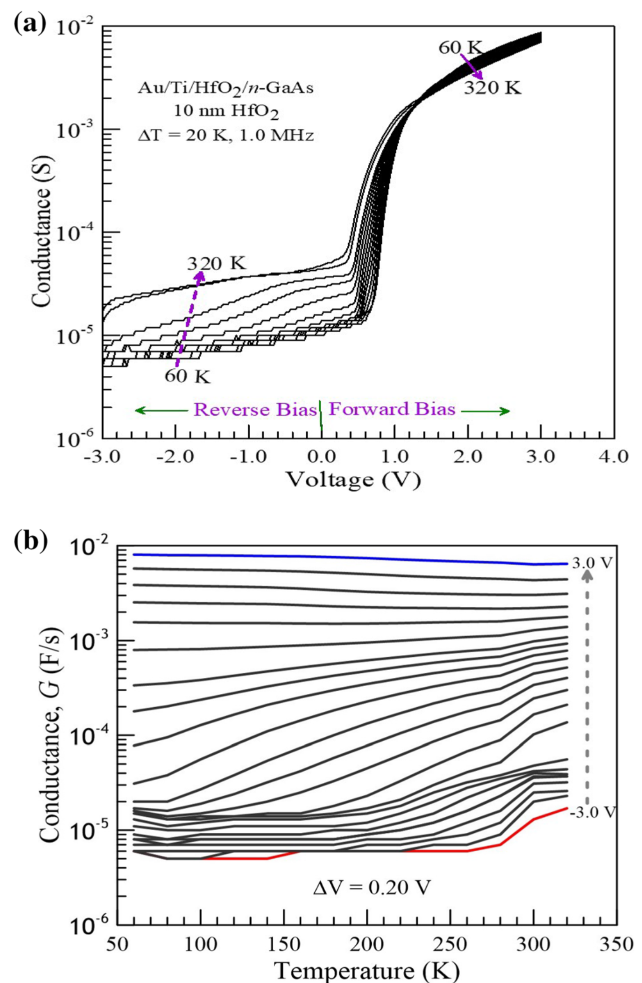

Fig. 6 (color online) **a** The temperature-dependent G–V plots of the Au/Ti/HfO_2/*n*-GaAs diode. **b** The voltage-dependent G–T plots of the Au/Ti/HfO_2/*n*-GaAs diode at 1000 kHz frequency

n-GaAs semiconductor interface. The negatively charged acceptor-type interface state charge Q_{ss} also increases the positive space charge in the depletion region or the presence of a net negative Q_{ss} may be caused increase in the barrier height [79–86]. The negative Q_{ss} charge is defined as [82–84]:

$$\Delta\Phi = \frac{Q_{ss}\delta}{2\varepsilon_i} \quad (5)$$

where ε_i is the dielectric constant of HfO_2 layer (22 ε_0), δ thickness of HfO_2 (10 nm) and the increase in the barrier height $\Delta\Phi = 0.94 - 0.77 = 0.17$V. Thus, an interface charge density value of Q_{ss}= 4.14 × 10^{12} Ccm^{-2} is obtained from Eq. (5).

The increase in the ideality factor much larger than one for MIS diode shows that the transport properties of the device cannot be well described by only TE model. Therefore, the barrier height and ideality factor are merely a curve fitting parameters for these samples and should not be interpreted as representing the true barrier height and current mechanism. That is, the determination processes of the diode parameters by means of eqns. (3) and (4) are to learn about whether the current mechanism through the device fits the standard TE theory [87]. Figure 4c shows the Fowler–Nordheim (FN) tunneling model plotted for Au/Ti/HfO_2/n-GaAs/In MIS diode from the I–V characteristics given in Fig. 4a. The FN equation can be applied to the tunneling mechanism

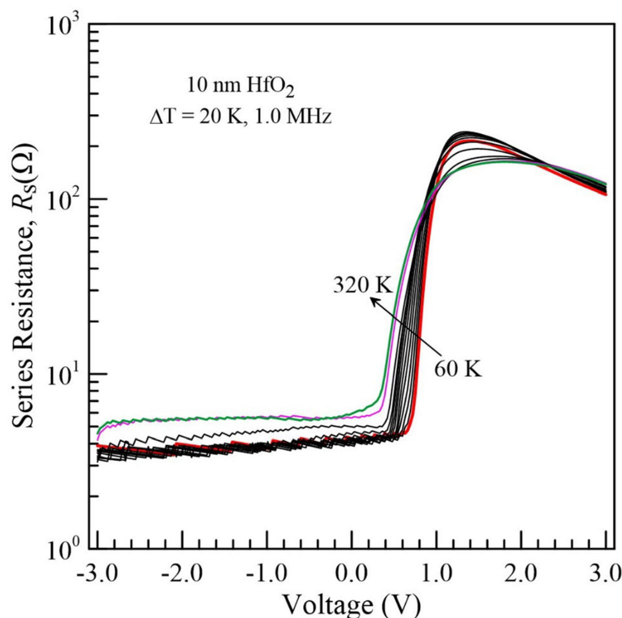

Fig. 7 (color online) The temperature-dependent R_s–V plots of the Au/Ti/HfO_2/n-GaAs diode

of carriers through thin oxide layers (i.e., tunneling through triangular barrier). The FN expression for the carriers is given as [88–90]

$$I_{FN} = \frac{Aq^2V^2}{8\pi hd^2\Phi_B}\left[\exp\left(\frac{8\pi d\sqrt{2m}\Phi_B^{3/2}}{3qhV}\right)\right] \quad (6)$$

$$B = \frac{Aq^2}{8\pi hd^2\Phi_B}$$

$$C = \frac{8\pi d\sqrt{2m_e}\Phi_B^{3/2}}{3qh}$$

$$\frac{I_{FN}}{V^2} = B\exp\left(-\frac{C}{V}\right)$$

The $\ln\left(\frac{I_F}{V_F^2}\right) vs V_F^{-1}$ plot in Fig. 4b consists of two linear regions. The linear behavior of the plot indicates that the FN tunneling current dominates through the interfacial thin-layer HfO_2. The straight lines in the low- and high-bias voltage regions in this figure are found in the exponential functions as $y = 0.064exp(-4.27x)$ and $y = 0.0057exp(-2.83x)$, respectively.

Figure 5a and b shows the temperature-dependent capacitance–voltage (C–V) and voltage-dependent capacitance–temperature (C–T) measurements for the Au/Ti/HfO_2/n-GaAs diodes at 1000 kHz, respectively. As shown in Fig. 5a, the values of capacitance increase with increasing temperature in the temperature range of 60–320 K. The values of capacitance give a peak in the temperature range of 160–320, shifting to forward-bias region with decreasing temperature. It is shown in Fig. 5a that the C values of Au/Ti/HfO_2/n-GaAs diode increase rapidly in the interval of − 3 and 3 V. In addition, the capacitance values decrease with decreasing voltage in the voltage range of − 3 –2.4 V at each temperature, whereas there is a slow increase in behavior between 150 and 320 K. The observed non-ideality behaviors in the admittance spectra can be due to inhomogeneities in the interfacial layer and barrier height in the diode. The interfacial passivation layer thickness, frequency and temperature can influence the G–V and C–V behavior of these diodes [91–99]. The C–V plot of these structures is influenced by various non-idealities such as the interfacial insulator layer, series resistance and interface states [1, 2, 99, 100]. Figure 6b shows the G–V plots of the Au/Ti/HfO_2/n-GaAs MIS structure. As shown in Fig. 6a, the G values of Au/Ti/HfO_2/n-GaAs MIS structure increase rapidly

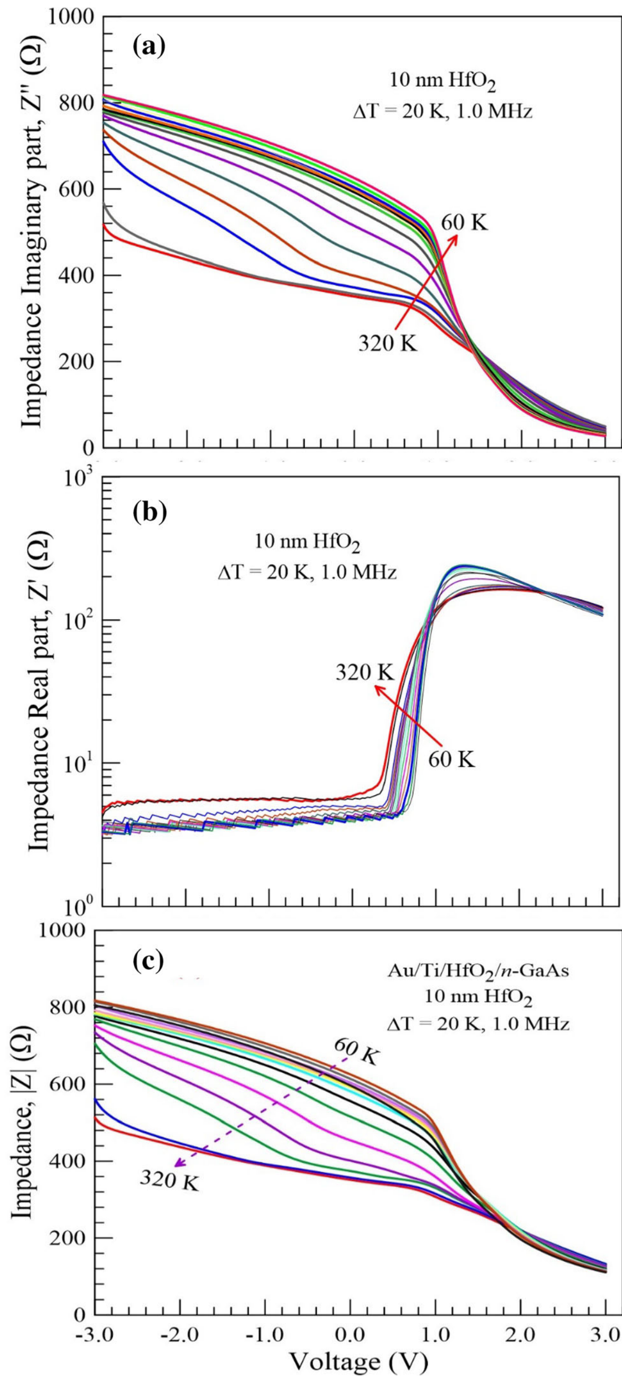

Fig. 8 (color online) The temperature-dependent (a) $Z'-V$ (b) $Z''-V$, (c) Z−V plots of the Au/Ti/HfO_2/*n*-GaAs diode

in the interval of 0.6 and 1.4 V, whereas there is a slow increase in behavior between − 3 and 0.6 V. Turut et al. reported similar *G–V* characteristics for the Au/Ti/Al_2O_3/n-GaAs structure at 300 K [86]. It was observed that unlike ideal Schottky diodes, *G–V* plots intersect at ∼ 1.4 V. This behavior appears in

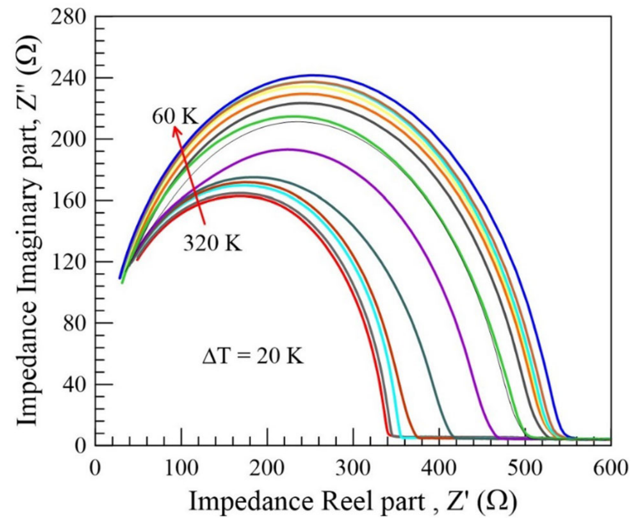

Fig. 9 The $Z''-Z'$ plots of the Au/Ti/HfO_2/*n*-GaAs diode

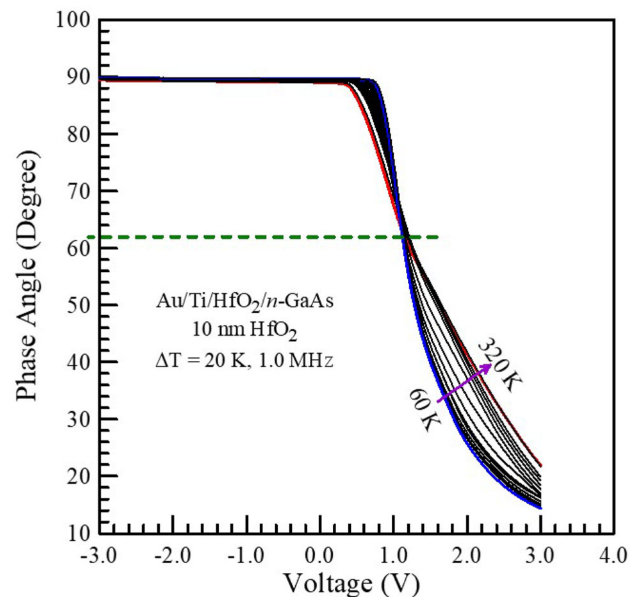

Fig. 10 (color online) The phase angle versus voltage plots of the Au/Ti/HfO_2/*n*-GaAs diode at 1000 kHz frequency

the case of inhomogeneous Schottky diodes, and the presence of series resistance (R_s) keeps this intersection unobservable and hidden in homogeneous Schottky diodes [66, 83]. Then, this crossing of the *G–V*, the *G* values of Au/Ti/HfO_2/n-GaAs diodes decrease with increasing temperature in the temperature range of 60–320 K. As shown in Fig. 6b, the conductance value increases with increasing voltage for each temperature.

The R_s profile was determined in the strong accumulation region from the $C-V$ and $G-V$ measurements [49, 101, 102],

$$R_s = \frac{G_m}{(G_m)^2 + (\omega C_m)^2} \tag{7}$$

and the corresponding values are calculated according to Eq. (7) and demonstrated in Fig. 7 for each temperature at 1000 kHz. As shown in this figure, in the voltage range of − 3.0–0.4 V, the R_s is the constant for each temperature and the R_s value of the Au/Ti/HfO_2/*n*-GaAs MIS diode increases rapidly in the interval of 0.4 and 0.95 V. In the voltage range of 0.95–2.2 V, the R_s gives a peak depending on temperature. The two crossings of the R_s–V curves appear at forward bias (≈0.95 V and 2.2 V), and this observation can be concluded as being a non-ideal Schottky diode behavior [66, 83].

The total impedance (Z) can be expressed as [12, 103]

$$Z = \frac{1}{Y} = Z_{\mathrm{Re}} + jZ_{\mathrm{Im}} = \frac{1}{G_m + j\omega C_m} \tag{8}$$

where Z_{Im} and Z_{Re} are the imaginary and real part of the total impedance Z, respectively. Then, Eqn. (8) can be decomposed by

$$Z = \frac{G_m}{(G_m)^2 + (\omega C_m)^2} - \frac{j\omega C_m}{(G_m)^2 + (\omega C_m)^2} \tag{9}$$

As shown in Eqs. (8) and (9), Y is the admittance and G_m and C_m are the measured conductance and capacitance, respectively. The R_s is the reel part of impedance given in Eq. (7).

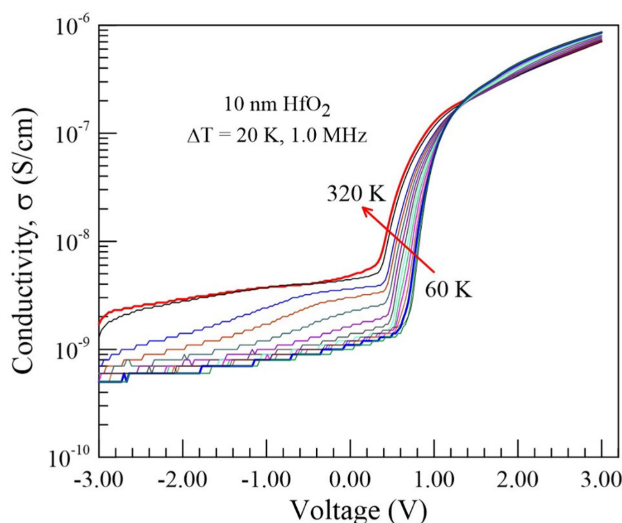

Fig. 11 (color online) The temperature-dependent $\sigma - V$ plots of the Au/Ti/HfO_2/*n*-GaAs diodes

Figure 8a exhibits the voltage-dependent plots of the imaginary impedance (Z″) of the Au/Ti/HfO_2/*n*-GaAs MIS structure in the temperature range of 60-320 K. As shown in Fig. 8a, the Z″ value of the MIS diode decreases with increasing voltage at each temperature and decreases with increasing temperature in the voltage range of − 3–0.4 V. A crossing of the Z'–V curves appears at forward bias (≈1.4 V). After this crossing of the Z'–V curves, the Z' value of diode increases with increasing temperature in the voltage range of 1.4–3 V. Figure 8b exhibits the voltage-dependent plots of the impedance real part of the Au/Ti/HfO_2/*n*-GaAs diode in the temperature range of 60-320 K. The real part of impedance corresponds to R_s. This figure also shows that the Z' value of the diode is constant in the voltage range of − 3.0–0.4 V for each temperature. In addition, the Z'–V curves have two crossings at forward bias (≈0.95 V and 2.2 V). As shown in Fig. 8b and Fig. 7, the Z'–V plots exhibit the same behavior as R_s–V plots. Figure 8c exhibits the total impedance of the MIS diode. It is obvious from Fig. 8b that the total impedance decreases with increasing voltage at each temperature and the crossing of the Z–V curves appears at forward bias (≈1.7 V). As shown in Fig. 8c, the total impedance value increases with increasing temperature in the voltage range of 1.7–3 V. Figure 9 exhibits the impedance imaginary part versus the real impedance part of the MIS diode in the temperature range of 60-320 K. The complex impedance Z consists of an imaginary part Z'' and a real part Z' which can be estimated from measured values of C and G [104, 105]. It is well-known fact that the $Z'-Z''$ plot is called a Nyquist diagram. This plot can provide further electrical information about the diode [106]. The Nyquist spectra recorded for the Au/Ti/HfO_2/*n*-GaAs diode at different temperatures show the single semicircular arcs with different diameters. These semicircles indicate the homogeneity of the HfO_2layer. The semicircle radius increases with decreasing the temperature. As shown in Fig. 9, the maximum points of the semicircular arcs are shifted toward the origin on increasing temperature [106–110].

Figure 10 exhibits the phase angle versus voltage plots for the Au/Ti/HfO_2/*n*-GaAs diode. As given in this figure, the phase angle is constant (same value) in

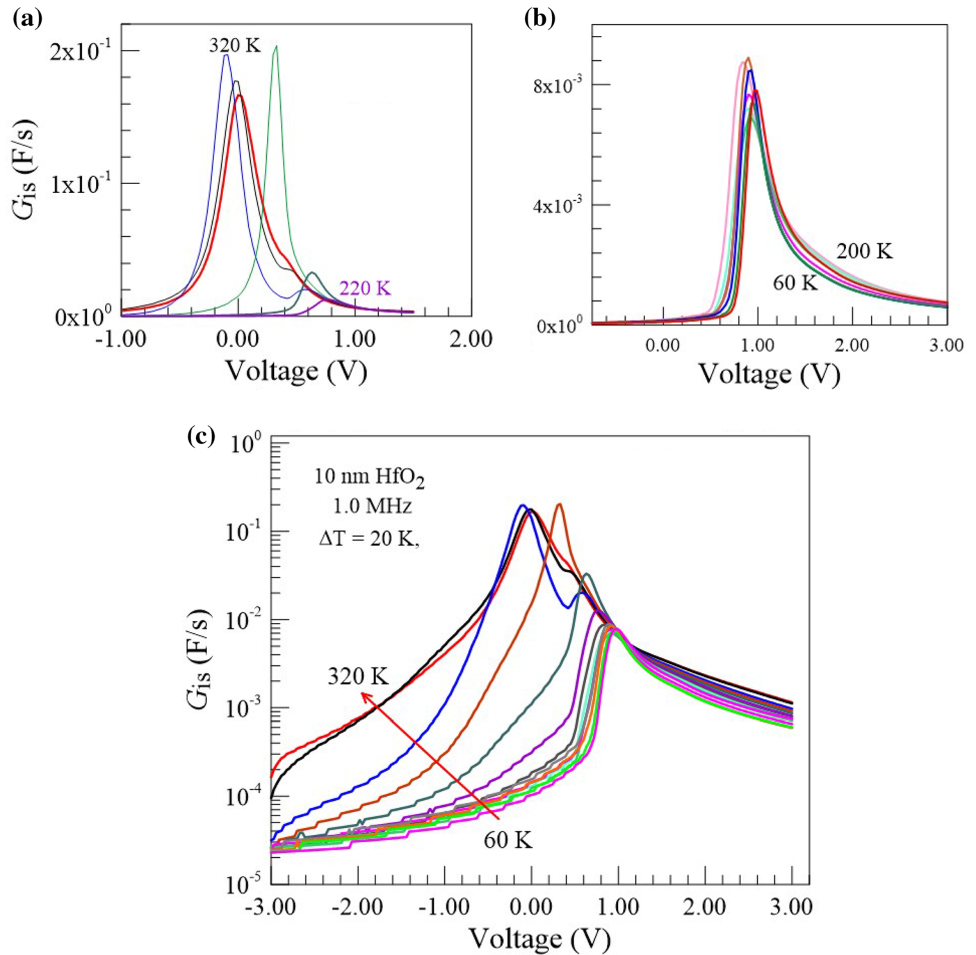

Fig. 12 The temperature-dependent G_{is}–V plots of the Au/Ti/HfO_2/n-GaAs diode at 1000 kHz frequency. **a** Lin–Lin plots in 60–200 K range, **b** Lin–Lin plots in 200–320 K range, **c** semi-log plots in 60–320 K range with steps of 20 K

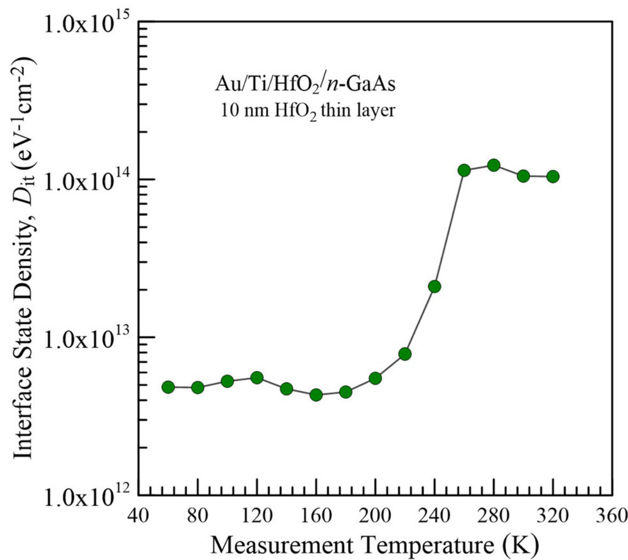

Fig. 13 (color online) Dependence distribution of the interface states on sample temperature for the Au/Ti/HfO_2/n-GaAs structure with about 10-nm HfO_2 layer thickness at 1000 kHz frequency

the voltage range of (−3)-0.6 V as temperature independent. Then, the phase angle increases with decreasing temperature in the voltage range of 0.6 V–1.2 V. In addition, an intersection point at phase angle curves is observed at about 1.20 V as independent of temperature. Turut et al. reported the phase angle for the Au/Ti/Al_2O_3/n-GaAs structure is always 90° from − 10 V to 0.0 V in the reverse-bias branch, and it suddenly decreases at 0.0 V and then approaches 0° from 0.0 V to 4.0 V in the forward branch [86]. This behavior is similar to the phase angle–voltage plot of the Au/Ti/HfO_2/n-GaAs diode. The case clearly indicates that the diode behaves more capacitively at the reverse-bias region rather than the forward-bias region [111].

Figure 11 exhibits the conductivity (σ) versus voltage of the Au/Ti/HfO_2/n-GaAs diode in the temperature range of 60-320 K. The σ of the Au/Ti/HfO_2/n-GaAs diodes increases with increasing temperature between − 3 and 1.4 V. In addition, the

crossing of the σ–V curves appears at forward bias (≈1.4 V).

The interface traps are defects located at the semiconductor–oxide layer interface. At frequency of AC voltage, the loss depends both on the interface trap level density near the Fermi level and on the speed of response of interface traps, determined by their capture probability. Thus, interface trap level density for energy levels and capture probability within the semiconductor band gap can be determined using the loss [80].

Figure 12 represents the experimental conductance of the interface states versus voltage plots for the Au/Ti/HfO_2/n-GaAs MIS structure with about 10-nm HfO_2 layer thickness at 1000 kHz frequency. (a) Lin–Lin plots in 60–200 K range, (b) Lin–Lin plots in 200–320 K range and (c) semi-log plots in 60–320 K range with steps of 20 K. The interface state conductance G_{is} for the G_{is} versus voltage curve ateach temperature was calculated from the following expression [111]

$$G_{is} = \frac{w^2 G_m C_{ox}^2}{G_m^2 + w^2 (C_{ox} - C_m)^2} \tag{10}$$

where C_{ox} is the interfacial layer capacitance and the G_m and C_m are the measurement experimental conductance and capacitance, respectively. Figure 13 displays the density distribution of the interface states on sample temperature for the Au/Ti/HfO_2/n-GaAs MIS diode. The interface state density value D_{it} at each temperature was calculated using the peak value in the interface state conductance versus voltage curve in $D_{it} = G_{max}/qwA$ expression. All interface states have the same time constant (relaxation time) because the measurements have made at 1.0 MHz; however, they have different energy positions in the semiconductor band gap at MS interface at each temperature. The interface state density value remains almost unchanged from 60 to 200 K, but it has an exponential rise with the temperature from about 200 K to 260 K, and it again remains almost unchanged from 260 to 320 K.

4 Conclusion

The main electrical parameters such as Φ_{Bo} and n for the Au/Ti/HfO_2/n-GaAs MIS structure fabricated by the ALD method and reference Au/Ti/n-GaAs diode were determined 0.94 eV and 1.30 and 0.77 eV and 1.07 from I–V curves at room temperature, respectively. As seen from results, the interfacial HfO_2 thin layer increased these values for the MIS structure and lowered leakage current. Finally, the C–V and G–V characteristics of Au/Ti/HfO_2/n-GaAs MIS structure were analyzed at 1000 kHz. The temperature- and voltage-dependent D_{it}, R_s, Z, Z', Z'' and phase angle of the MIS structure were examined in the temperature range of 60–320 K. It was observed that the G, C and R_s values displayed a behavior increasing with increasing temperature. The D_{it}, Z and Z' increased with decreasing temperature in the temperature range of 60–320 K.

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