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Solution-processed amorphous gallium oxide gate dielectric for low-voltage operation oxide thin film transistors

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ABSTRACT

Here, gallium oxide (Ga_2O_3) thin films were investigated as gate dielectric for thin-film transistors (TFTs) using the solution process method. The optical, microstructure, morphology, oxygen vacancy defect states and electrical performance metrics of Ga_2O_3 thin films annealed at different stages of temperature were explored. The excellent dielectric property of amorphous Ga_2O_3 thin films was found, but it was deteriorated after crystallization when the annealing temperature increased. The optimized Ga_2O_3 thin film exhibits a low leakage current density of 1.9×10^{-6} A cm^{-2} at 1.5 MV cm^{-2} and a large dielectric constant of 10.8. Furthermore, low-voltage operation oxide TFTs were demonstrated using this optimized amorphous Ga_2O_3 as gate dielectric. The device exhibits excellent bias stress stability with a high mobility of 8.5 cm^2/Vs, a threshold voltage of -1.4 V, a current on/off ratio of 10^4 and a subthreshold swing of 0.41 mV/Dec.

1 Introduction

Over the past decade, owing to their high transparency, high electron mobility and outstanding uniformity, metal oxide (MO) thin-film transistors (TFTs) have been extensively explored as electrical switch element in flat panel display, functional sensor arrays and other emerging electronic circuits [1–3]. Especially, many efforts have been made to develop high-k dielectric for the portable electronic devices, which is an effective way to enhance capacitive coupling and achieve low-operating voltage. Numerous candidate high-k materials, like ZrO_2, Y_2O_3, HfO_2, and Ga_2O_3 have been investigated [4–6]. Among them, Ga_2O_3 with the features of wide bandgap, large dielectric constant and excellent thermal stability leads to reduce direct-tunneling leakage current [7]. However, as far as we know, the literatures of Ga_2O_3 as gate dielectric for oxide TFTs are seldom reported. Although Chang et al. presented a-IGZO TFTs with Ga_2O_3 gate dielectric deposited by RF sputtering method, a SiO_2 interlayer

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is still required to reduce the leakage current and off-state current [8]. Moreover, it was reported that the Ga_2O_3 dielectric significantly reduce interfacial density states and lower leakage current for III-V semiconductor field-effect transistors [9].

Up to now, various growth techniques have been carried out to prepare Ga_2O_3 thin films, such as atomic layer deposition (ALD), chemical vapor deposition (CVD), molecular beam evaporation and solution process method [10, 11], among which solution process usually exhibits many advantages including simplicity, large-area uniformity, atmospheric processing, and low fabrication cost. As for the solution-processed metal oxide dielectrics, annealing conditions have great influence on chemical composition and physical properties. Although Xu et al. reported solution-processed Ga_2O_3 dielectric for low-voltage oxide TFTs, the relation of the electrical properties and the microstructure of Ga_2O_3 thin films need to be further investigated [12]. In this regard, solution-processed Ga_2O_3 thin films will be attractive and worthy of in-depth study for high-performance electronic devices. In this work, high-k Ga_2O_3 dielectric was fabricated by facile solution process method. The optical constant, phase composition, oxygen defects states, surface and dielectric properties of Ga_2O_3 thin films were systematically researched. Finally, solution-processed high performance In_2O_3 TFTs were integrated on the optimized amorphous Ga_2O_3 dielectrics.

2 Experimental details

2.1 Precursor preparation

All chemicals and solvents were purchased from Sigma-Aldrich. 0.2 M Ga_2O_3 precursor solution was prepared by dissolving $Ga(NO_3)3{\cdot}xH_2O$ in 2-methoxyethanol. 0.1 M In_2O_3 precursor solution was prepared by dissolving $In(NO_3)_3){\cdot}xH_2O$ in 2-methoxyethanol. Finally, the solutions were stirred overnight at room temperature.

2.2 Device fabrication

The TFTs were constructed on a heavily phosphor-doped n^+-Si substrate. Firstly, the substrate was ultrasonically cleaned and treated with an oxygen plasma. Then, Ga_2O_3 solutions were spin-coated on Si substrate at 3000 rpm for 30 s, followed immediately by annealing 20 min at 150 °C. Next, the films were post-annealed at 250, 350, 450 and 550 °C for 1 h after repeating the above operation four times. To investigate their dielectric properties, Metal-insulator-semiconductor (MIS) structure capacitors were fabricated by evaporate Al on the surface of Ga_2O_3 thin films. The area of Al electrode was 0.2 mm × 0.2 mm. For TFTs fabrication, the In_2O_3 precursor solution was spin-coated on the obtained Ga_2O_3 dielectrics and then annealed 20 min at 250 °C. Finally, Al was evaporated through a shadow mask to form source/drain electrodes with a channel length of 100 µm, and channel width of 1000 µm.

2.3 Thin film and device characterization

The film thickness and refractive indices were measured by a J.A. Woollam M2000U ellipsometer. Grazing incidence X-ray diffraction (GIXRD) were performed on a Rigaku ATXG diffractometer using Cu Kα (λ = 1.542 Å). X-ray photoelectron spectroscopy (XPS) was performed on Thermo Scientific Escalab 250 Xi spectrometer. The surface morphologies were measured by a Veeco Dimension Icon atomic force microscopy (AFM). The electrical properties of the capacitors and TFTs were measured using a Keithley 4200.

3 Results and discussion

Figure 1a shows the GIXRD patterns of Ga_2O_3 thin films annealed at various temperature. Obviously, the film remains amorphous state when the temperature is lower than 450 °C. However, several diffraction peaks can be observed when the annealing temperature reaches to 550 °C. These peaks can be recognized and consistent with the primary planes of the β-Ga_2O_3 structure listed in the JCPDS 41-1103, even if their intensities are not absolutely homologous to those shown in this file, which may indicate exit of alignment or texturing effect [13]. For crystallized oxide dielectrics, the grain boundary usually leads to impurity diffusion and acts as prior path of leakage current, which seriously affects the reliability of devices. Figure 1b shows the refractive index curves of Ga_2O_3 films performed in the range 350–1000 nm. The thickness of the films annealed at 250, 350, 450 and 550 °C were determined as 73, 69,

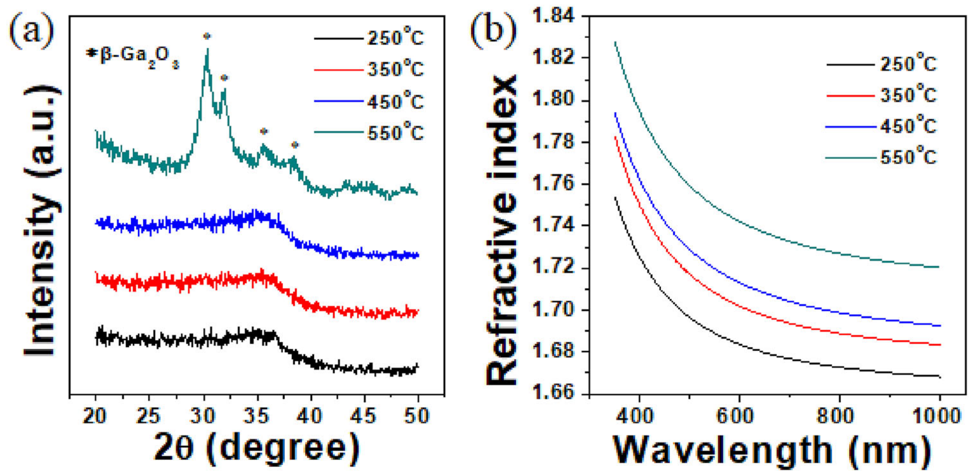

Fig. 1 **a** GIXRD patterns and **b** refractive index *vs.* wavelength curves of the Ga_2O_3 thin films annealed with various temperature

66, 63 nm by fitting with a Cauchy model, respectively. It also can be seen that the refractive indices decrease with the increase of wavelength and increase with the increase of annealing temperature. The difference of the thickness and optical constant can be explained by the densification process and phase transformation. It has been known from GIXRD patterns that as-deposited Ga_2O_3 films is amorphous and often contains many structural defects. With the annealing temperature increasing, the Ga_2O_3 films become denser. When the annealing temperature reaches to 550 °C, the β-Ga_2O_3 crystal structure formed and led to a larger increase of refractive indices due to the growth of crystal grains. From surface morphologies measured by AFM shown in Fig. 2, the root mean square (RMS) roughness of films annealed at 250 °C, 350 °C, 450 °C, 550 °C were 0.118, 0.121, 0.128, 0.463 nm, correspondingly. The Ga_2O_3 thin films show relatively smooth surface when the annealing temperature is less than 450 °C. The increased RMS value of 550 °C annealing film can be attributed to the crystallization, which is consistent with the result of GIXRD. Generally, a smooth surface can suppress gate leakage current, however, a rough surface would generate electronic traps or defects due to field-intensification inhomogeneous and deteriorate the transistor performance.

Figure 3a shows the O 1 s XPS spectra of Ga_2O_3 films. The peaks were fitted into a low-energy peak centered at 530.3 eV and a high-energy one at 531.9 eV. It was known that the peak at the 530.3 eV is associated with Metal–Oxygen bond species. As well, the peak at 531.9 eV is attributed to Metal-Hydroxide bond groups, such as OH- or H_2O on the film surface [11, 14]. For simplicity, O1, O2 and O1 + O2 are defined as the areas of low-energy peak, high-energy peak and the total area of the O 1 s peak. Consequently, O1/(O1 + O2) and O2/(O1 + O2) denote the relative quantity of Metal–Oxygen bond and Metal-Hydroxide bond in the Ga_2O_3 thin films. The ratio of O1/(O1 + O2) and O2/(O1 + O2) are calculated and plotted in Fig. 3b. We found that the fraction of the Metal–Oxygen bond in Ga_2O_3 increased from 84.1 to 90.3% and the Metal-Hydroxide bond in Ga_2O_3 decreased from 15.9 to 9.7% when the annealing temperature goes up from 250 to 550 °C. The XPS results reveal that higher annealing temperature reduces the Metal-Hydroxide bond and improves bulk Metal–Oxygen bond. It was noted that the Metal-Hydroxide bond can discrete energy levels and generate trap states in the forbidden band of Ga_2O_3 films, leading to the increased leakage current and the reduced breakdown voltage [15, 16]. Figure 3c exhibits the XPS Ga 3d spectra. It can be seen that all the peaks are in the range of 20.0 to 20.3 eV. However, with the annealing temperature rise, Ga 3d peaks are shifted to lower binding energy, which can be attribute to progressive oxidization or decrease of coordination number of Ga^{3+} in the films [17].

The leakage current density of Ga_2O_3 thin films is shown in Fig. 4a. For the films annealed at 250 °C, 350 °C, 450 °C and 550 °C, the leakage current densities were 4.2×10^{-6}, 2.4×10^{-6}, 1.9×10^{-6} and 6.6×10^{-5} A cm^{-2} (at 1.5MV/cm^2), respectively. The leakage current for low temperature annealed films may relate to hydroxyl groups and nitrate which provide leakage paths. Obviously, the 350 °C and 450 °C annealed films show lower leakage currents density, which mainly caused by thermal pyrolysis of nitrate and hydroxyl groups as well as the formation of

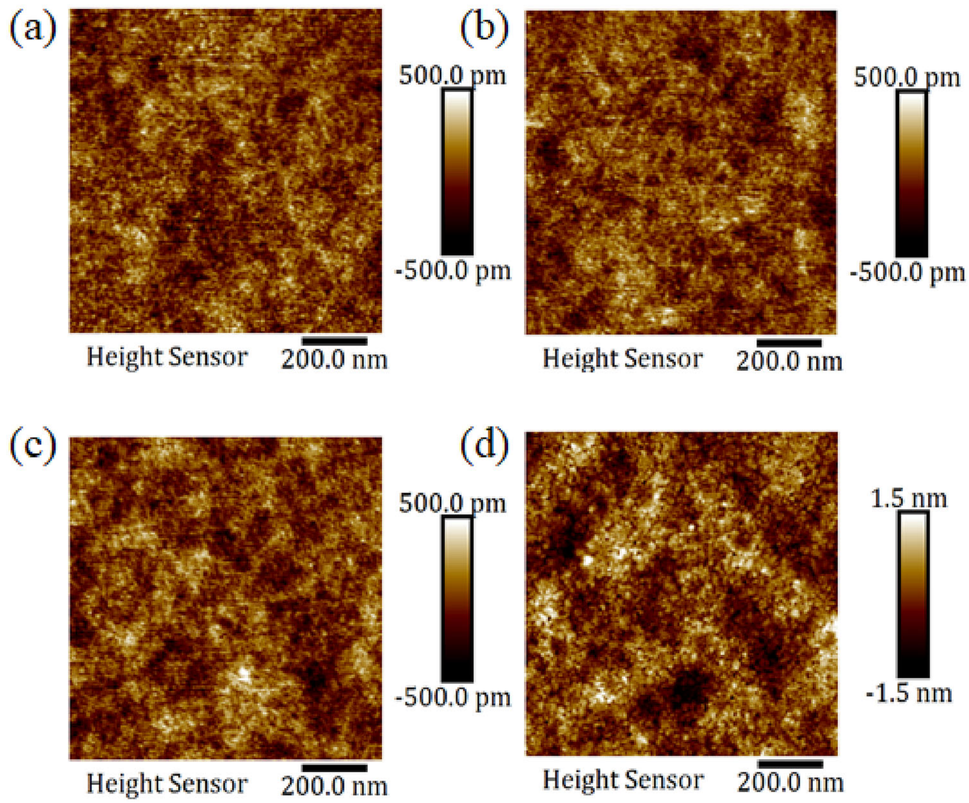

Fig. 2 AFM images of the Ga_2O_3 thin films annealed with various temperatures. **a** 250 °C, **b** 350 °C **c** 450 °C and **d** 550 °C

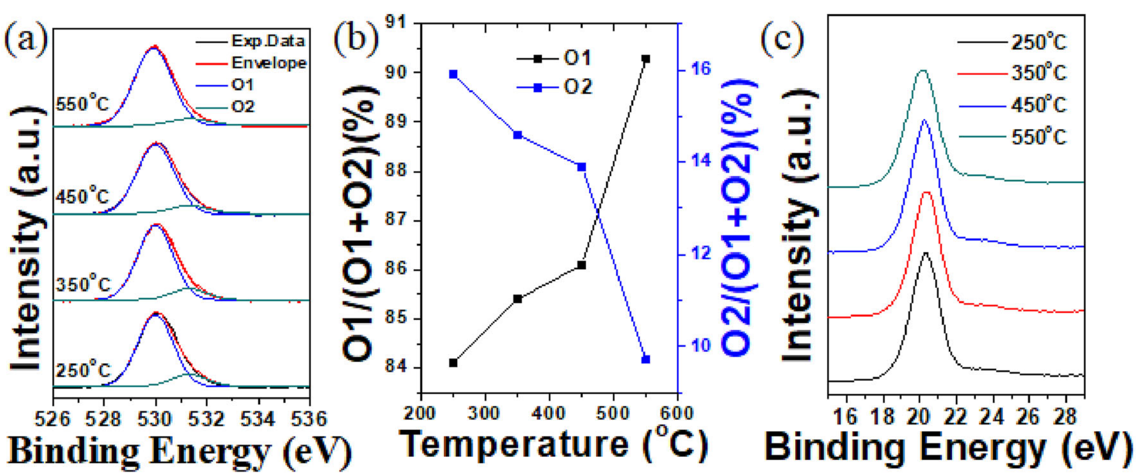

Fig. 3 **a** XPS spectra of O 1 s peaks for Ga_2O_3 thin films annealed with various temperatures. **b** Summarized ratios of oxygen ions states and bonded oxygen (**c**) The corresponding Ga 3d spectra of the Ga_2O_3 thin films annealed with various temperatures

metal oxide framework [18]. However, the leakage current density increased dramatically when temperature reaches to 550 °C, resulting from the crystallization of Ga_2O_3 film identified by GIXRD. Figure 4b shows the C-V curves of $Al/Ga_2O_3/Si$ capacitors at 1 MHz. It was observed that the capacitance at accumulation range increases when the annealing temperature rising, but it dramatically reduces when the temperature reach to 550°C. The relative dielectric constant of the Ga_2O_3 thin films can calculated by the following formula: $C = \varepsilon_0 \varepsilon_r s/d$, where C, ε_0, ε_r, s and d are the dielectric capacitance, absolute dielectric constant, relative dielectric constant, the area of electrode and thickness of the dielectric layer, respectively. Assuming 2.5 nm thick native SiO_2 with a dielectric constant of 3.9 on the Si

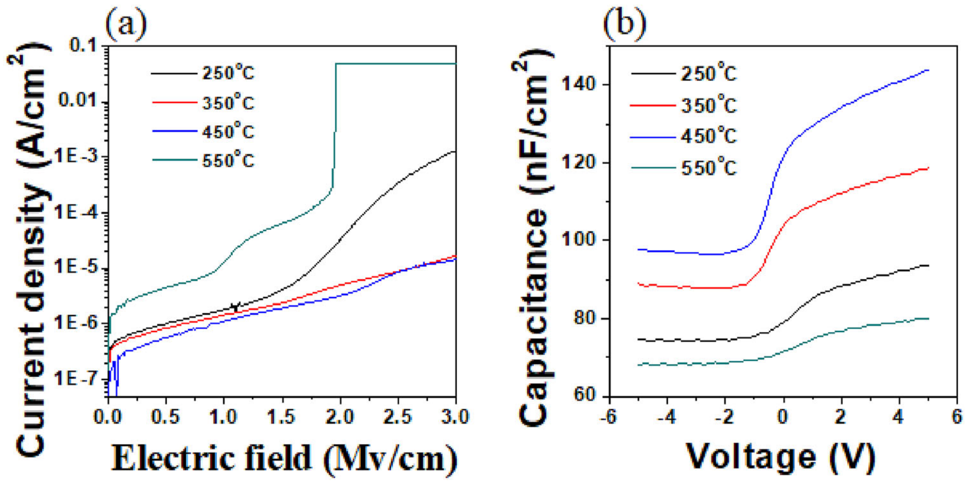

Fig. 4 **a** The leakage current density and **b** C-V curves of the Ga_2O_3 thin films annealed at various temperatures

bottom electrode, C can be modeled as Ga_2O_3 and SiO_2 capacitor in series, that is $1/C = 1/C_{Ga2O3} + 1/C_{SiO2}$. Accordingly, the calculated relative dielectric constant for Ga_2O_3 films annealed at 250 °C, 350 °C, 450 °C, 550 °C were 7.7, 9.3, 10.8, and 5.7, respectively, consistent with the surface morphology results of AFM.

Based on the above analysis, In_2O_3 TFTs integrated with 450 °C annealed Ga_2O_3 dielectric were fabricated. The output curves measured with the V_{GS} varied from 0 to 5 V in step of 1 V and transfer curves measured at a fixed V_{DS} of 5 V are shown in Fig. 5a, b. The device exhibits typical n-type field-effect transistor behavior with low operation voltage. The electrical hysteresis was negligible indicating small amounts of interface traps between the Ga_2O_3 dielectric and the In_2O_3 channel layer. The mobility (μ) and the subthreshold slope (SS) of the TFTs can be calculated by the following Eqs. (1) and (2) [19, 20].

$$I_{DS} = \left(\frac{\mu C_i W}{2L}\right)(V_{GS} - V_T)^2 \quad (1)$$

$$SS = \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}}\right)^{-1} \quad (2)$$

Here, C_i is the areal capacitance, V_T is the threshold voltage. The V_T was extracted by fitting the straight line of the square root of I_{DS} vs. V_{GS} in the saturation region and extrapolating to $I_{DS} = 0$. Just as mentioned above, C_i can be modeled as Ga_2O_3 and SiO_2 capacitor in series and was calculated to be 1382 nF cm^{-2}. The device exhibits a high mobility of 8.5 cm^2/Vs with a current on/off ratio of 10^4, a near zero threshold voltage of −1.4 V and a low SS of 0.41 V/Dec.

Figure 5c shows the evolution of the transfer properties of In_2O_3 TFT with different stress durations. A voltage of 3 V was constantly biased to gate electrode and the source electrode were grounded for

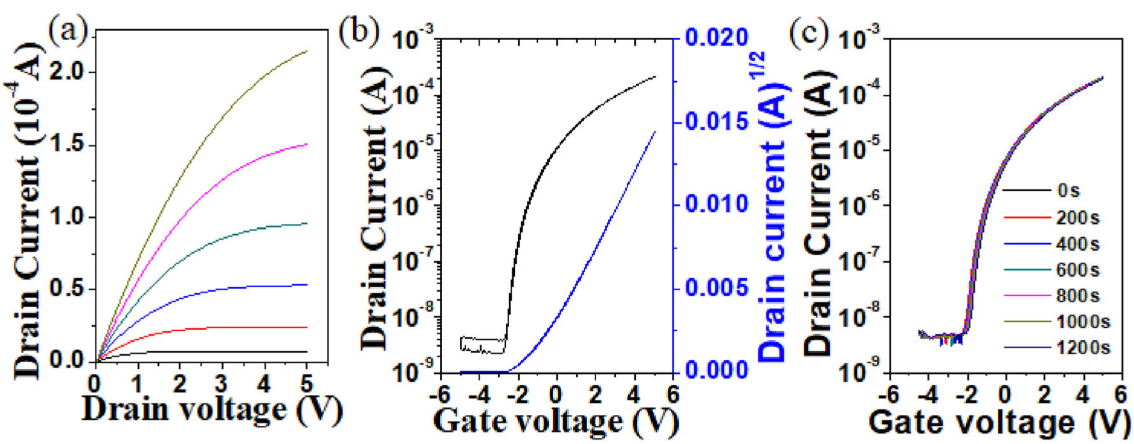

Fig. 5 **a** Output curves, **b** transfer curves and **c** bias stress stability of the In_2O_3 TFT using 450 °C annealed Ga2O3 dielectric

1200 s. The device exhibits an insignificant threshold voltage shift of 0.26 V indicating excellent operational stability. This negligible value shift also reveals that there are very few trap defects existing in the dielectric and the channel layer [21].

4 Conclusion

In summary, we have fabricated the solution-processed Ga_2O_3 thin films and investigated the optical, microstructure, surface morphology, composition and electrical properties. It was found that the dielectric properties of amorphous Ga_2O_3 thin films are excellent, but it was deteriorated after crystallization when annealing temperature rising. Moreover, oxide TFTs were fabricated using the optimized amorphous Ga_2O_3 dielectrics. The devices exhibit a high mobility of 8.5 cm^2/Vs, a threshold voltage of −1.4 V, a current on/off ratio of 104 and a subthreshold swing of 0.41 mV/Dec as well as excellent bias stress stability.

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