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Effect of purity of Al interlayer on stress and thermal cycling durability of die-attach Ni–Sn joints

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ABSTRACT

In this study, an effect of Al layer insertion to die-attach Ni–Sn joints with semiconductor chips by solid–liquid interdiffusion bonding on the stress and thermal cycling durability was investigated focusing on the purity of Al. The results showed that the Al interlayer significantly decreased the residual compressive stress in the semiconductor chips after bonding, and the use of 4N-Al (99.99 wt%) decreased the residual stress more significantly than the use of 2N-Al (99 wt%). Additionally, during thermal cycling up to 200 °C, a change from compressive to tensile stress occurred, which decreased with time; the decrease for 4N-Al was greater than that for 2N-Al. After 500 thermal cycles between − 40 and 200 °C, fewer voids were observed in the Ni–Sn SLID with Al interlayer joints than those in the Ni–Sn SLID joint, and the voids were fewer in the 2N-Al interlayer joint than in the 4N-Al interlayer joint; this suggests a balance in the relationship between stress reduction and thermal durability in the chip of die-attach joints. Therefore, it indicated that the use of Al interlayer and optimization of the composition are important to balance high stress reduction in the semiconductor chips and thermal durability of die-attach joints.

1 Introduction

With the demand to reduce CO_2 emissions in the automobile industry, SiC power modules have been developed to enhance the performance of electrical vehicles [1, 2]. SiC power devices enable a high output because of the high efficiency and thermal stability at high operation temperature above 200 °C [3, 4]. However, the components that comprise these power modules are required to have heat resistance to ensure reliability. One important component to bond power devices and metal electrodes is the die-attach material. Sn-based solders have been widely used as die-attach materials due to their ductility, which is essential to prevent stress concentration in die-attach power devices generated by the mismatch of thermal coefficient between devices and metal electrode. However, Sn-based solders, having low melting points of approximately 230 °C, cause the deterioration of durability of the bonding layer due to the low thermal fatigues. To increase the melting temperature of the bonding layer, high-temperature soldering [5–7], sintering with nano/micro particles [8–12], and solid–liquid interdiffusion (SLID)

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bonding using Ni–Sn, Cu–Sn, and Au–Sn solders (also known as transient liquid phase (TLP) bonding) [13–15] have been proposed. Die-attach joints using the above methods are expected to enhance strength and thermal fatigue because the bonding layers have higher melting temperatures than those of Sn-based solders. However, die-attach joints with high-strength bonding materials have a critical issue of lower reliability due to stress concentration in power devices after bonding or under thermal cycling due to lower ductility of bonding layers [16, 17]. To overcome this problem, the methods of mixing highly ductile resin powders with nanoparticles or TLP powders have been proposed recently [18, 19]. However, it is difficult to obtain stable mechanical properties of the bonding layer with these methods because the formation of the composite structures of the bonding layer is strongly influenced by the bonding process.

Therefore, we considered the use of an Al sheet with high ductility equivalent to a Sn-based solder and higher strength than that of the Sn-based solders. Additionally, the Al sheet can exhibit stable mechanical properties due to its homogeneous microstructure. However, the Al cannot be directly used as bonding material due to its melting temperature of 660 °C, which is out of the soldering temperature range below 450 °C. In addition, Al forms strong surface oxidation, which reduces bond ability. Therefore, we used SLID reaction with a Ni layer, which is practically used for plating on Al and power devices, to bond with Al, and proposed the insertion of the Al interlayer into a semiconductor chip and a Cu electrode as an effective method to use Ni–Sn solders by SLID bonding. In our previous study [20], the stress reduction in the chips of the joints and the suppression of crack propagation in the joints after thermal cycling at temperatures up to 200 °C have been demonstrated by using an Al interlayer, indicating that the Al interlayer enhances the thermal cycle reliability of the Ni–Sn joint by SLID bonding. However, these results did not clarify the effect of the Al interlayer on the stress reduction in semiconductor chips and the thermal durability of the die-attach joint. In this study, we focused on the purity of Al interlayer, which affects the mechanical properties, and investigated the effect of purity on the stress behavior of the chips of joints and thermal cycling durability.

2 Materials and methods

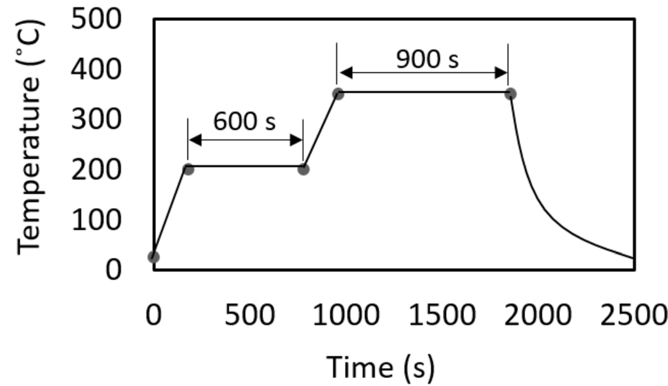
2.1 Joint preparation

Bonding layers between semiconductor chips (5 mm × 5 mm) and Cu plates (20 mm × 20 mm) were prepared by Ni–Sn bonding with and without an Al interlayer. Si chips and SiC chips were used for stress measurement and thermal cycling durability tests, respectively. Using physical vapor deposition (PVD), both sides of the chips were covered with Al, Ti, and Ni-sputtered layers. Cu plates were prepared from an oxygen-free rolled copper sheet. One side of the Cu plates was covered with Ni and Sn layers for Ni–Sn bonding without an Al interlayer. For the case of using an Al interlayer, the Ni layer was deposited on one side of the Cu plates. The Al interlayers, with size of 100 mm × 100 mm and thickness of 100 μm, were prepared from rolled Al sheets with different purities of 99 wt% (2N) and 99.99 wt% (4N). The sheets contain residual strain by the disorder of the atomic arrangement in the crystal due to the random plastic deformation by rolling. Therefore, the sheets were annealed at 350 °C for 1 h in argon atmosphere to remove the residual strain by using Al recrystallization. Subsequently, the oxides and contaminations on the surface of the Al sheets were removed by Ar ion sputtering for 5 min at a pressure of 0.5 Pa in the PVD chamber. Ni and Sn layers were then deposited on both sides of the Al sheets, followed by cutting into square pieces of size 7 mm × 7 mm.

All the joints were bonded using a batch-type reflow furnace in a hydrogen atmosphere. To form the Ni–Sn bonding layer, the joints were two-step annealed with a pressure of 0.5 MPa by the reflowed gas, as shown in Fig. 1a. For the case of using Al sheets, the Ni/Sn-sputtered Al sheet was set between the semiconductor chips and Cu plates, as shown in Fig. 1b. Table 1 represents a summary of the structure of Ni–Sn, Ni–Sn/Al(2N), and Ni–Sn/Al(4N) joints.

2.2 Stress measurement

To measure the stress in the chips generated by the bonding, Si chips were applied to the joints. The Si gauge chips have a higher sensitivity for stress than that for the SiC chips, due to the low Young's modulus of 190 GPa. A schematic illustration of the stress measurement system is shown in Fig. 2. Si chips with size of 5 mm × 5 mm were prepared from a Si (110)



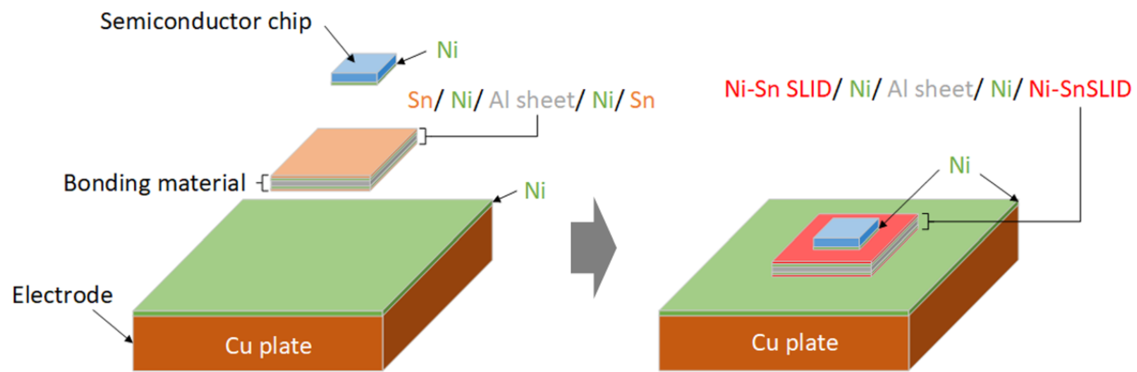


Fig. 1 **a** Temperature pattern of annealing to form Ni–Sn bonding layer and **b** schematic diagram of Ni–Sn bonding with an Al interlayer

Table 1 Structure of Ni–Sn, Ni–Sn/Al(2N), and Ni–Sn/Al(4N) joints

Joint	Structure		
	SiC or Si chip	Bonding layer	Cu plate
Ni–Sn	SiC (330) or Si (200)/Al (0.1)/Ti (0.1)/Ni (3)	None	Sn (5)/Ni (3)/Cu (3000)
Ni–Sn/Al(2N)		Sn (5)/Ni (3)/Al(2N) interlayer (100)/Ni (3)/Sn (5)	Ni (3)/Cu (3000)
Ni–Sn/Al(4N)		Sn (5)/ Ni (3)/Al(4N) interlayer (100)/Ni (3)/Sn (5)	

(): thickness of layer in μm

wafer and were composed of gauge elements with the size of 300 μm × 300 μm, as shown in Fig. 2a. The gauge elements were patterned with 1-mm intervals on the chips. The gauge elements were doped with B^+ ions to obtain a p-type Si layer to prevent temperature effect [21]. The stress was measured as voltage changes along the Si < 110 > direction at the center of the chip. Wheatstone bridge circuits were built by the joints, as shown Fig. 2b. The voltages at the points 2 (V_2), 3 (V_3), and 4 (V_4) were

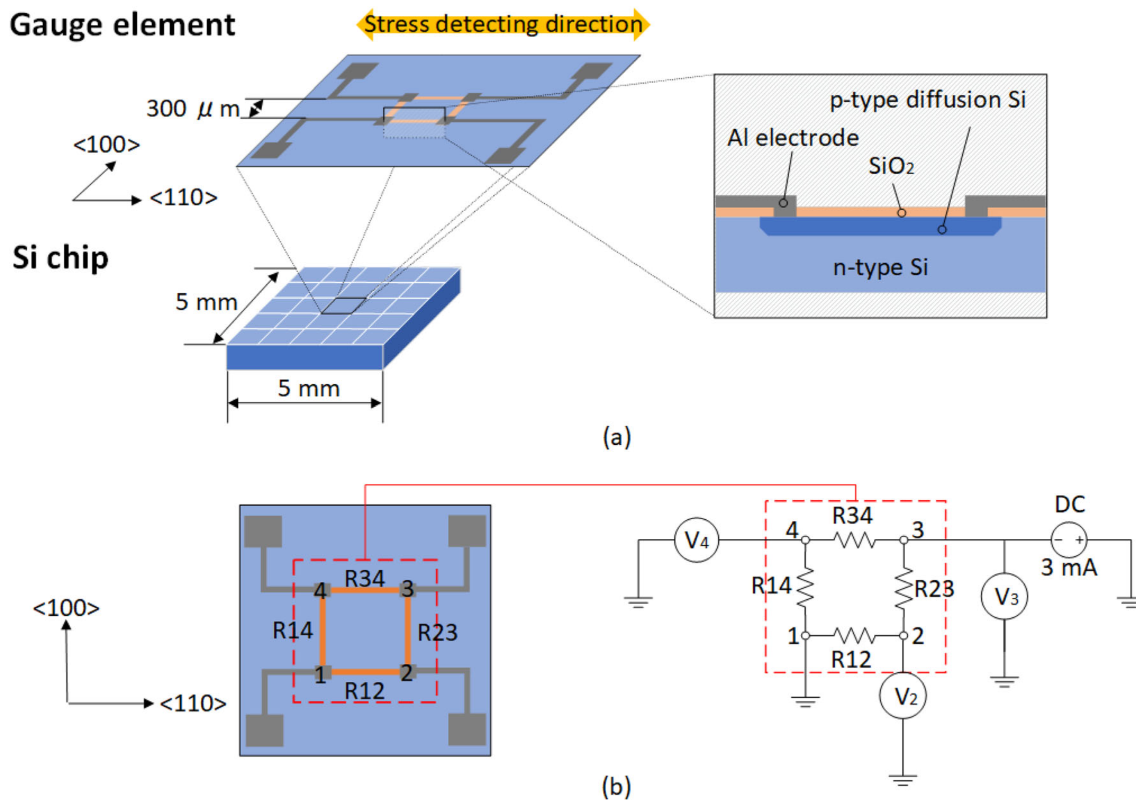


Fig. 2 Schematic illustration of **a** Si gauge chip and **b** stress measurement circuit

measured by applying electric current of 3 mA. The stress was calculated from Eq. (1) by assuming the piezoresistivity coefficient of 160 $m^2 N^{-1}$ as previously reported [20, 22, 23]. Positive and negative stress indicate tensile and compressive states, respectively.

$$\sigma = \frac{1}{160 \times 10^{-6}} \times \frac{V_{initial} - V_{test}}{V_3} \quad (1)$$

2.3 Evaluation of thermal cycling durability

The thermal cycling durability of the joints was evaluated at temperatures between − 40 and 200 °C for 500 heating–cooling cycles using a thermal cycling furnace. All the joints were observed by scanning acoustic microscopy (SAM) using ultrasonic wave with a frequency of 50 MHz before and after thermal cycling to detect the defects.

After 500 thermal cycles, the cross-section of the joints was prepared by cutting at the center of the chips and polishing using a cross-section polisher (CP). All the cross-sectional specimens were observed using scanning electron microscopy (SEM), and their composition were obtained using energy dispersive X-ray spectroscopy (EDS). The Ni–Sn/Al joints were further analyzed by electron backscatter diffraction (EBSD) and orientation imaging microscopy (OIM) analysis to estimate the grain size at the Al interlayer. The grain boundaries were determined as boundaries between neighboring dominants having differences of the crystallographic orientations above 5°.

3 Results and discussion

The cross-sectional SEM images of the joints are shown in Fig. 3. The uniform white-colored regions without the voids indicating the Ni–Sn bonding layers sandwiched between the Ni layers were clearly observed in all the joints. The composition of the Ni–Sn layers was $Ni_{42}Sn_{58}$ (at. %) which corresponds to Ni_3Sn_4. These results indicate that the fabricated joints were suitable for the evaluation of the stress and the thermal cycling durability.

The stress behavior of the joints with the Si chips measured at 25 °C on measurement time is shown

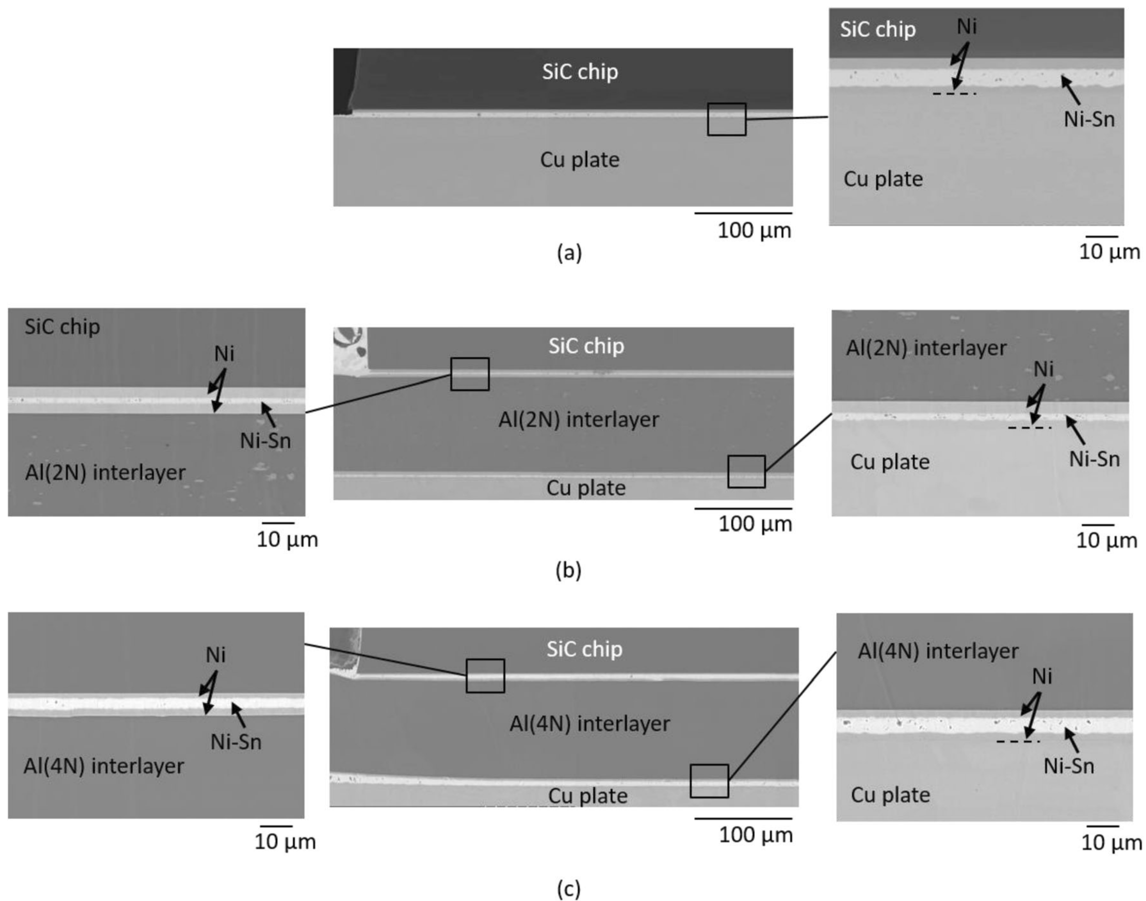


Fig. 3 Cross-sectional SEM images of **a** Ni–Sn, **b** Ni–Sn/Al(2N), and **c** Ni–Sn/Al(4N) joints

Fig. 4. After bonding, the chip showed the stresses of − 501 MPa for Ni–Sn, − 245 MPa for Ni–Sn/Al(2 N), and − 176 MPa for Ni–Sn/Al(4N). The compressive stress of the chips was decreased by using Al interlayers. In addition, the stress for Ni–Sn/Al(4N) was lower than that for Ni–Sn/Al(2N), indicating that the purity of Al interlayer is effective to suppress the residual stress generated in the chip of the joint. On the other hand, the stresses were

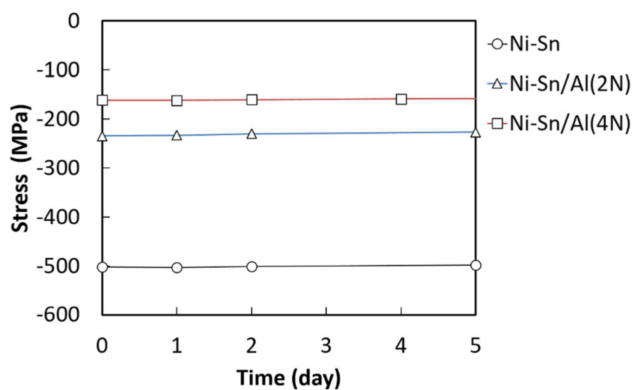


Fig. 4 Dependence of the joints with the Si chips on measurement time for **a** Ni–Sn, **b** Ni–Sn/Al(2N), and **c** Ni–Sn/Al(4N) joints. Measurement temperature was fired to be 25 °C

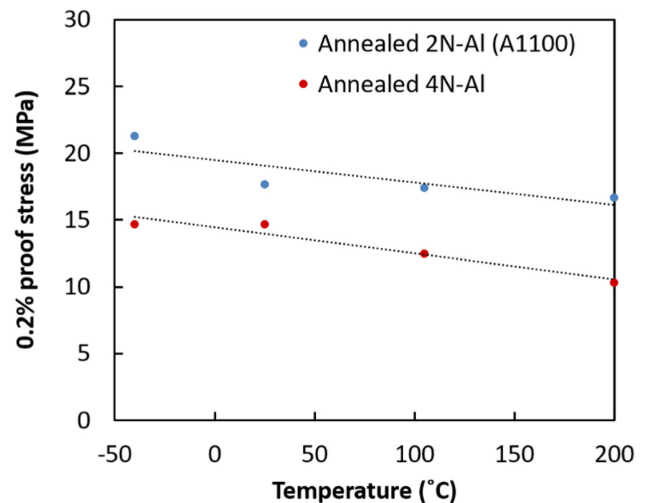


Fig. 5 0.2% proof stress of 2N-Al and 4N-Al depending on temperatures

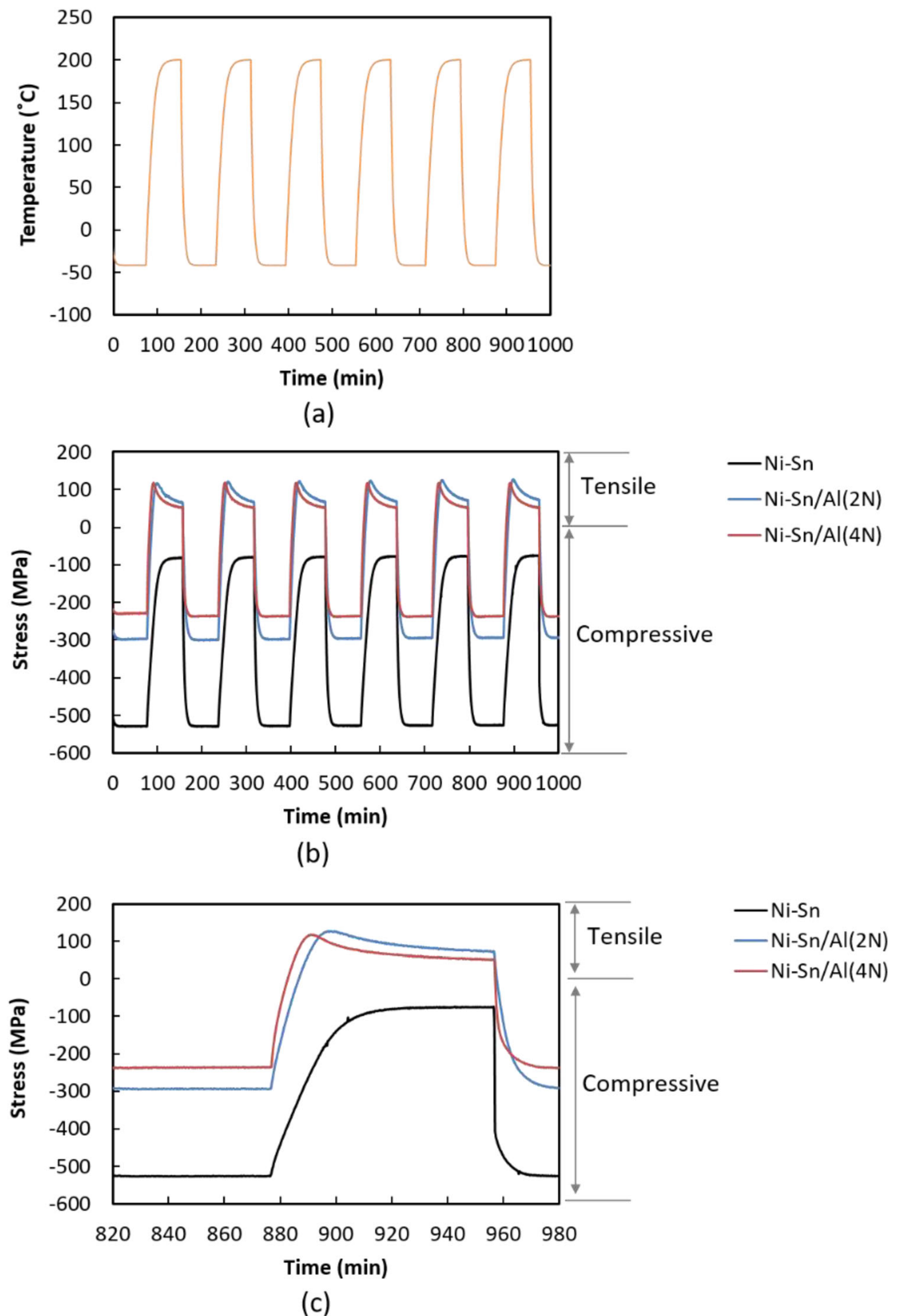


Fig. 6 Changes of **a** measurement temperature and **b** stress for thermal cycling and **c** stress change at the measurement time from 820 to 980 min. in the Si chip for Ni–Sn, Ni–Sn/Al(2N), and Ni–Sn/Al(4N) joints

constant for all chips regardless of the measurement time, meaning that the creep deform did not occur in the bonding layers of the joints. The differences of the stress depending on the bonding layers was attributed to the ductility and strength of Al. For the case of the chips without an Al interlayer, the large residual stress generates in the chip, due to the large mismatch of the coefficient of thermal expansion between Si chip and Cu plate (Si: 2–3 $\times$ 10^{-6} K^{-1}, Cu: 17 $\times$ 10^{-6} K^{-1}) [24, 25] and the low ductility of the Ni–Sn layer. In contrast, using the Al interlayer, the residual stresses in the chips were declined, and the stress became lower when using 4N-Al. Figure 5 shows the relationship between temperature and

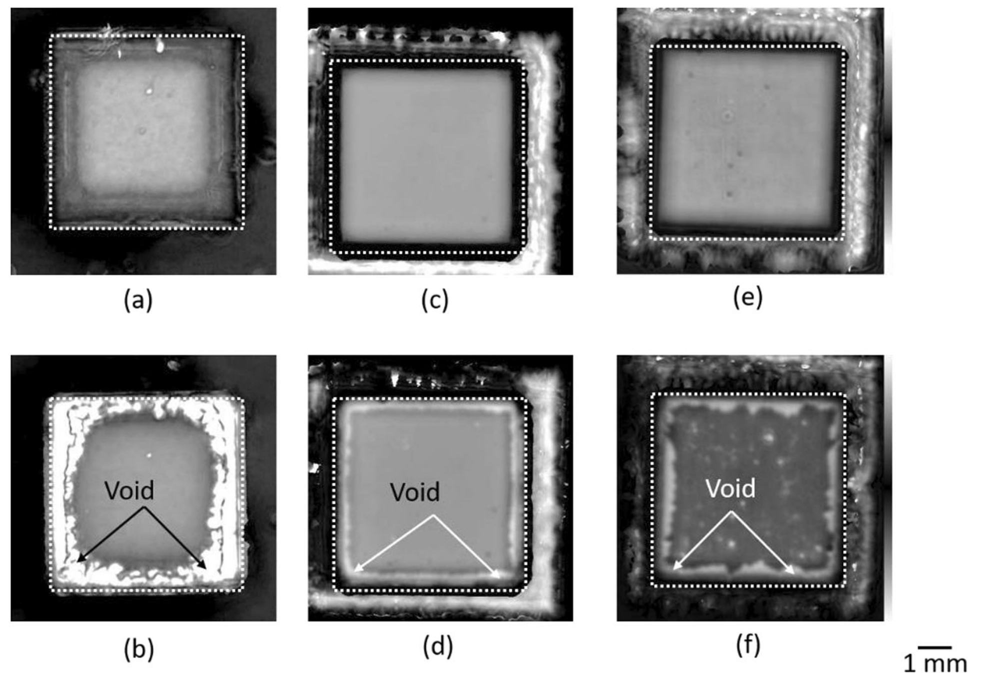


Fig. 7 SAM images before and after thermal cycling of **a**, **b** Ni–Sn, **c**, **d** Ni–Sn/Al(2N), and **e**, **f** Ni–Sn/Al(4N) joints with SiC chips

0.2% stiffness for 2N-Al (A1100) and 4N-Al. The data were obtained from tensile test using stress relief bulk metals at strain rate of 2×10^{-3} s^{-1}. Generally, the lower 0.2% stiffness leads to high plastic deformability. The 0.2% stiffness of 4N-Al is lower than that of 2N-Al regardless of temperature; therefore, the plastic deformability of 4N-Al is inferred to be higher than that of 2N-Al. Therefore, the Al(4N) interlayer is thought to deform plastically in the bonding process more than the Al(2N) interlayer, resulting in the reduction of the stress generated in the chips. From the results, it was clarified that the reduction in residual stress of die-attach Si chip after bonding is produced by using a high-purity Al interlayer produces.

The dependence of the stress for the joints with the Si chips on the thermal cycling are shown in Fig. 6. All joints had no changes in the stress by the cycling time. For the case of the Ni–Sn joint, only the compressive stress occurred and changed depending on the measurement temperature. The maximum value of the compressive stress of the Ni–Sn joint was 526 MPa at the temperature of − 40 °C. On the other hand, the stress for Ni–Sn/Al joints changed from compressive to tensile states during the temperature rise process and from tensile to compressive states during the cooling process. The compressive stress at the temperature of − 40 °C for the Ni–Sn/Al joint was 294 MPa for Al(2N) and 237 MPa for Al(4N). Ni–Sn/Al joints also showed a decrease in the tensile stress with the temperature rise of approximately 200 °C. The decrease of the tensile stress for Ni–Sn/Al(4N) was greater than that for Ni–Sn/Al(2N), whereas both displayed a maximum stress of approximately 125 MPa.

The difference of the change in stress between the Ni–Sn and Ni–Sn/Al joints was possibly caused by a higher coefficient of thermal expansion of Al (23×10^{-6} K^{-1}) than that of Ni_3Sn_4 (3.5×10^{-6} K^{-1}). Therefore, during heating to 200 °C, the stress in the chips of the Ni–Sn/Al joint changed from compressive to tensile state due to the large expansion of Al. In contrast, the difference of the decrease in tensile stress holding at 200 °C between Ni–Sn/Al(2N) and Ni–Sn/Al(4N) joint was caused by the difference of the thermal 0.2% stiffness between 2N-Al and 4N-Al, as mentioned above. The relationship between the temperature and 0.2% stiffness (Fig. 5) indicates that the 0.2% stiffness was lower at high temperatures than at low temperatures for all Al compositions, and the 0.2% stiffness of 4N-Al was lower than that of 2N-Al regardless of temperature. The lower 0.2% stiffness of Al caused the tensile stress reduction in the chips because the low 0.2% stiffness of the material became easy to deform plastically.

From these results, it is clarified that the insertion of the high-purity Al interlayer is effective to decrease the stress in the chips of die-attach joints.

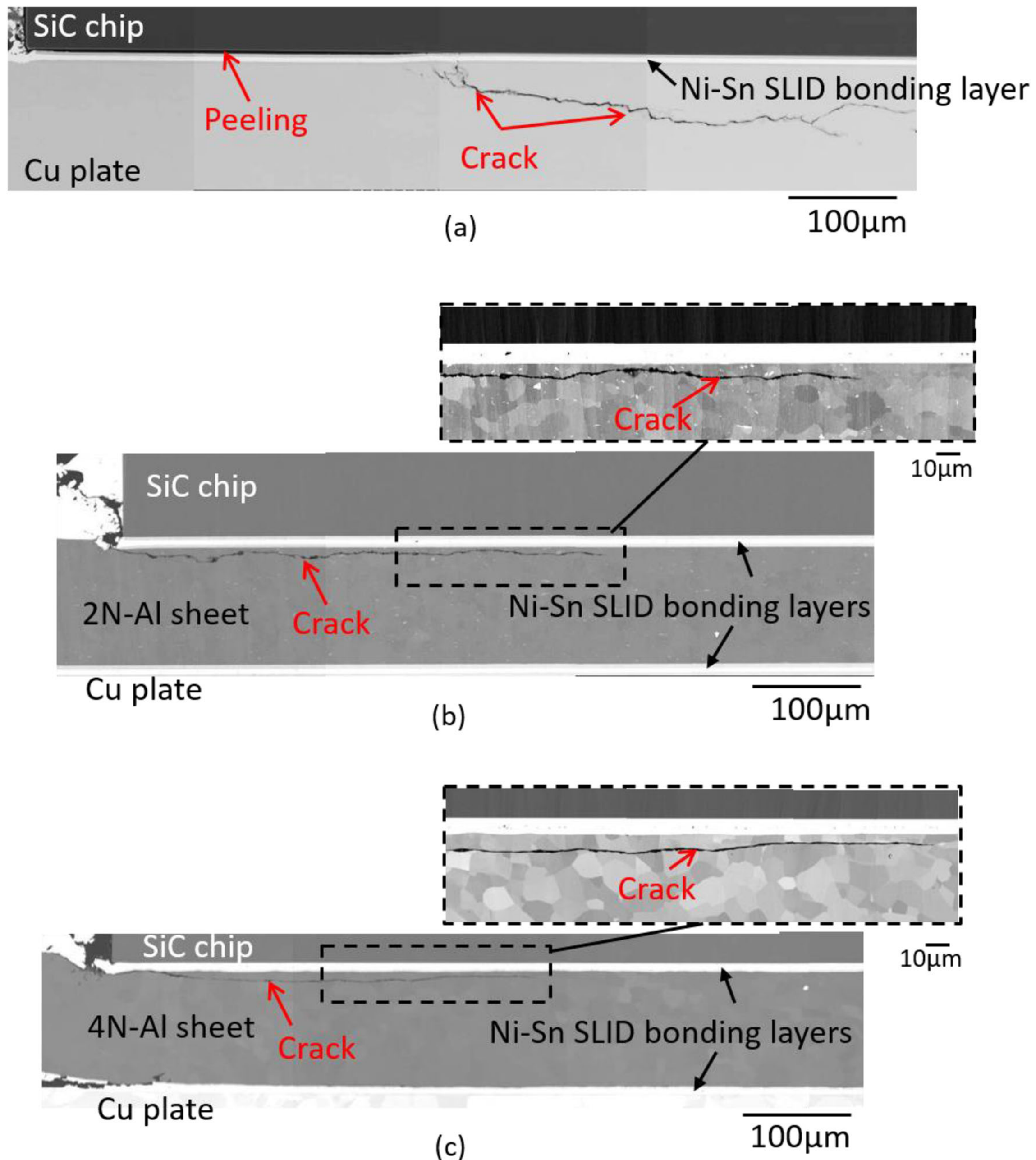


Fig. 8 Cross-sectional SEM images of **a** Ni–Sn, **b** Ni–Sn/Al(2N), and **c** Ni–Sn/Al(4N) joints with SiC chips after 500 thermal cycles

The SAM images of the bonding layers of the Ni–Sn, Ni–Sn/Al(2N), and Ni–Sn /Al(4N) joints before and after 500 thermal cycles are shown in Fig. 7. The initial states of the joints showed no void in the SAM images (Fig. 7a, c, and e) independent of the bonding layers, according to the SEM images shown in Fig. 3. Through the thermal cycling, the void was generated at the edge of the bonding area for all joints and the amount was changed by the bonding layers (Fig. 7b, d, and f). The Ni–Sn/Al bonding layers showed that the void area was less than one quarter smaller than that of the Ni–Sn bonding layer. In addition, the size of the void was decreased with lower purity of the Al interlayer. The result shows that the use of the Al interlayer is effective to improve thermal cycling durability; however, the use of Al with higher purity decreases thermal cycling durability.

The cross-sectional SEM images of the joints after the thermal cycling are shown in Fig. 8. The peeling between the SiC chip and the Ni layer, and the crack

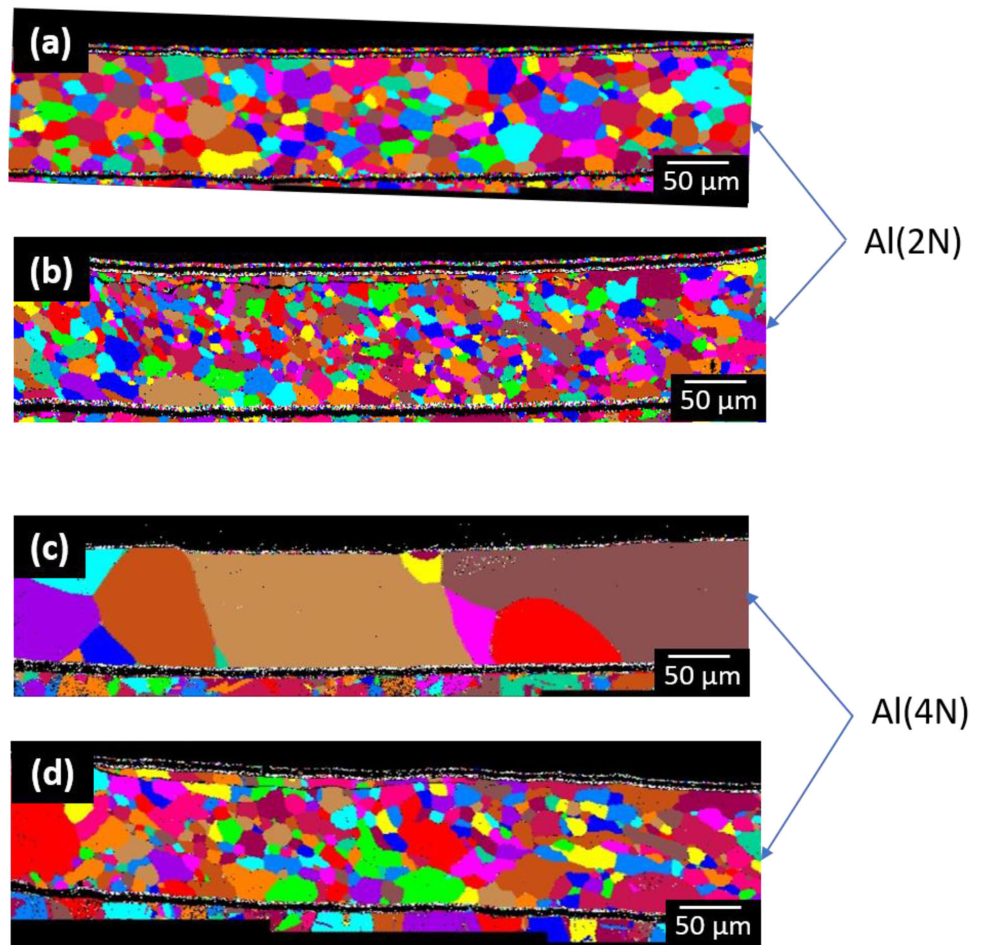


Fig. 9 EBSD grain maps of Al interlayers in Ni–Sn/Al joints before and after 500 thermal cycles for **a**, **B** Al(2N) and for **c**, **d** Al(4N), respectively

in the Cu plate were observed in the Ni–Sn SLID joint. Although the cracks were observed in the Al interlayer of the Ni–Sn/Al joints, the peeling did not occur in the joints, indicating that the plastic deformation of the Al interlayers induced the reduction of the stress in the joints and suppressed the occurrence of the peeling. The crack shape of the Al interlayer of the Ni–Sn/Al(4N) joint was nearly a straight line; however, that of the Ni–Sn/Al(2N) joint was a meandering line. This suggested that the high purity of Al could not possibly suppress the crack propagation because the precipitation strengthening in the Al could not occur for a reduced impurity level (e.g., Si, Fe) [26].

The EBSD grain maps of the Al interlayers for Ni–Sn/Al joints with the SiC chips before and after the thermal cycling are shown in Fig. 9. The initial grain size was changed by the purity of the Al layers, and was ~ 50 and ~ 400 µm for Al(2N) and Al(4N), respectively. Through thermal cycling, their grain sizes became smaller than their initial sizes. The grain refinement of the Al interlayers indicates recrystallization, which was caused by the repeated plastic deformation under thermal cycling. The same phenomenon was reported for Sn solders [27, 28], which was induced by the repeated plastic and creep deformation under thermal cycling. The results indicate that the Al interlayers of the Ni–Sn/Al joints enable strain relaxation similar to the Sn solders.

4 Conclusion

In this study, the effect of an Al layer insertion to die-attach Ni–Sn joints with semiconductor chips by SLID bonding on the stress and thermal cycling durability were investigated, focusing on the purity of Al. The obtained results demonstrated that with or without the use of an Al interlayer, there was a decrease in the residual compressive stress. In the chip of joints after bonding, the stress was further decreased owing to the use of the Al interlayer.

Additionally, the use of the 4N-Al (99.99 wt%) interlayer resulted in a greater decrease in the compressive stress compared with that with the use of the 2N-Al (99 wt%) interlayer. After that 500 thermal cycles between − 40 and 200 °C, the number of voids observed in the Ni–Sn SLID joint with 2N-Al or 4N-Al interlayers were fewer than those in the Ni–Sn SLID joint without the Al interlayer, and the 2N-Al interlayer resulted in a fewer number of voids than the 4N-Al interlayer. These differences possibly resulted difference in strength, suggesting that the purity of 0.2% stiffness of Al, has an effect on stress behavior in semiconductor chips of joints, as well as thermal cycling durability. Thus, it was established that to balance high stress relaxation and thermal durability in die-attached joints, it is important to use an Al interlayer while optimizing its composition.

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Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

References

1. G. Mauromicale, A. Raciti, S. A. Rizzo, and G. Susinni, 45th Annual Conference of the IEEE Industrial Electronics Society (IECON), 2019, pp. 1973–1978.
2. R. Ramachandran, J. Nielsen, and M. Nymand, 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 3503–3507
3. K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, H. Reisinger, IEEE Trans. Electron. Devices **66**, 4604 (2019)
4. J.O. Gonzalez, R. Wu, S. Jahdi, O. Alatise, IEEE Trans. Ind. Electron. **67**, 7375 (2020)
5. Y. Yamada, Y. Takaku, Y. Yagi, I. Nakagawa, T. Atsumi, M. Shirai, I. Ohnuma, K. Ishida, Trans. Jpn. Inst. Electron. Packag. **2**, 79 (2009)
6. G. Zeng, S. McDonald, K. Nogita, Microelectron. Reliab. **52**, 1306 (2012)
7. M. Prach, R. Koleňák, Procedia Eng. **100**, 1370 (2015)
8. S.T. Chua, K.S. Siow, J. Alloys Compd. **687**, 486 (2016)
9. X. Liu, H. Nishikawa, Scr. Mater. **120**, 80 (2016)
10. S.A. Paknejad, S.H. Mannan, Microelectron. Reliab. **70**, 1 (2017)
11. N. Saud, R.M. Said, I.O.P. Conf, Ser. Mater. Sci. Eng. **701**, 12050 (2019)
12. W.S. Hong, M.S. Kim, C. Oh, J. Electron. Mater. **49**, 188 (2020)
13. Z.X. Zhu, C.C. Li, L.L. Liao, C.K. Liu, C.R. Kao, J. Alloys Compd. **671**, 340 (2016)
14. B. Lee, S. Hyun, J. Yoon, J. Mater. Sci. Mater. Electron. **28**, 7827 (2017)
15. D.H. Jung, A. Sharma, M. Mayer, J.P. Jung, Rev. Adv. Mater. Sci. **53**, 147 (2018)
16. P. Quintero, T. Oberc, and P. McCluskey, Electronic Components and Technology Conference, 2008, pp. 2131–2138.
17. T. Ishizaki, D. Miura, A. Kunob, R. Nagao, S. Aoki, Y. Ohshima, T. Kino, M. Usui, Y. Yamada, Microelectron. Reliab. **64**, 287 (2016)
18. H. Tatsumi, A. Lis, H. Yamaguchi, Y. Kashiba, A. Hirose, IEEE Trans. Compon. Packaging Manuf. Technol. **5**, 2111 (2019)
19. K. Sugiura, T. Iwashige, K. Tsuruta, C. Chen, S. Nagao, T. Funaki, K. Suganuma, IEEE Trans. Compon. Packag. Manufact. Technol. **9**, 609 (2019)
20. H. Ito, M. Kuwahara, H. Kadoura, M. Usui, IET Power Electron. **12**, 492 (2019)
21. Y. Nishibe, Y. Yagi, K. Nishiyama, H. Ohno, K. Akamatus, N. Ohno, ASME **2**, 925 (1992)
22. C.S. Smith, Phys. Rev. **94**, 42 (1954)
23. R. Hull, *Properties of Crystalline Silicon* (INSPEC, London, 1999), pp. 421–428. https://www.worldcat.org/title/properties-of-crystalline-silicon/oclc/41984192
24. H. Watanabe, N. Yamada, M. Okaji, Int. J. Thermophys. **25**, 221 (2004)
25. J.D. James, J.A. Spittle, S.G.R. Brown, R.W. Evans, Meas. Sci. Technol. **12**, R1 (2001)
26. P. Li, H. Li, X. Liang, L. Huang, K. Zhang, Z. Chen, Mater. Sci. Eng. A **732**, 341 (2018)
27. J. Han, P. Gu, L. Ma, F. Guo, J. Liu, J. Electron. Mater. **47**, 2479 (2018)
28. H. Xu, F. Liu, L. Zhou, H. Zhao, M. Li, Microelectron. Reliab. **110**, 113623 (2020)

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