Journal of Materials Science: Materials in Electronics (2020) 31:12372–12381
https://doi.org/10.1007/s10854-020-03783-z

Impact of SiO_2 interfacial layer on the electrical characteristics of Al/Al_2O_3/SiO_2/n-Si metal–oxide–semiconductor capacitors

Nakibinge Tawfiq Kimbugwe[1] · Ercan Yilmaz[1,2]

Received: 11 March 2020 / Accepted: 10 June 2020 / Published online: 22 June 2020

Abstract
The aim of this study is to reduce the oxide and interface-trap charges and also improve the stability at the oxide–semiconductor interface by growing a SiO_2 interface layer on a Si wafer then depositing Al_2O_3 thin film. Effective oxide charges density (N_{ox}), border trap charges density (N_{bt}), interface states density (N_{it}), diffusion potential (V_D), donor concentration (N_D), and barrier height (Φ_B) were calculated using the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements at different annealing temperatures. The flat-band voltage (V_{fb}) changed with annealing temperature and the V_{fb} value for the 450 °C annealed sample was closest to the ideal V_{fb}. The sample also possessed a high dielectric constant. For these reasons, C–V and G/w–V values of this sample at different frequencies were obtained. Compared to previous studies, very low N_{bt}values (~ 10^9 eV^{-1} cm^{-2}), low N_{it} values (~ 10^{10} eV^{-1} cm^{-2}) and high Φ_B values for the annealed samples were obtained due to the SiO_2 interface layer.

1 Introduction

The metal–oxide–semiconductor (MOS) capacitors have been the foundation for microelectronic and optoelectronic devices since the 1960s [1]. The oxide plays a major role in charge and energy storage due to its significant dielectric constant (k). This has made the MOS capacitor be used in MOS-based technology such as new-generation biosensors, radiation sensors, and charged-coupled devices [2, 3]. The oxide properties together with its stability on semiconductor materials affect the electrical characteristics of the entire MOS structure. These electrical characteristics determine the applicability of the structure in different technologies [4] and are usually investigated by taking capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements. The conductance (G/w) measurement is based on the exchange of majority charge carriers between the majority charge carrier band of silicon and the interface states. This exchange results in conductance losses [4].

Initially, SiO_2 was solely used as the oxide in MOS capacitors because of its good electrical and material properties such as excellent insulation and interfacial bonding especially with Si [5, 6]. However, later on, researchers suggested a need to replace SiO_2 since it was associated with high current leakage especially for thicknesses less than 2 nm [7]. Another reason for the replacement was that SiO_2 led to the poor performance of devices functioning at high temperatures or high electric fields. The investigated alternatives included high-k materials such as Al_2O_3, HfO_2, and Sm_2O_3 [5]. The deposition of these high-k materials directly on Si results in the formation of uncontrollable silicate or oxide layers in the high-k/Si interface which causes a decline in the effective dielectric constant, device performance, and channel mobility. Therefore, since SiO_2 is highly stable with Si, researchers suggested growing a SiO_2 layer on Si then depositing a high-k dielectric on it to reduce the lattice mismatch at the high-k/Si interface [8–11].

Previously, a study [12] on the Al/Al_2O_3/Si MOS capacitor was done at our laboratory. Interface-trapped charges density, effective oxide charge density, series resistance, and flat-band shifts were the main electrical parameters analyzed. These electrical parameters were obtained by the aid of C–V and G/ω–V) measurements for samples annealed at different temperatures. However, some electrical parameters were unsatisfactory which indicated that the quality of the fabricated Al/Al_2O_3/Si MOS capacitor

✉ Ercan Yilmaz
yilmaz@ibu.edu.tr

[1] Nuclear Radiation Detectors Applications and Research Center, Bolu Abant Izzet Baysal University, 14030 Bolu, Turkey

[2] Physics Department, Bolu Abant Izzet Baysal University, 14030 Bolu, Turkey

needs improvement. For example, we obtained big flat-band shifts, high series resistance (R_s) values, and the flat-band voltages were not close to the ideal one.

Here, we focus on improving the quality of the MOS capacitor by introducing a SiO_2 layer in between the Al_2O_3/Si interface and also investigating the effects of SiO_2 on the electrical characteristics of the newly fabricated Al/Al_2O_3/SiO_2/n-Si MOS capacitor. In order to investigate the electrical characteristics, we take *C–V* and *G*/*ω*–*V* measurements at different frequencies for Al/Al_2O_3/SiO_2/n-Si MOS samples annealed at different temperatures. The effect of the SiO_2 layer is thoroughly analyzed by using the obtained electrical parameters including the barrier height which is a good parameter in determining electron injection or current leakage.

2 Experiments

An n-type (100) wafer with thickness of 500 µm and resistivity of 2–4 Ω cm was dried using nitrogen just after undergoing the standard RCA (Radio Corporation of America) cleaning process [13]. SiO_2 films were then grown on the Si wafer by dry oxidation in the diffusion furnace at 1000 °C; afterwards, the Al_2O_3 thin film (of purity 99.99%) was deposited on the wafer by electron beam (E-beam) evaporator for 10 min, at substrate temperature of 200 °C and starting base pressure of 4.8×10^{-4} Pa. The thicknesses of SiO_2 and Al_2O_3 films measured by Angstrom Sun Spectroscopic reflectometer were 20 nm and 140 nm, respectively. The wafer was then divided into 4 samples; 1 was left as-deposited; 3 were annealed separately at temperatures of 250 °C, 450 °C, and 750 °C in an N_2 ambient for 30 min with each sample annealed at 1 temperature value. A shadow mask with circular dots of diameter 1.5 mm was placed on the Al_2O_3/SiO_2/n-Si samples, and the front aluminum contacts were deposited at 200 W by RF magnetron sputtering. The whole back contact was deposited without the shadow mask. The entire fabrication process was performed in the Class-100 cleanroom laboratories in Centre for Nuclear Radiation Detector Applications and Research Center, Bolu Abant Izzet Baysal University. DC electrodes were connected to the HIOKI 3250 LCR meter from which the *C–V* and *G*/*ω*–*V* measurements of the MOS capacitors were obtained. This was done in the voltage range of − 10 V to 10 V and in the frequency range of 100 kHz to 1 MHz. In order to eliminate the series resistance (R_s) from the obtained measurements, corrections were done on both capacitance and conductance values. The first step in correction was to obtain R_s values from Eq. 1 using the measured conductance (G_m) and capacitance (C_m) values in strong accumulation [13]

$$R_s = \frac{G_m}{G_m^2 + (wC_m)^2}, \tag{1}$$

where w is the angular frequency. Then, by using the R_s values we obtained the corrected capacitance (C_c) and conductance (G_c/w) as shown in Eqs. 2 and 3 [14, 15].

$$C_c = \frac{\left[(G_m)^2 + (wC_m)^2\right]C_m}{a^2 + (wC_m)^2}, \tag{2}$$

$$G_c = \frac{\left[(G_m)^2 + (wC_m)^2\right]a}{a^2 + (wC_m)^2}, \tag{3}$$

where $a = (G_m) - \left[(G_m)^2 + (wG_m)^2\right]R_s$.

The border trap charges density (N_{bt}) is used to estimate the oxide quality and it was calculated from Eq. 4 [16, 17].

$$N_{bt} = \frac{C_{ox}(\Delta V_{fb,hys})}{qA}, \tag{4}$$

where $\Delta V_{fb,hys}$ is the flat-band voltage shift obtained from the forward–backward *C–V* hysteresis. Its values at different annealing temperatures are shown in Table 1. The oxide trap charges density (N_{ox}) was calculated from Eq. 5 [18, 19].

$$N_{ox} = \frac{C_{ox}(\Phi_{ms} - V_{fb})}{qA}, \tag{5}$$

where q is the charge of an electron, A is the area of the capacitor plate (front contact), and C_{ox} is the effective capacitance of the oxides. The values of C_{ox} were obtained from the strong accumulation region in the *C–V* curve.

The interface-trap charges density (N_{it}) values were calculated from Eq. 6 [4, 20, 21].

$$N_{it} = \frac{2}{qA}\frac{G_{c,max}/w}{\left[(G_{c,max}/wC_{ox})^2 + (1 - C_c/C_{ox})^2\right]}, \tag{6}$$

where $G_{c,max}/w$ is the peak value of the corrected conductance and C_c is the corresponding corrected capacitance to $G_{c,max}/w$.

The built-in voltage or diffusion potential (V_D), the energy difference between the bulk Fermi level and conduction band edge (E_F), and barrier height (Φ_B) were attained by the aid of the linear regions of the $1/C^2$–V graph that will be explained in the Results and discussion section. Best fits for the linear regions were done using OriginLab program from which the slopes and the intercepts were obtained. The relation between C_c and V is given in Eqs. 7 and 8 [4, 15, 22].

Table 1 Electrical parameters for the Al/Al_2O_3/SiO_2/n-Si MOS capacitor with Al_2O_3/SiO_2/n-Si films annealed at different temperatures and those left as-deposited obtained at 1 MHz

T (°C)	ΔV_{fb} (V)	N_{bt} ($\times 10^{10}$ cm^{-2})	V_{fb} (V)	N_{ox} ($\times 10^{11}$ cm^{-2})	$G_{c,max}$ ($\times 10^{-11}$ F)	C_c ($\times 10^{-10}$ F)	N_{it} ($\times 10^{11}$ eV^{-1} cm^{-2})	V_D (V)	E_F (eV)	N_D ($\times 10^{13}$ cm^{-3})	$\Delta\phi_B$ (eV)	ϕ_B (eV)	R_s (Ω)
As deposited	0.18	3.11	− 1.75	2.56	5.30	3.36	3.82	− 0.16	0.363	− 2.29	3.67	3.47	28.39
250	0.013	0.19	− 1.41	1.62	0.56	2.35	0.225	− 2.03	0.436	− 0.136	3.30	4.89	146.07
450	0.009	0.14	− 0.80	0.799	0.88	2.64	0.417	− 1.36	0.428	− 0.186	3.23	4.17	54.79
750	0.077	0.44	− 2.19	1.08	0.55	1.28E	0.100	− 2.63	0.399	− 0.569	5.02	7.25	33.72

$$C_c^{-2} = \frac{2(V_0 + V)}{\varepsilon_s \varepsilon_0 q A^2 N_D}, \tag{7}$$

$$\frac{d(C_c^{-2})}{dV} = \frac{2}{\varepsilon_s \varepsilon_0 q A^2 N_D} = \text{Slope}, \tag{8}$$

where ε_s is the dielectric constant of the semiconductor, ε_0 is the permittivity of free space, A is the front contact area of the capacitor, V is the applied bias, N_D is the donor concentration, and V_0 is where the lines intercept with the voltage axis is given in Eq. 9 [23, 24].

$$V_0 = V_D - \frac{k_B T}{q}, \tag{9}$$

where T is the room temperature and $k_B$is the Boltzmann constant. Equation 10 was used to obtain the barrier height (Φ_B) [22]

$$\Phi_{B(C-V)} = V_D + E_F - \Delta\Phi_B, \tag{10}$$

where E_F is the energy difference between the bulk Fermi level and conduction band and is obtained from Eq. 11.

$$E_F = \frac{k_B T}{q} \ln\left(\frac{N_c}{N_D}\right). \tag{11}$$

$N_c$is the effective density of traps in Si conduction band given by Eq. 12 [22].

$$N_c = 2\left[\frac{2\pi m_e^* m_0 k_B T}{h^2}\right]^{\frac{3}{2}}. \tag{12}$$

m_0 is the rest mass of the electron, $m_e^* = 0.55 m_0$ is the effective mass of the electron, and h is the Planck's constant. The image barrier lowering is $\Delta\Phi_B$and was calculated from Eq. 13 [4].

$$\Delta\Phi_B = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right]^{\frac{1}{2}}. \tag{13}$$

E_m is the maximum electric field and was calculated from Eq. 14 [4].

$$E_m = \left[\frac{2qN_D V_0}{\varepsilon_s \varepsilon_0}\right]^{\frac{1}{2}}. \tag{14}$$

The values of V_D, E_F, N_D, $\Delta\Phi_B$, and Φ_B are listed in Table 1.

The effective capacitance for low frequencies (C_{LF}) is obtained from Eq. 15 [25].

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{\left(C_{sc} + \left(C_{it}/(1 + w^2\tau^2)\right)\right)}, \tag{15}$$

where w ($w = 2\pi f$) is the angular frequency, $C_{it}$is the excess capacitance due to interface traps, $C_{sc}$is the capacitance in the semiconductor, and τ is the life-time of the interface traps and is equal to $C_{it}R_s$. The effective capacitance for high frequencies (C_{HF}) is obtained from Eq. 16 [26, 27]. As shown in Fig. 1 C_{it} disappears in a high frequency limit.

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}}. \tag{16}$$

3 Results and discussion

C–V measurements reveal reliable information about the oxide layer and the oxide–semiconductor interface in the MOS structure [25]. With the deposition of Al contact on the front and backside, the MOS structure is complete and these measurements can be done. Apart from the metal–semiconductor work difference (Φ_{ms}), the MOS capacitor is affected by electrical charges in the oxide and traps at the interface. These charges are distributed as shown in Fig. 2: surface charges (Q_S) depend on the band bending due to applied bias and doping; interface-trapped charges (Q_{it}) are charges that fill the empty traps at the interface [20, 25], the filling and emptying of traps enables the measurement of interface state density (N_{it}) using the *C–V* and *G*/*ω*–*V* measurements as will be discussed later; mobile ionic charges are the metal ions that escape into the oxide at high bias and at high temperatures; oxide-trapped charges are charges captured by the traps located inside the oxide layers, these traps can be eliminated by low-temperature annealing; fixed oxide charges are well established within the oxide layers about 3 nm from the oxide–semiconductor interface and cannot be eliminated or reduced even when large potentials are applied [20, 25, 28]. The effective oxide charge (Q_{eff}) is the sum of Q_f, Q_{ot}, and Q_m[28].

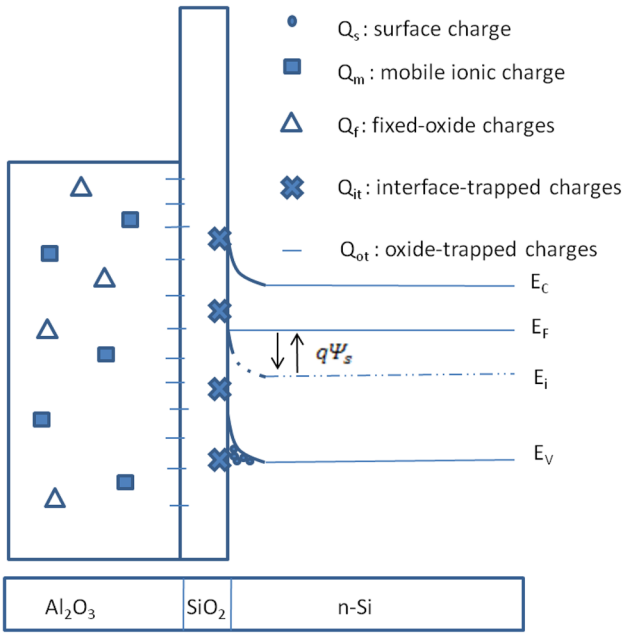

Fig. 2 Distribution of charges in the Al_2O_3/SiO_2/n-Si multilayer

The *C–V* and *G*/*ω*–*V* curves obtained from the Al/Al_2O_3/SiO_2/n-Si MOS capacitors annealed at temperatures 250 °C, 450 °C and 750 °C for high frequency (1 MHz) are shown in Fig. 3a, b. The distortions and shifts in the *C–V* and *G*/*ω*–*V* stem from the interface states, border traps, dielectric constant of the interfacial layer, and series resistance (R_s) which

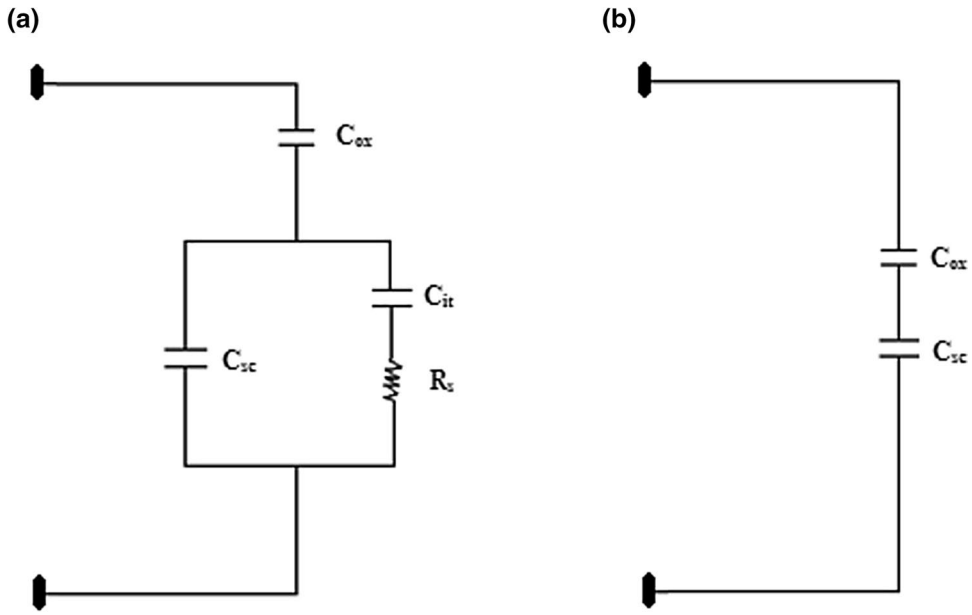

Fig. 1 Effective capacitance of the circuit in **a** low- and **b** high-frequency limits

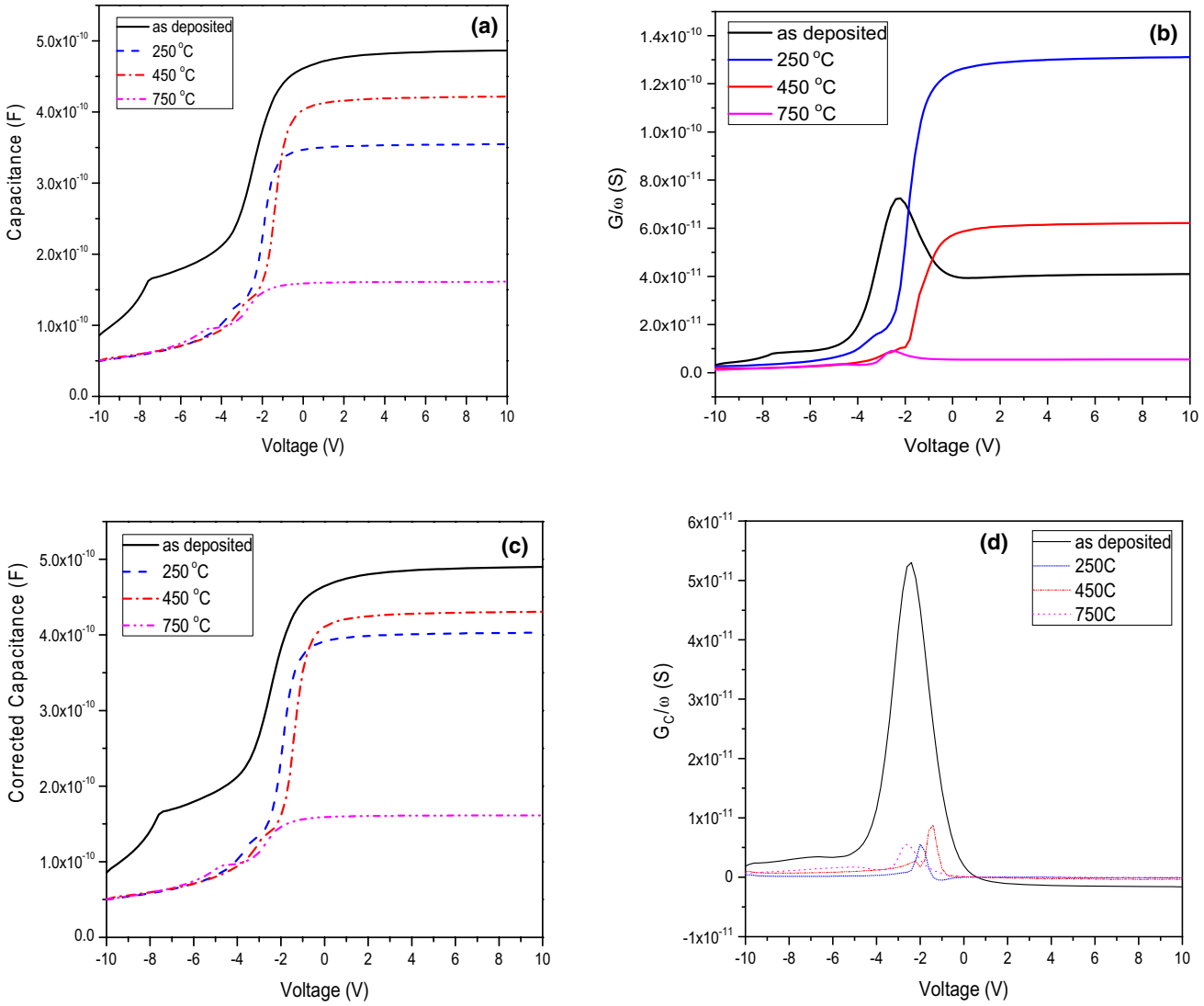

Fig. 3 Variations in **a** the measured capacitance (C), **b** measured conductance (G/ω), **c** the corrected capacitance (C_c), and **d** corrected conductance (G_c/w) of the Al/Al_2O_3/SiO_2/n-Si MOS capacitor with Al_2O_3/SiO_2/n-Si films annealed at different temperatures and those left as-deposited taken at 1 MHz

occurs between the contacts and the substrate. Therefore much attention should be paid to these parameters in order to improve the performance of microelectronic and opto-electronic devices [28].

The oxidation of Si leads to growth of an oxide that has very few fixed oxide charges and less than 10^{10} interface states eV^{-1} cm^{-2}. A significant amount of such interface states (especially those that are as a result of Si dangling bonds) are passivated by annealing at temperatures around 400 °C. Passivation does not ultimately eliminate the interfacial defects as they can emerge again after ionizing irradiation or energetic electron injection occurs across the SiO_2/Si interface [29]. As shown in Table 1, the effective oxide trap density (N_{ox}) and interface traps density (N_{it}) decreased for samples annealed at temperatures 250 °C and 450 °C. The sample annealed at 450 °C is seen to even possess the lowest border trap density (0.44×10^{10} cm^{-2}). A low trap density signifies low electron injection or current leakage which is a significant problem in MOS field effect transistors. At high annealing temperature in an inert ambient both electron and hole traps are generated. It also results in the generation of a low field self-healing breakdown [29]. Hickmott [29] improved the speculation that a decrease of SiO_2 at the SiO_2/Si interface may occur due to the reaction:

$$Si + SiO_2 \rightarrow 2SiO \uparrow, \tag{17}$$

where the SiO is a volatile gas presumed to move away from the interface leaving behind a deficiency in oxygen. Evidence given by a number of papers showed that SiO can

diffuse through the oxide network and the activation energy required for the process is in the range of 4.2–4.4 eV. This value is close to 4.7 eV, which is the estimated value for O to diffuse through the oxide [29]. So, the oxygen deficiency defects due to the Si–O destruction [29, 30] at high temperatures (700–1060 °C) cause a reduction in the quality of the dielectric layer which drastically decreases the charge storing capability. This is the reason why the sample annealed at 750 °C had a very low accumulation region capacitance as observed in Fig. 3c. Unlike the G_c/w curves in Fig. 3d, a negligible change is observed between the C–V and C_c–V curves in Fig. 3a and c, respectively, this indicates that the effect of series resistance on capacitance is negligibly small. However, a kink is observed in the C_c–V curve of the as-deposited sample at the depletion-inversion region, this kink is as a result of the electrically active defects at the oxide–semiconductor interface and it fades as the annealing temperature increases [9]. There are shifts in the C_c–V curve for different annealing temperatures both in the accumulation region and the mid-gap. In an earlier study on the Al/Al_2O_3/Si MOS capacitor [12], it was proved that post-deposition annealing reduces the oxide traps that are as a result of nonstoichiometric and weak bonds that form after growth of the thin films. These traps are the major reason for the flat-band voltage (V_{fb}) shifts. In this study, the SiO_2 layer led to the formation of stronger bonds because it is highly stable with silicon and as a result the border traps decreased. The border trap charges density (N_{bt}) for the as-deposited MOS capacitor is 3.11×10^{10} cm^{-2} which is about 10 times lower than that (7.47×10^{11} cm^{-2}) in the previous study [12].

In Fig. 3a, it is observed that annealing at 250 °C caused the flat-band voltage (V_{fb}) to shift to the right. Again, for 450 °C, the V_{fb} extended farther to the right, closer to the ideal V_{fb} (− 0.27 V). These shifts were as a result of the decrease in the effective oxide charge density (N_{ox}) which comprises of border trap density (N_{bt}) as shown in Table 1. An increase in annealing temperature leads to the formation of bonds; hence, the trap densities are reduced; the nitrogen used in the annealing process may also reduce these traps when the dangling bonds are chemically active [31–33]. At 750 °C, the V_{fb}shifted to the left because the bonds become weak or broken at very high temperatures leaving more traps in the oxides and at the Al_2O_3/SiO_2 and SiO_2/Si interfaces. The as-deposited sample had the highest capacitance in the accumulation region, this may be due to the interface traps that form layers in the SiO_2/n-Si and Al_2O_3/SiO_2 surface which cause an extra capacitance (C_{it}) that increases the effective capacitance. Annealing improves the surfaces by eliminating or reducing the interface traps density (N_{it}), this is why at 250 °C a significant decrease in the capacitance occurred in the accumulation region [8]. For the 450 °C annealed sample, an improvement of the dielectric constant occurred since farther annealing enables atoms to settle in their lattices [32], this sample had the lowest flat-band shift as shown in Fig. 4 and Table 1. This is the reason why its border trap density was the lowest compared to the other samples. At high annealing temperatures possible parasitic $SiO_x/AlSiO_x$ layers are formed, these layers degrade the effective dielectric constant and increase the total thickness of the oxides which results into a huge decline in the capacitance [12]. This explains why the accumulation region capacitance at 750 °C was very low compared to others.

The conductance is essential in investigating the interface quality of MOS structure, conductance is a result of interactions between interface traps and majority carrier densities in the Si [12]. Interface-trap density (N_{it}) is calculated by using either the conductance method [34] or the high-low frequency capacitance method [25]. In this study, the conductance method by Goetzberger and Nicollian [15] was used since measurements were taken for only one frequency (1 MHz). According to Fig. 3d, the peaks of the corrected conductance curves are highest for the as-deposited sample, this is because it had the highest interface-trap density (N_{it}) value, and the lowest was with the sample annealed at 750 °C as shown in Table 1. We noticed that after annealing, the N_{it} values decreased from ~ 10^{11} to ~ 10^{10} eV^{-1} cm^{-2}. These N_{it}values of the annealed samples in this study (double gate oxide layer Al_2O_3/SiO_2 MOS capacitor) are 10 times lower than those in the previous study (single oxide layer Al_2O_3 MOS capacitor) [12]; therefore, the stronger bond between SiO_2 and Si results in a decrease in the traps as the atoms settle in their lattices after annealing.

In Fig. 5b there is an intersection of the lines because of the capacitance variations in the depletion region. The N_{it} values in Table 1 only represent the total density of both the donor and acceptor interface traps. This means that these

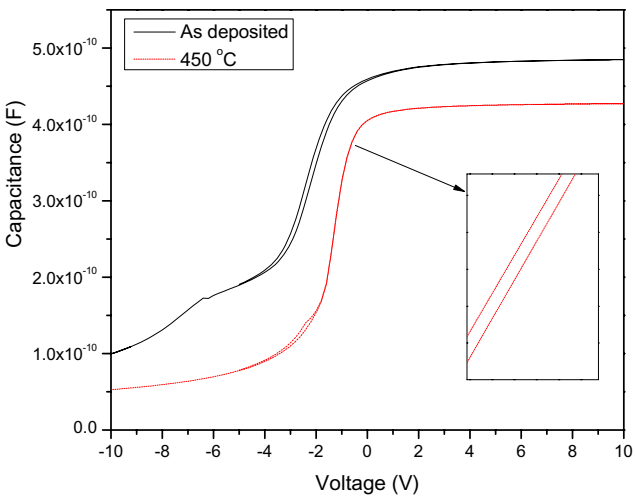

Fig. 4 The hysteresis of the capacitance of the Al/Al_2O_3/SiO_2/n-Si MOS capacitor with Al_2O_3/SiO_2/n-Si films annealed at 450 °C and those left as-deposited taken at 1 MHz

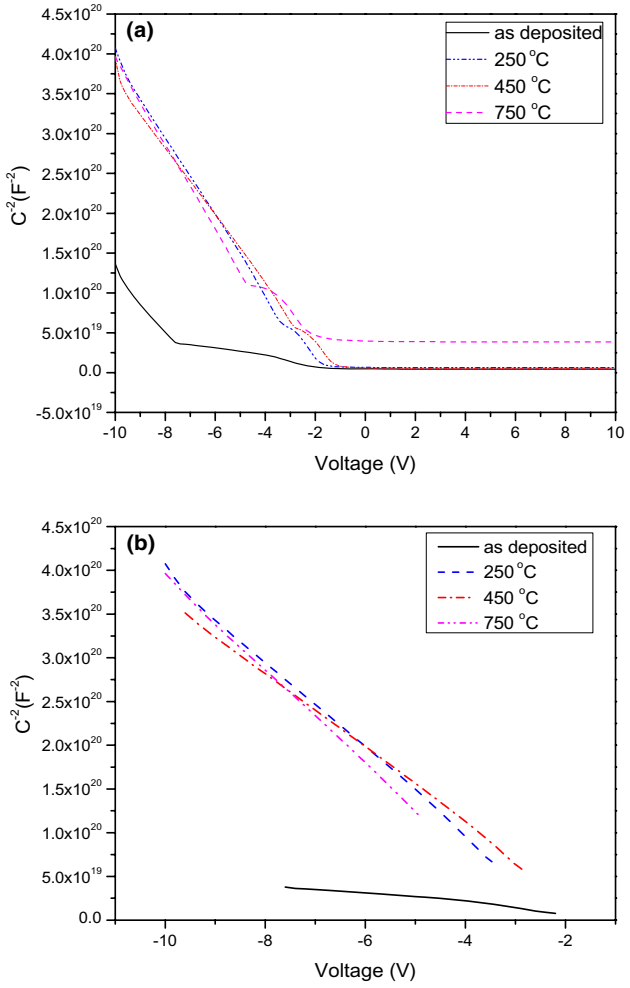

Fig. 5 **a** C^{-2}–V plots of the Al/Al_2O_3/SiO_2/n-Si MOS capacitor with Al_2O_3/SiO_2/n-Si films annealed at different temperatures and those left as-deposited taken at 1 MHz. **b** C^{-2}–V plots of linear region of the Al/Al_2O_3/SiO_2/n-Si MOS capacitor with Al_2O_3/SiO_2/n-Si films annealed at different temperatures and those left as-deposited taken at 1 MHz

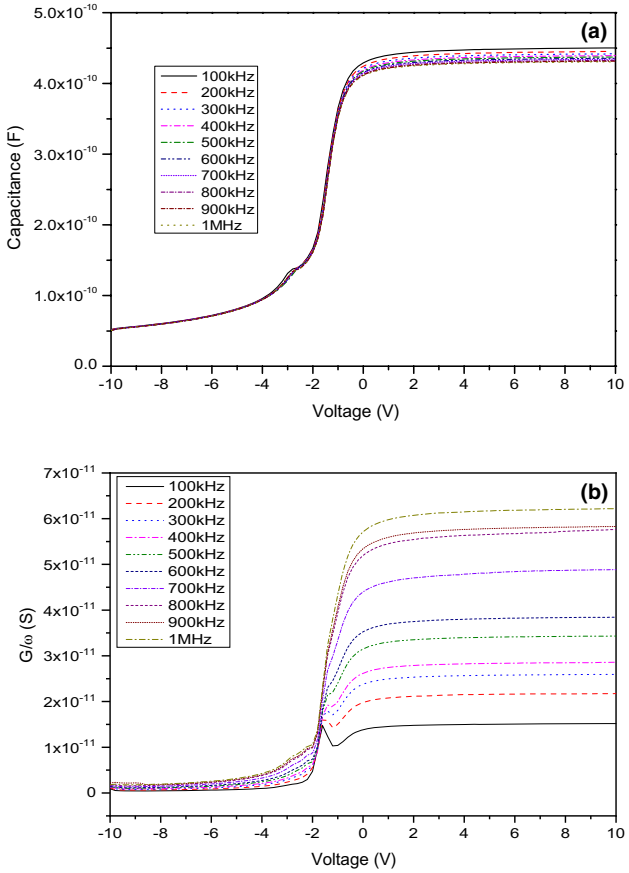

Fig. 6 **a** Varying capacitance (C) of the 450 °C annealed Al/Al_2O_3/SiO_2/n-Si MOS capacitor measured at different frequencies. **b** Varying conductance (G/ω) of the 450 °C annealed Al/Al_2O_3/SiO_2/n-Si MOS capacitor measured at different frequencies

values cannot be used to determine the polarity of the interface traps separately. On the other hand, the barrier height (Φ_B) can give us a hint on the polarity of the interface traps. For the n-type semiconductor, while the negatively charged interface traps (acceptor-like) increase the barrier height, the positively charged interface traps (donor-like) decrease the barrier height. Therefore, the variation in Φ_B is caused by the existing and newly formed traps with a change in annealing temperature. Another cause of change in the barrier height is the internal electric field caused by the traps in the low quality oxide and interface [35]. A low barrier height results in high electron injection which means high tunneling possibility for electrons; therefore, a high barrier height reduces electron injection (leakage current). In Table 1, all barrier heights were high compared to the usual Φ_B values in the literature which range from 0.56 to 3.68 eV [22, 32, 36].

The frequency-dependent electrical characteristics of the Al/Al_2O_3/SiO_2/n-Si MOS capacitor were studied with the aid of the C–V and G/ω–V measurements as shown in Fig. 6a, b. These measurements were taken for only the 450 °C annealed MOS capacitor because of its high C_{ox} related to a high dielectric constant (ε_{ox}), and its flat-band voltage (− 0.8 V) was the closest to the ideal flat-band voltage (~ − 0.27 V) compared to the other samples. Again, correction was performed in order to eliminate series resistance. Figure 7a, b contains the corrected capacitance (C_c) and corrected conductance (G_c/w) curves, while there was almost no difference between C–V and C_c–V curves, the difference between G/ω–V and G_c/w–V was significant. This explains

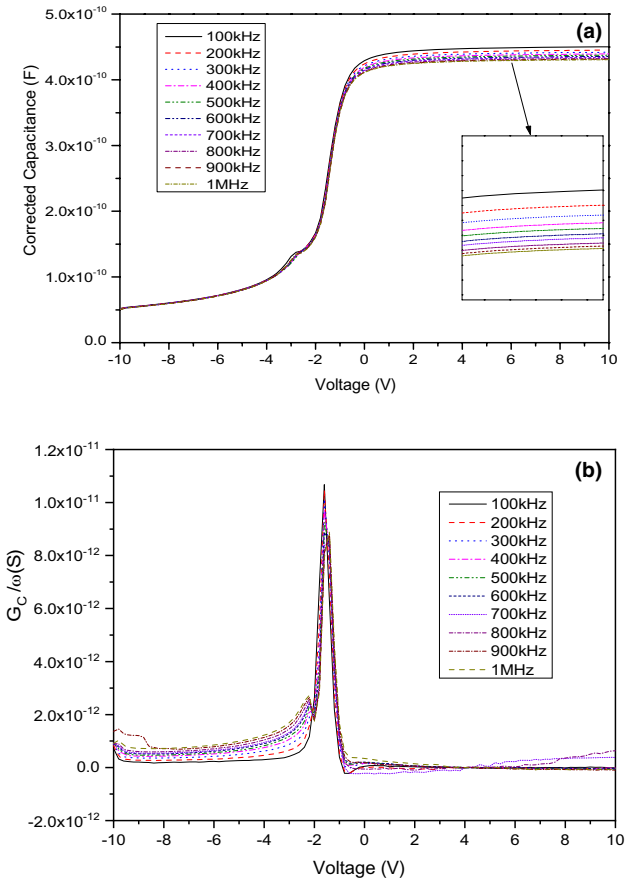

Fig. 7 **a** Varying corrected capacitance (C_c) of the 450 °C annealed Al/Al_2O_3/SiO_2/n-Si MOS capacitor at different frequencies. **b** Varying corrected conductance (G_c/w) of the 450 °C annealed Al/Al_2O_3/SiO_2/n-Si MOS capacitor at different frequencies

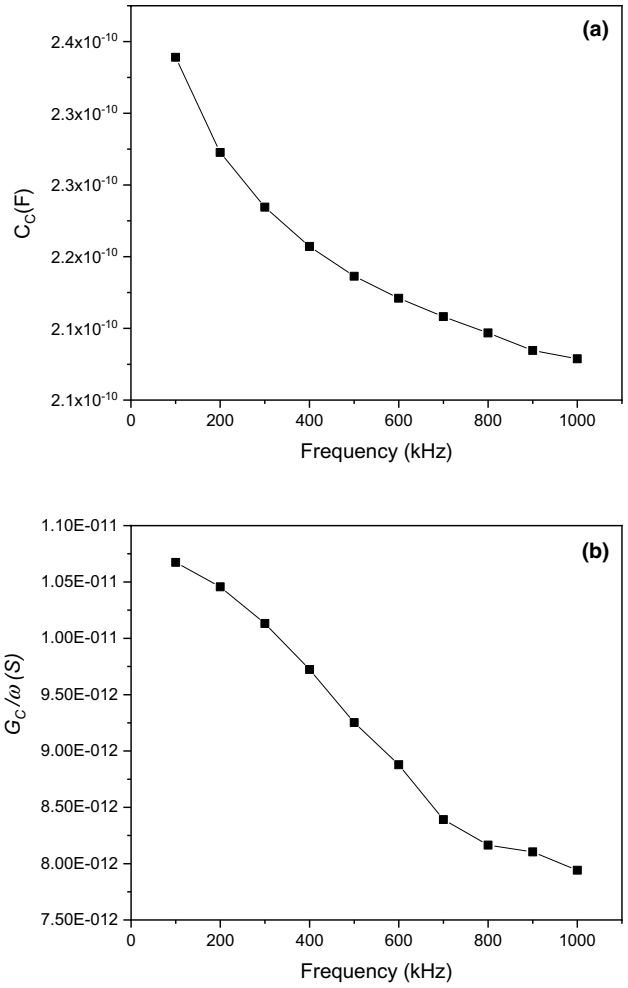

Fig. 8 Graph of **a** corrected capacitance (C_c) and **b** corrected conductance (G_c/w) with frequency for the Al/Al_2O_3/SiO_2/n-Si MOS capacitor annealed at 450 °C

that series resistance greatly affected conductance. As observed in Fig. 8a, the capacitance values decreased with increasing frequency due to time-dependent surface traps, particularly interface traps [26, 37, 38]. In Eq. 15, τ is the life-time of the interface traps and is equal to $C_{it}R_s$, values of τ in the literature are in the range (10^{-6} to 10^{-7} s) [17]. So, $w\tau$ is extremely small for low frequencies (< 500 kHz). $w^2\tau^2$ is therefore neglected in Eq. 12. That is to say, an excess capacitance C_{it} evolves as a result of the interface-trapped charges which can follow the AC signal at low frequencies. Equation 15 then becomes Eq. 16 [26]. For high frequencies (≥ 500 kHz), $w^2\tau^2$ is quite higher compared to C_{it}, meaning that the interface-trapped charges can no longer follow the AC signal.

After correction, the conductance–voltage (G_c/w–V) peaks appeared for all frequencies. This means that series resistance (R_s) had a strong influence on the conductance. As observed in Fig. 9, maximum values of R_s are obtained in the depletion region and the amplitude of the peaks decreases with an increase in frequency. This indicates

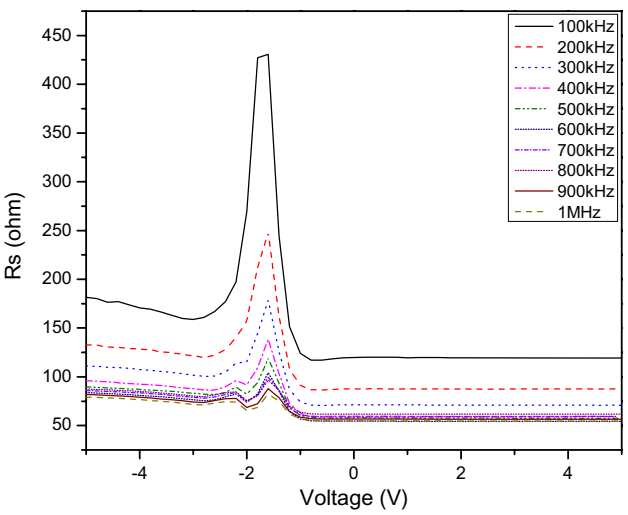

Fig. 9 R_s–V plots for the 450 °C annealed Al/Al_2O_3/SiO_2/n-Si MOS capacitor measured at different frequencies

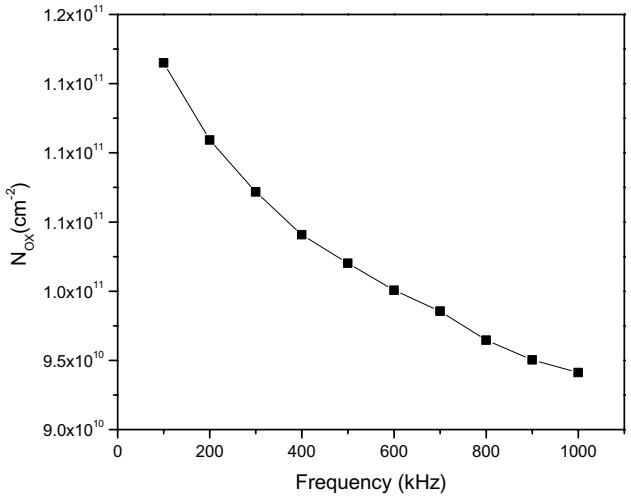

Fig. 10 Variations in the effective oxide density (N_{ox}) of the 450 °C annealed Al/Al_2O_3/SiO_2/n-Si MOS capacitor at different frequencies

that R_s depends on the frequency-dependent charges such as interface charges and oxide-trapped charges [37, 39]. From these behaviors it can be evaluated that carriers possess sufficient energy to break free from their traps found between metal and silicon in the semiconductor band gap [37]. Furthermore, there was a significant deviation of the curves for low frequencies (< 500 kHz), while for high frequencies the deviations were too small. This is also because at high frequencies the charges in the traps found at the metal/Si interface acquire sufficient energy to leave these traps [4, 37].

A rare case in this study was that the effective oxide density as shown in Fig. 10 and Table 2 decreased with increasing frequency. A possible reason for this behavior is that the border trap charges were also affected by frequency. In the oxide, border traps are located near the interface, and carriers in the semiconductor can be captured in these traps after tunneling. The frequency affects these charges since an increase in the time constant for tunneling exponentially increases with the distance between interface and border traps [40].

4 Conclusion

The Al/Al_2O_3/SiO_2/n-Si MOS capacitor was fabricated and the effect of the SiO_2 on the electrical characteristics was analyzed. *C–V* and *G*/*ω*–*V* curves obtained from the Al/Al_2O_3/SiO_2/n-Si MOS capacitors annealed at temperatures 250 °C, 450 °C, and 750 °C for high frequency (1 MHz). These curves distorted and shifted from the ideal ones due to presence of interface states density (N_{it}), border trap density (N_{bt}), effective oxide charge density (N_{ox}), and series resistance (R_s). The closest flat-band voltage (V_{fb}) to the ideal one was with the sample annealed at 450 °C, this sample also had a high capacitance (C_{ox}) which was related to its high dielectric constant (ε_{ox}). Corrections were made for the *C–V* and *G*/*ω*–*V* measurements, and it was noticed that the effect of *R* on capacitance was negligible but that on conductance was significant. N_{ox} and N_{it} values were very low (~ 10^9 eV^{-1} cm^{-2} and ~ 10^{10} eV^{-1} cm^{-2}, respectively) indicating reduced lattice mismatches due to the highly stable SiO_2.

A rare case in this study was that the effective oxide density decreased with increasing frequency. A possible reason for this behavior was that the border trap charges were also affected by frequency. So, in general, the SiO_2 layer played a major role in improving the quality of both the oxide layers and the interfaces.

Table 2 Electrical parameters for the 450 °C annealed Al/Al_2O_3/SiO_2/n-Si MOS capacitor obtained at different frequencies

Frequency (kHz)	V_{fb} (V)	N_{ox} ($\times 10^{11}$ cm^{-2})	$G_{c,max}$ ($\times 10^{-11}$ F)	C_c ($\times 10^{-10}$ F)	N_{it} ($\times 10^{10}$ eV^{-1} cm^{-2})
100	−1.00	1.17	1.07	2.34	3.26
200	−9.77	1.11	1.05	2.27	3.09
300	−0.96	1.07	1.01	2.23	2.93
400	−0.94	1.04	0.97	2.21	2.77
500	−0.93	1.02	0.92	2.19	2.61
600	−0.92	1.00	0.88	2.17	2.49
700	−0.91	0.99	0.86	2.67	4.12
800	−0.92	0.97	0.87	2.66	4.13
900	−0.895	0.95	0.89	2.65	4.18
1000	−0.890	0.94	0.88	2.64	4.18

Acknowledgements This work is supported by the Presidency of Turkey, Presidency of Strategy and Budget under Contract Number 2016K12-2834.

Data availability We confirm that the data supporting the findings of this study are available within the article and its supplementary material.Code availability Not applicable.

Compliance with ethical standards

Conflicts of interest We declare that there is no conflict of interest.

References

1. L. Christophe, *Making Silicon Valley: Innovation and the Growth of High Tech, 1930–1970* (Chemical Heritage Foundation, Philadelphia, 2006), pp. 253–256
2. S.S. Cetin, H.I. Efkere, T. Sertel, A. Tataroglu, S. Ozcelik, Silicon **100**, 1–5 (2020). https://doi.org/10.1007/s12633-020-00383-8
3. A. Kahraman, U. Gurer, R. Lok, S. Kaya, E. Yilmaz, J. Mater. Sci. Mater. Electron. **29**(20), 17473–17482 (2018)
4. A. Kahraman, E. Yilmaz, S. Kaya, A. Aktag, J. Mater. Sci. Mater. Electron. **26**(11), 8277–8284 (2015)
5. M.I. Idris, N.G. Wright, A.B. Horsfall, Mater. Sci. Forum **924**, 486–489 (2018)
6. Y. Wang, R. Jia, C. Li, Y. Zhang, AIP Adv. **5**(8), 3–8 (2015)
7. A. Bouazra, S.A. Nasrallah, M. Said, A. Poncet, Res. Lett. Phys. (2008). https://doi.org/10.1155/2008/286546
8. N.M. Terlinden, G. Dingemans, V. Vandalon, R.H.E.C. Bosch, W.M.M. Kessels, J. Appl. Phys. **115**(3), 033708 (2014)
9. R. Khosla, E.G. Rolseth, P. Kumar, S.S. Vadakupudhupalayam, S.K. Sharma, J. Schulze, IEEE Trans. Device Mater. Reliab. **17**(1), 80–89 (2017)
10. S. Kitai, O. Maida, T. Kanashima, M. Okuyama, Jpn. J. Appl. Phys. **1**(42), 247–253 (2003)
11. J. Robertson, Rep. Prog. Phys. **69**, 327 (2006)
12. S. Kaya, E. Budak, E. Yilmaz, Turk. J. Phys. **42**(4), 470–477 (2018)
13. R. Khosla, S.K. Sharma, J. Vac. Sci. Technol. B **36**, 012201 (2018)
14. S. Demirezen, I. Orak, Y. Azizian-Kalandaragh, S. Altindal, J. Mater. Sci. Mater. Electron. **28**, 12967–12976 (2017)
15. A. Tataroğlu, G.G. Güven, S. Yilmaz, A. Büyükbas, Gazi Univ. J. Sci. **27**(3), 909–915 (2014)
16. X.Y. Liu, Y.Y. Wang, Z.Y. Peng, C.Z. Li, J. Wu, Y. Bai, Y.D. Tang, K.A. Liu, H.J. Shen, Chin. Phys. B **24**, 087304 (2015).
17. I. Hussain, M.Y. Soomro, N. Bano, O. Nur, M. Willander, J. Appl. Phys. **112**, 064506–064507 (2012)
18. A. Kahraman, H. Karacali, E. Yilmaz, J. Alloys Compd. **825**, 154171 (2020)
19. R. Khosla, P. Kumar, S.K. Sharma, IEEE Trans. Device Mater. Reliab. **15**(4), 610–616 (2015)
20. G. Brammertz, H.C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W.E. Wang, M. Caymax, M. Meuris, M. Heyns, ECS Trans. **16**, 507 (2008)
21. P. Zhao et al., 2D Mater. **5**, 3 (2018)
22. W. Bachir Bouiadjra, A. Saidane, A. Mostefa, M. Henini, M. Shafi, Superlattices Microstruct. **71**, 225–237 (2014)
23. S. Kaya, E. Yilmaz, IEEE Trans. Electron Devices **62**(3), 980–987 (2015)
24. A. Kahraman, E. Yilmaz, A. Aktag, S. Kaya, IEEE Trans. Nucl. Sci. **63**(2), 1284–1293 (2016)
25. M. Pawlik et al., Energy Procedia **60**(C), 85–89 (2014)
26. S. Kaya, R. Lok, A. Aktag, J. Seidel, E. Yilmaz, J. Alloys Compd. **583**, 476–480 (2014)
27. J. Robertson, R.M. Wallace, Mater. Sci. Eng. R **88**, 1–41 (2015)
28. S.M. Sze, *Semiconductor Devices Physics and Technology* (Wiley, Hoboken, 1985)
29. R.A.B. Devine, J. Phys. III France **6**, 1569–1594 (1996)
30. N. Balaji, C. Park, S. Chung, M. Ju, J. Raja, J. Yi, J. Nanosci. Nanotechnol. **16**, 4783 (2016)
31. W. Von Ammon, R. Hölzl, J. Virbulis, E. Dornberger, R. Schmolke, D. Gräf, J. Cryst. Growth **226**(1), 19–30 (2001)
32. A. Kahraman, J. Mater. Sci. Mater. Electron. **29**(10), 7993–8001 (2018)
33. T. Hosoi et al., Mater. Sci. Forum **679–680**, 496–499 (2011)
34. W. Kern, J. Vossen, *Thin Film Processes* (Academic, New York, 1978)
35. T.P. Chen, IEEE Trans. Electron Devices **49**, 1493–1496 (2002)
36. R. Lok, S. Kaya, H. Karacali, E. Yilmaz, J. Mater. Sci. Mater. Electron. **27**(12), 13154–13160 (2016)
37. H. Xiao, S. Huang, Mater. Sci. Semicond. Process. **13**, 395 (2010)
38. H.M. Baran, A. Tataroglu, Chin. Phys. **B22**, 047303–047304 (2013)
39. F. Parlaktürk, Ş. Altindal, A. Tataroğlu, M. Parlak, A. Agasiev, Microelectron. Eng. **85**, 81 (2008)
40. I. Dökme, Ş. Altindal, Physica B **393**(1–2), 328–335 (2007)