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Determination of frequency and voltage dependence of electrical properties of Al/(Er_2O_3/SiO_2/*n*-Si)/Al MOS capacitor

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Abstract

In this study, we investigated the effects of applied voltage and frequencies on the electrical properties of Al/(Er_2O_3(150 nm)/SiO_2(20 nm)/n-Si)/Al MOS capacitor. The e-beam deposited Er_2O_3/SiO_2 films were annealed at 650 °C in N_2 ambient and the crystal and phase identification of the films were confirmed by X-ray diffractometry. The capacitance–voltage (*C–V*) and the conductance–voltage (*G/ω–V*) measurements of the MOS capacitor were carried out for voltage frequencies from 50 kHz to 1 MHz at several steps. The parameters of doping concentration, diffusion potential, built-in potential, barrier height, Fermi energy level, the image force barrier lowering and the depletion layer width were calculated by *C–V* and *G/ω–V* data. While the depletion layer width decreased with increasing frequencies, the diffusion potential and the barrier height increased a little with small frequencies (200 kHz ≤ *f*) first, then decreased insignificantly. We also studied the frequency effects on the series resistance (R_s) and the interface state density (D_{it}) through the *C–V* and *G/ω–V* curves, and found noticeable decreases in R_s and D_{it} values with increasing frequency. The measured and calculated results reveal that both R_s and D_{it} frequency dependence have significant impacts on Er_2O_3/SiO_2/*n*-Si MOS capacitor properties. These effects are basically because of the interfacial charge behavior of thin SiO_2 layer contained in between *n*-Si and Er_2O_3.

1 Introduction

For new generation highly advanced complementary metal oxide semiconductor (CMOS) technology, the improved electronic devices with well-known features are required. The metal–oxide–semiconductor (MOS) capacitors are used in many different application areas of optoelectronics, microelectronics, thermophotovoltaic and biomedical applications since they have outstanding optical and electrical properties [1]. The early MOS capacitors had SiO_2 as the oxide layer between metal and semiconductor. Because of the excessive gate leakage current associated with the SiO_2 layer which leads an increase in static power consumption and error in logic devices, of late, research is on finding better high permittivity (high-k) alternatives to the SiO_2 layer [2]. In the past decade, for the highly advanced complementary metal oxide semiconductor (CMOS) technology, many high-k materials such as Pr_2O_3, Al_2O_3, Er_2O_3, Sr_2O_3, HfO_2, ZrO_2, La_2O_3, Fe_2O_4, Dy_2O_3, and TiO_2 have been proposed as possible alternatives to SiO_2 [3–6]. However, Er_2O_3 is one of the promising high-k materials that has pluses over SiO_2 because it owns a higher dielectric constant (10–14), a wider bandgap (~ 5.4 eV), a relatively large conduction band offset (~ 3.5 eV), and lower gate leakage current [7]. Despite that, there are still some issues concerning the degradation of the metal–oxide–semiconductor (MOS) device reliability, this is because of the difficulty in finding a high-k material that has a perfect interface match with Si as compared to SiO_2. For this reason, an extremely thin SiO_2 layer is deposited onto the Si before the high-k layer reducing the lattice mismatch. Besides, the SiO_2 interfacial layer could not only reduce the lattice match but it would also increase the thermodynamic stability between high-k materials and Si [2]. A high thermodynamic stability reduces the formation of silicides and rugged surfaces [8].

Among many other deposition techniques to fabricate Er_2O_3 thin films, we had used the electron beam (e-beam) vapor deposition technique. The e-beam evaporation is a physical vapor deposition (PVD) technique whereby an intense electron beam is generated from a filament and

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steered via electric and magnetic fields to strike the source material and vaporize it within a vacuum environment [9, 10]. This technique has some key advantages over the other techniques; it has high and controllable rate of deposition, high density, and homogeneity of the prepared thin films, etc. The e-beam PVD technique has attracted much more attention because such technique has control on porosity, film structure, stoichiometry film growth rate. All these parameters may be controlled by varying the deposition conditions. This method has also been used to deposit high-k films because of controllable interface growth and low contamination. While in many other techniques an oxidation interface layer occurs on Si substrate due to oxygen ambient at high annealing temperatures, it does not happen in the e-beam PVD technique [11].

In this work, we systematically investigated the Er_2O_3/SiO_2/*n*-Si structure deposited by e-beam PVD technique and determined the electrical characteristics for MOS capacitor such as barrier height (Φ_B), diffusion potential (V_D), donor concentration (N_D), Fermi energy level (E_F), and depletion layer width (W_D) by measured capacitance–voltage (*C*–*V*) and conductance–voltage (*G*/*ω*–*V*) data. We also studied the behavior of the interface states density (D_{it}) and the series resistance (R_s) through *C*–*V* and *G*/*ω*–*V* data for frequencies from 50 kHz to 1 MHz at room temperature.

2 Experimental details

Four samples were annealed in N_2 atmosphere at temperatures ranging from 450 to 750 °C to optimize crystallinity. All samples were analyzed by X-ray diffraction and found that the sample annealed at 650 °C illustrated a good cubic structure and may exhibit interesting electrical properties.

In order to fabricate the MOS capacitor, a 6-inch, 500 µm thick *n*-type Si wafer (100) with resistivity of 2–4 cm Ω was dried using nitrogen gas. Following the standard RCA cleaning procedure, the SiO_2 layer was grown on *n*-Si by dry oxidation at 1000 °C. The Er_2O_3 thin film was deposited on SiO_2/*n*-Si structure by e-beam evaporation under the pressure of 3×10^{-4} Torr in the growth rate of 1.5 Å/s. The thickness of SiO_2 and Er_2O_3 layers were measured using Angstrom Sun Spectroscopic reflectometer and found to be 20 nm and 150 nm, respectively. Then a portion of deposited Er_2O_3/SiO_2 film was annealed at 650 °C for 30 min under N_2 ambient with the flow rate of 1000 sccm. Metallization processes were performed to convert annealed thin films to MOS capacitors. A shadow mask with 1.5 mm circular dots was placed on the Er_2O_3/SiO_2/Si structure, with aluminum (Al) deposition at 120 W by RF magnetron sputtering. The back contact was obtained by covering the entire back surface in the same conditions with front contacts. Al contacts were used to reduce possible signal loss and to eliminate a possible potential barrier that may form between the electrode and semiconductor interface. As schematically shown in Fig. 1, the Al/(Er_2O_3/SiO_2/*n*-Si)/Al MOS capacitors were fabricated. The films' structure was characterized by Rigaku 2500PC X-ray diffraction (XRD) with the CuK_α characteristic X-ray wavelength of 1.5 Å. The 2*θ* range was between 10° and 80°. The 2*θ* step and the step acquisition time were 0.01 and 5 per second for all diffract grams.

The surface morphology of the 150 nm Er_2O_3 film was analyzed using AFM. Figure 2 shows the AFM image of the Er_2O_3 film in 3D with the size of 4 µm × 4 µm. The film is characterized by the roughness root-mean-square (R_q) which is obtained to be 1.77 nm as deposited. For the film annealed at 650 °C, the R_q is obtained to be 2.3 nm. The increase in roughness is related to the film thickness of Er_2O_3.

The electrical measurements; *C*–*V* and *G*/*ω*–*V* were performed with the Keithley 4200-SCS Parameter Analyzer for voltage raised from − 5 to 5 V at frequencies from 50 kHz to 1 MHz in a 50 step first, then at 100 kHz steps at room temperature. Finally, all of the fabrication processes and the experiments were performed in Class-100 cleanroom laboratories in Bolu Abant Izzet Baysal University Nuclear Radiation Detectors Application and Research Center, Turkey.

3 Measurements, calculations and discussions

The obtained XRD spectra of the Er_2O_3/SiO_2/n-Si were given in Fig. 3. While the as-deposited Er_2O_3/SiO_2 film shows polycrystalline structure weak spectrum peaks, the annealed sample at 650 °C for 30 min in a nitrogen environment exhibits stronger reflections peaks, in particular, the peaks at $2=\theta21.0°$, 29.5°, 35.0°, 48.9°, and 58.6° can be associated to reflections for the (211), (222), (400), (440), and (622) planes of the Er_2O_3 cubic lattice with the lattice parameter of 10.54 Å [9, 12, 13]. It is observed that the preferred orientation of the fabricated film is in the cubic phase structure with (222). The peaks were indexed by the International Centre for Diffraction Data (ICCD) card number 77–0463.

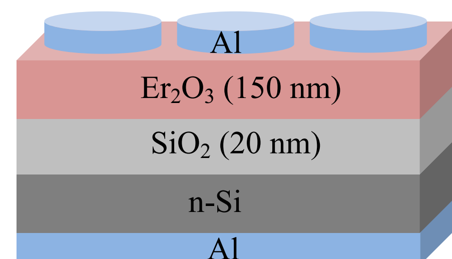

Fig. 1 Structure of Al/(Er_2O_3/SiO_2/n-Si)/Al MOS Capacitors

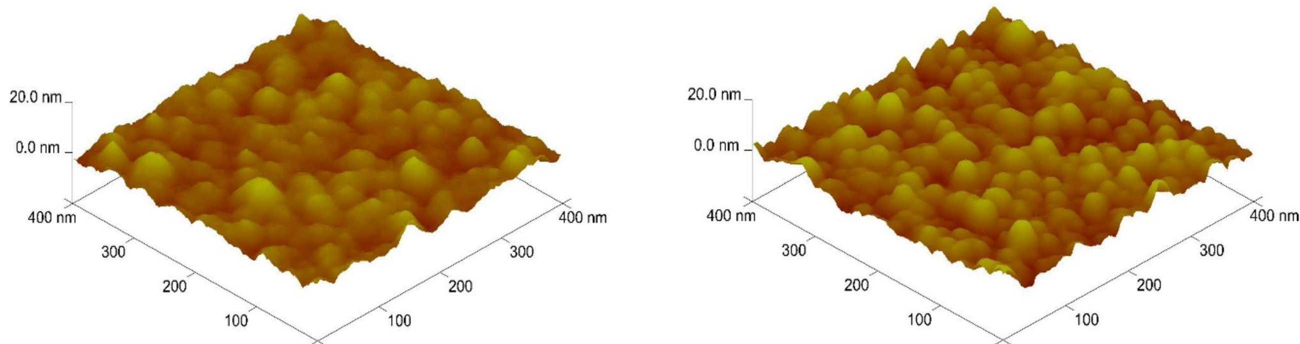

Fig. 2 AFM image of the Er_2O_3 film: as deposited (left) and annealed at 650 °C (right)

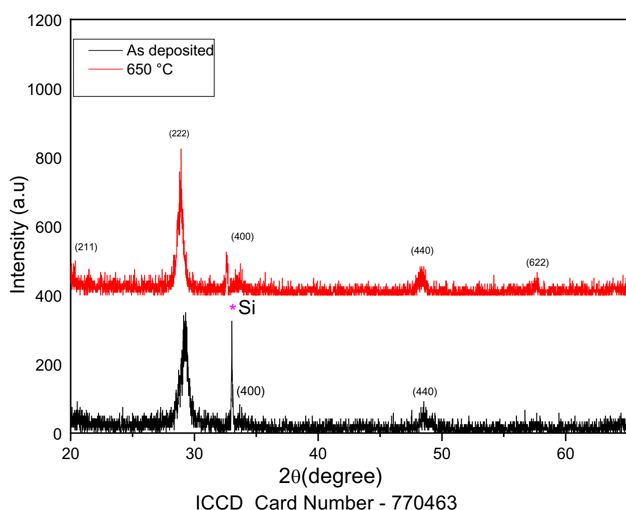

Fig. 3 XRD spectra of Er_2O_3/SiO_2 thin films on n-Si (100) substrate

In general, the capacitance of a dielectric material (C_{die}) inserted between metal electrodes is given as

$$C_{die} = \varepsilon_o \kappa_{die} \frac{A}{t_{ox}} \tag{1}$$

where ε_o is the permittivity of free space (8.85×10^{-12} F/m), κ_{die} is the dielectric constant of dielectric layer (SiO_2 (3.9)) or (Er_2O_3 (14)) used for calculation, A is the metal gate electrode area (Al (1.77×10^{-2} cm^2)) and t_{ox} is the thickness of the dielectric (SiO_2 (20 nm) or Er_2O_3 (150 nm)). Calculated capacitance of $C_{SiO2} = 3.05 \times 10^{-9}$ F and $C_{Er_2O_3} = 1.46 \times 10^{-9}$ F.

In Fig. 4a, the total oxide capacitance of the sample equivalent to the series of the capacitance of the SiO_2 layer and the Er_2O_3 layer is represented and calculated by the following equation [14–16].

$$C_{ox} = \frac{C_{SiO_2} C_{Er_2O_3}}{C_{SiO_2} + C_{Er_2O_3}} \tag{2}$$

where $CSiO_2$ and CEr_2O_3 are the capacitances of the SiO_2 and Er_2O_3 layers, respectively. By substituting calculated $CSiO_2$ and CEr_2O_3 values into Eq. (2), the total oxide capacitance (C_{ox}) was found to be 9.89×10^{-10} F.

Figure 4b, c show C–V and G/ω–V data accomplished over the frequency range of 50 kHz and 1 MHz. As shown in Fig. 4b, the capacitance tends to decrease with increasing frequency. However, as the frequency is raised, the capacitance reduces to a limit and stays there because the defect charges have no enough time to rearrange and response to the applied voltage.

As shown in Fig. 4c, the existence of R_s causes the measured conductance (G_m/ω) to increase with increasing frequency while the admittance peaks reduce relatively as the frequency increases, however, when G_m is corrected (G_C/ω), it decreases with frequency (See Fig. 7). This indicates that at low frequencies, flow of charge through the interface is possible and the characteristics depend on the relaxation time and the AC signal frequency [17].

At a given frequency, most of the errors in the C–V and G/ω–V features are due to the series resistance (R_s) in the strong accumulation region and a portion of the depletion region.

Using Nicollian and Goetzberger calculation approach, the R_s of MOS devices may be deducted from the strong accumulation region measurements of the capacitance (C_{ma}) and the conductance (G_{ma}) at high frequencies (≥ 200 kHz) [18, 19]. For the capacitor biased into strong accumulation region, the frequency-dependent complex impedance of MOS device can be described as

$$Z_{ma} = R_s + iX = \frac{G_{ma}}{(G_{ma})^2 + (\omega C_{ma})^2} - i\frac{\omega C_{ma}}{(G_{ma})^2 + (\omega C_{+})^2} \tag{3}$$

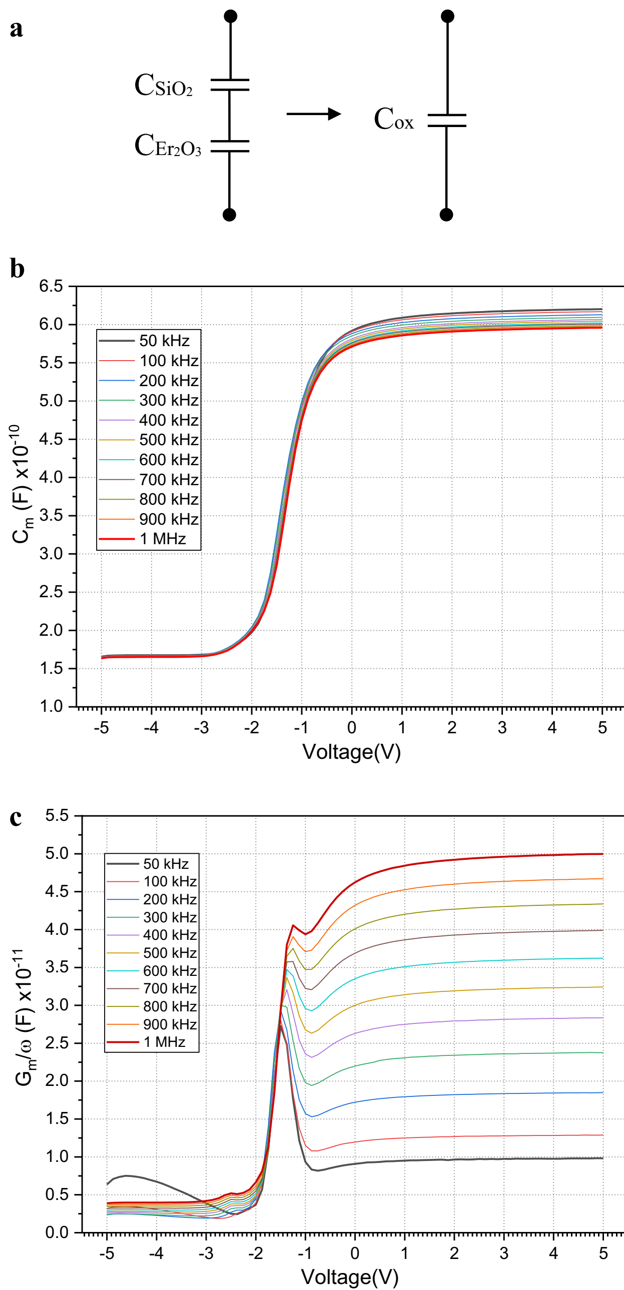

Fig. 4 **a** Equivalent capacitance to the series of the capacitances SiO_2 layer and Er_2O_3 layer. **b** Measured capacitance (C_m) of Al/(Er_2O_3/SiO_2/n-Si)/Al MOS capacitor for various frequency ranges from 50 kHz to 1 MHz. **c** Measured conductance (G_m/ω) of Al/(Er_2O_3/SiO_2/n-Si)/Al MOS capacitor for various frequencies ranges from 50 kHz to 1 MHz

where ω = 2πf is the voltage angular frequency. Using the real part of Eq. (3), the R_s values can be found for the given frequencies [20].

$$R_S = \frac{G_{ma}}{(G_{ma})^2 + (\omega C_{ma})^2} \quad (4)$$

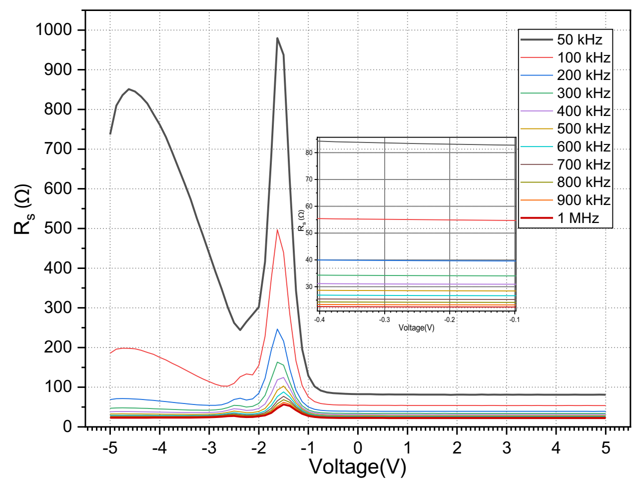

Fig. 5 Series resistance curves for Er_2O_3/SiO_2/n-Si MOS capacitor for various frequencies ranges from 50 kHz to 1 MHz

The calculated R_s values versus voltage frequency are calculated and plotted in Fig. 5 for Al/(Er_2O_3/SiO_2/n-Si)/Al MOS capacitor. The R_s values are varying in range of 850–32 Ω for frequencies of 50–600 kHz, and 29–25 Ω for frequencies of 700–1000 kHz as voltage increases from − 5 V to about − 2.25 V. The R_s get their peak values at around − 1.5 V as voltage increases from − 2.25 to − 0.375 V. Later, as shown in Fig. 5 (emplacement), when voltage increased from − 0.375 to 5 V the peaks disappear and R_s decrease, become stable and remained fixed in 84–27 Ω range for frequencies of 50–600 kHz, and 25–23 Ω range for frequencies of 700–1000 kHz [21]. The reason for this to happen is the displacement and rearrangement of the frequency-dependent charges such as fixed oxide charge, oxide trapped charge, mobile oxide charge, and interface trapped charge. The *C–V* and *G*/*ω–V* were corrected due to the fact that R_s is voltage dependent at the strong accumulation region as seen in R_s–*V* plot (Fig. 5). In addition, the interface trap charges may have enough energy to jump through traps placed between the metal (rear contact) and the semiconductor interface in the Si bandgap [17, 18].

The *C–V* and *G*/*ω–V* data were corrected by the use of strong accumulation region R_s values [21]. The corrected capacitance (C_C) and corrected conductance (G_C) are calculated from the equations [22].

$$C_C = \left(\frac{{G_m}^2 + (\omega C_m)^2}{a^2 + (\omega C_m)^2} \right) C_m \quad (5)$$

$$G_C = \left(\frac{{G_m}^2 + (\omega C_m)^2}{a^2 + (\omega C_m)^2} \right) a \quad (6)$$

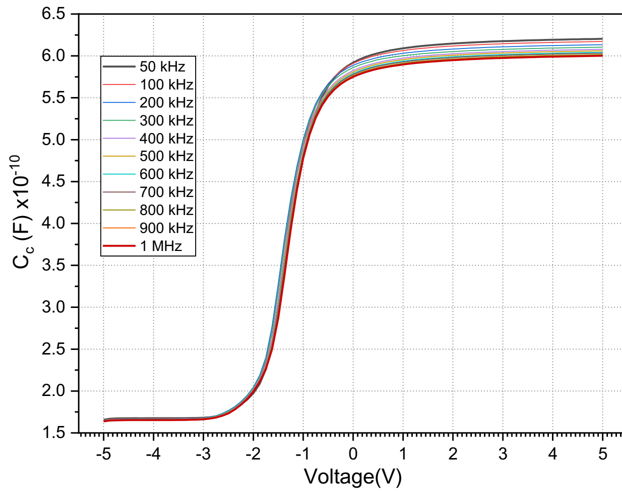

Fig. 6 Corrected capacitance (C_c) characteristics of Al/(Er_2O_3/SiO_2/n-Si)/Al MOS capacitor for various frequencies range from 50 kHz to 1 MHz

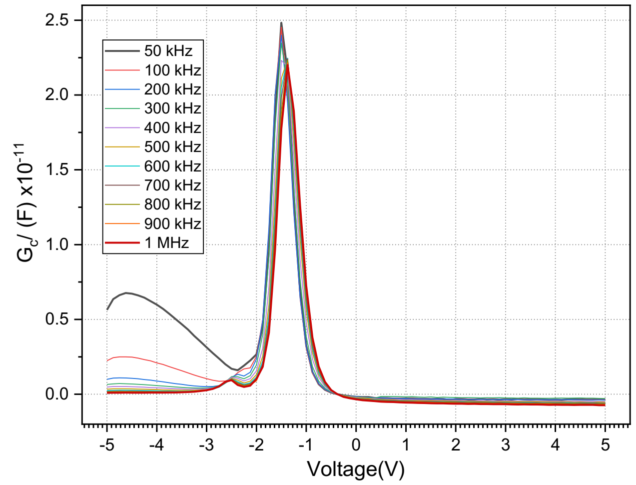

Fig. 7 Corrected conductance (G_C/ω) measurements for Al/(Er_2O_3/SiO_2/n-Si)/Al MOS capacitor for various frequencies ranges from 50 kHz to 1 MHz

where

$$a = G_m - \left[G_m{}^2 + (\omega C_m)^2 \right] R_S \tag{7}$$

Figures 6 and 7 show the C_c–V and G_c/ω–V curves of the MOS capacitor measured in the voltage raised from − 5 to 5 V. There is no significant change between the C–V and the C_c–V curves because the thin SiO_2 layer deposited onto the Si to reduce the lattice mismatch keeps the capacitance almost the same. However, in G/ω–V and G_c/ω–V curves, there is an important variation. After the measured conductance is corrected, the admittance peaks fade away as the frequency increases. This fading is attributed to the decrease in R_s which is demonstrated by Fig. 5 and in Table 1.

The interface state density, D_{it} was calculated using the Hill-Coleman method by the equation [22, 23].

$$D_{it} = \frac{2G_{c.max}/\omega}{Aq[(G_{c.max}/(\omega C_{ox}))^2 + (1 - C_c/C_{ox})^2]} \tag{8}$$

where q is the elementary charge (1.60×10^{-19} C), A is the gate electrode area of the MOS capacitor (1.77×10^{-2} cm^2), $G_{c.max}/\omega$ are maximum values of G_c/ω collected from the G_c/ω–V curve, C_C is corrected capacitance of the MOS capacitor corresponding to $G_{c.max}$, and C_{ox} is the equivalent (total) capacitance of oxides.

As shown in Fig. 8 and Table 1, the D_{it} decreases as a reciprocal function ($\sim 1.5f^{-0.09} \times 10^{11}$) with the increase of applied bias voltage frequency, f. Particularly, at low frequencies the interface density is strongly dependent on frequency which leads an increase in the capacitance of the MOS structure in strong accumulation region. On the other hand, it is expected that at high frequencies (> 1 MHz), the interface densities to be negligibly dependent on frequency because at low frequencies while the D_{it} can follow the applied voltage signal, at high frequencies the D_{it} cannot. This is because its transport mechanisms are too slow compared to the signal [21, 24].

Acceptor-like interface states and donor-like interface states are the two interface states affecting Φ_B. The Φ_B, N_D, E_F, and V_D are obtained from the reciprocal squared of corrected $C_c{}^{-2}$–V plot. At higher frequencies, it is observed that linearity of the obtained $C_c{}^{-2}$–V curves increases indicating the uniform distribution of interface states in the device structure given Fig. 9.

The relation between $C_c{}^{-2}$ and V is given as [22, 23]

$$C_C^{-2} = \frac{2(V_o + V)}{\kappa_s \varepsilon_o q A^2 N_D} = mV + mV_o \tag{9}$$

where m is the slope and mV_o is the intercept that determined from $C_c{}^{-2}$–V plot given in Fig. 9.

$$m = \frac{2}{\kappa_s \varepsilon_o q A^2 N_D} \tag{10}$$

where A is the gate electrode area (1.77×10^{-2} cm^2), κ_s is the dielectric constant of silicon (11.9 for n-Si). From Eq. (10)

$$N_D = \frac{2}{\varepsilon_s \varepsilon_o q A^2 |m|} \tag{11}$$

N_D is the free electron concentration when all shallow donor levels are ionized, V is the applied bias voltage and V_o is the built-in potential. From the intercept of $C_c{}^{-2}$–V plot with the V axis, V_o (= intercept/m) can be determined by Eq. (9) [17–19]

Table 1 Electrical parameters of E-beam $Al/(Er_2O_3/SiO_2/n\text{-}Si)/Al$ MOS capacitor

Frequency (kHz)	$G_{c.max}/\omega$ (10^{-11} F)	C_c (10^{-10} F)	R_s (−5 to −2.25 V) (Ω)	R_s (−0.375 to 5 V) (Ω)	D_{it} (10^{10} eV^{-1} cm^{-2})
50	2.49	5.753	849.37–263.16	83.98	10.030
100	2.45	5.744	197.75–261.95	55.35	9.826
200	2.37	5.741	72.50–69.84	39.58	9.469
300	2.29	5.718	47.96–50.07	34.46	9.055
400	2.26	5.677	38.62–41.60	31.08	8.766
500	2.19	5.656	32.91–35.90	28.65	8.404
600	2.17	5.638	29.40–32.12	26.72	8.275
700	2.15	5.628	27.07–29.65	25.33	8.168
800	2.13	5.612	25.53–27.73	24.28	8.033
900	2.11	5.604	24.35–26.30	23.40	7.935
1000	2.10	5.601	23.36–24.86	22.51	7.874

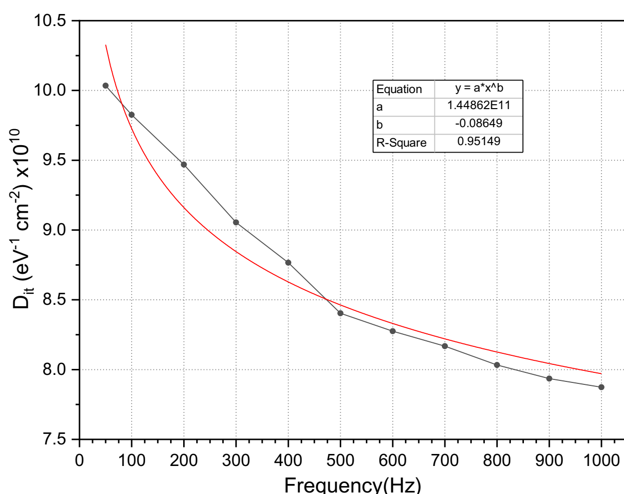

Fig. 8 Variations of D_{it} as a function of frequency for $Al/(Er_2O_3/SiO_2/n\text{-}Si)/Al$ MOS capacitor

$$V_D = V_o + \frac{k_B T}{q} \tag{12}$$

where V_D is the diffusion potential, k_B is the Boltzmann's constant (1.38×10^{-23} JK^{-1}), T is the room temperature in Kelvin (300 K). The barrier height (Φ_B) may be calculated using the C_c^{-2}–V measurements in the equation [25].

$$\Phi_B = c_2 V_o + \frac{k_B T}{q} + E_F - \Delta\Phi_B \tag{13}$$

where c_2 is the correction factor which is the relationship between the theoretical doping concentration ($N_D = 4.31 \times 10^{15}$ cm^{-3}) and the experimental values and can be extracted from the slope of C^{-2}–V curves or may be given as $c_2 \approx N_D(\text{exp.})/N_D(\text{th.})$ [4, 26–28], $E_F = \frac{k_B T}{q} \ln(\frac{N_C}{N_D})$ is the Fermi energy level, N_C (2.82×10^{19} cm^{-3}) is the effective density of states [$\sim 5.0 \times 10^{15}$ T$^{3/2}$ (m^*_n/m_o), T = 300 K,

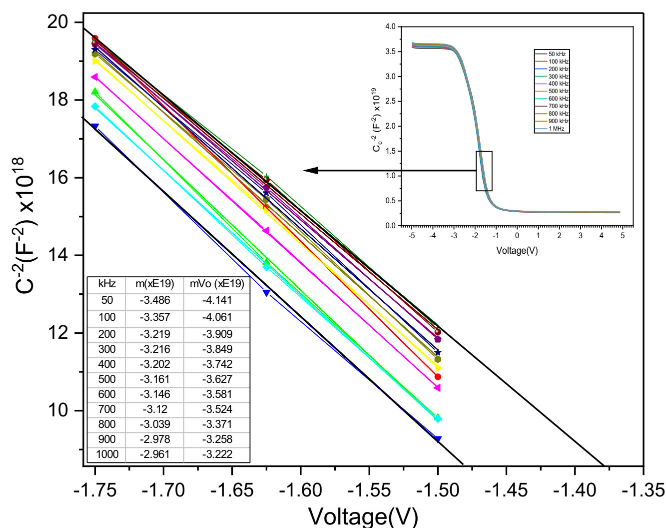

Fig. 9 C_c^{-2}–V characteristics and corresponding linear fit function of $Al/(Er_2O_3/SiO_2/n\text{-}Si)/Al$ MOS capacitor at various frequencies from 50 kHz to 1 MHz

Table 2 Electrical parameters of Al/(Er_2O_3/SiO_2/n-Si)/Al MOS capacitor obtained from C_C^{-2}–V

Frequency (kHz)	V_o (V)	V_D (eV)	N_D (10^{15} cm^{-3})	E_F (eV)	$\Delta\Phi_B$ (10^{-3} eV)	Φ_B (eV)	W_D (10^{-4} cm)	c_2
50	1.19	1.21	1.087	0.2628	1.744	0.567	1.213	0.252
100	1.21	1.24	1.128	0.2618	1.768	0.584	1.201	0.262
200	1.21	1.24	1.177	0.2607	1.789	0.598	1.178	0.273
300	1.20	1.22	1.178	0.2607	1.783	0.593	1.169	0.273
400	1.17	1.19	1.183	0.2606	1.775	0.587	1.153	0.275
500	1.15	1.17	1.199	0.2603	1.772	0.585	1.135	0.278
600	1.14	1.16	1.204	0.2602	1.771	0.584	1.128	0.279
700	1.13	1.16	1.214	0.2599	1.771	0.584	1.119	0.282
800	1.11	1.14	1.247	0.2593	1.775	0.586	1.095	0.289
900	1.09	1.12	1.272	0.2587	1.778	0.588	1.076	0.295
1000	1.09	1.11	1.279	0.2586	1.778	0.587	1.071	0.297

$m^*_n/m_o = 1.08$ for *n*-Si] in the conduction band for *n*-Si at room temperature, and $\Delta\Phi_B$ is the image force barrier lowering which is calculated from

$$\Delta\Phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_o}} \text{where} E_m = \sqrt{\frac{2qN_D V_D}{\varepsilon_s\varepsilon_o}} \quad (14)$$

E_m is the maximum electric field [29, 30].

The obtained electrical parameters are listed in Table 2. Diffusion potentials V_D(s) are located at negative voltages indicating that positive charges are trapped in the MOS capacitor in the fabrication process. Furthermore, as seen in Table 2, the doping concentration N_D, increases with increasing applied voltage frequency. The Fermi level E_F is almost constant with varying applied voltage frequency. $\Delta\Phi_B$ varies a little about 1.773×10^{-3} eV depending on the frequency. V_D and V_o are related through temperature ($V_o = V_D - k_BT/q$, $T = 300$ K) and values are very close. They increase for 50 kHz and 100 kHz frequencies then decrease with the increase of frequency accordingly. The C_c^{-2}–*V* data also reveals that Φ_B stays almost constant. This is because of the dependence of the built-in potential V_o, E_F, and $\Delta\Phi_B$. Finally, the depletion layer width (W_D) is given by the equation,

$$W_D = \sqrt{\frac{2\varepsilon_s\varepsilon_o V_D}{qN_D}} \quad (15)$$

where V_D is the diffusion potential and N_D is the free electron concentration. Depending on V_D/N_D ratio W_D decreases from 1.117×10^{-4} to 1.029×10^{-4} cm with increasing frequency (see Table 2) [18, 29].

4 Conclusion

In summary, the electrical parameters of Al/(Er_2O_3/SiO_2/n-Si)/Al MOS capacitor such as R_s, D_{it}, Φ_B, $\Delta\Phi_B$, V_o, V_D, N_D, W_D, and E_F were determined from frequency-dependent *C–V*, *G/ω–V* and C_c^{-2}–*V* data. The experimental results show that the Φ_B and V_D increases for 50–100 kHz frequencies and then decrease with increasing frequency. We also investigated the effects on the series resistance (R_s) and the interface state density (D_{it}) through the *C–V* and *G/ω–V* plots. From the obtained results, we noticed that the effect of voltage and frequency on R_s reduction is significant. The introduction of SiO_2 layer between the high-k Er_2O_3 and n-Si appears to be the main reason for R_s reduction. R_s–*V* (Fig. 5) and *G/ω–V* (Fig. 7) curves demonstrate a strong and high response at − 1.5 V for all frequencies. However, at voltages greater than − 0.375 V R_s decreases, becomes stable and remains fixed. Similarly, the admittance peaks reduced and disappeared at high frequencies. The disappearance of these peaks from Figs. 5 and 7 is because the interface charges can hardly follow the AC signal at high frequencies. Calculations also show that D_{it} is affected by frequencies greatly. Figure 8 shows the decrease in D_{it} as a reciprocal function ($\sim 1.5f^{-0.09} \times 10^{11}$) of the applied voltage frequency. Especially, at low frequencies, D_{it} is strongly dependent on frequency which leads an increase in the capacitance of the MOS structure in the strong accumulation region. However, at high frequencies, D_{it} cannot follow the AC signal since its transport mechanisms are too slow compared to the signal.

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