



Electrical characteristics of atomic layer deposited Au/Ti/HfO₂/n-GaAs MIS diodes in the wide temperature range

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Abstract

Au/Ti/HfO₂/n-GaAs MIS (metal/insulating layer/semiconductor) diodes were fabricated by atomic layer deposition technique and their electrical properties were investigated in detail by the help of current–voltage (I – V) and admittance measurements in the temperature range of 60–320 K. Together with the surface morphology analysis on the HfO₂ thin-film layer, main electrical parameters such as series resistance (R_s), zero bias barrier height (Φ_{Bo}), ideality factor (n), impedance (Z) and phase angle were determined and effects of temperature on these parameters of the MIS diodes were discussed. The evaluation of I – V data exhibits a decrease in R_s and Φ_{Bo} , however an increase in n , with a decrease in temperature. Temperature-dependent conductance (G) and capacitance (C) characteristics of the MIS diode were investigated at 1000 kHz in the voltage interval in between – 3 and 2 V. G and C values were found in a direct relation with the change in temperature. On the other hand, Z values showed an inverse proportionality with temperature. The phase angle versus voltage plots were evaluated at different temperatures (60–320 K) at 1000 kHz and the obtained results indicated that the device behaves more capacitive in the voltage range of – 3 V and about 0.4 V for all temperature, and phase angle decreases with increasing temperature from 0.4 to 1.6 V. In addition, the interface state density (D_{it}), the effective oxide charge density (Q_{eff}) and effective number of charges per unit area (N_{eff}) of the fabricated diodes were investigated over temperature range 60–320 K in which these values were found in a decreasing trend with increasing temperature.

1 Introduction

Thin-film technology has been widely used in the production from past to present and characterization of variety of devices derived from traditional metal–semiconductor (MS) with Schottky barrier (SB) formation between metal and semiconductor [1, 2]. Recent experimental results have shown that addition of an interface layer in this structure by different methods affects significantly the electronic characteristics and capacitive behavior of this type of diodes. Thus,

the demands in a wide variety of electronic applications have triggered the use of interface layers where different deposition methods have been point of interest to reach feasible regions of interest. In this field, the presence of this inter-layer can change the electrical characteristics of MS diode. The layer intentionally formed or self-generated oxide layer on the semiconductor surface can affect ideality of the diode behavior. It is a well-known fact that oxide/dielectric/insulator layers behave different than native oxide layer on the active semiconductor layer [3–5]. Most of the works on this SiO₂ layer have been retained its popularity with external deposition by different methods since it can provide inherent chemical and thermal stability on active semiconducting layer where it is commonly chosen as n- or p-type Si wafers [6–8]. Because of suffering from high leakage currents with SiO₂ interface layer, high-dielectric materials such as TiO₂, HfO₂ and ZrO₂ have been a point of interest in the diode applications as a potential candidate for SiO₂ [9–15]. At this point HfO₂ has attracted great interest as being a high-dielectric layer at the interfacial layer in which the reported studies on the use of this layer indicate reducing effect in the leakage current and being thermodynamically stable in

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contact with the surface of semiconductor substrate [16–20]. It is popular with the material characteristics of large band gap, high dielectric constant and resistivity [21–23]. At the interface, the high dielectric behavior of HfO_2 offers variety of advantageous, especially low leakage current and high barrier height to limit tunneling conduction in the diode [24, 25].

The surface properties and high-quality of HfO_2 layer strongly depend on deposition techniques and conditions of the interfacial layer and the preparation conditions of the HfO_2 surface before deposition of rectifying contact [26–28]. In literature, several deposition techniques, mainly atomic layer deposition (ALD), molecular-beam epitaxy (MBE), sputtering and metal-organic chemical vapor deposition (MOCVD), have been used to grow HfO_2 on semiconductor [29–32]. Among them, ALD technique with its submonolayer-by-submonolayer deposition mode characteristic has been preferred in thin-film deposition to achieve conform and uniform film thickness with monolayer precision and it is one of the feasible techniques for depositing oxide materials in the fabrication of MIS structures [33–36]. The oxide materials play significant roles in the forming of the barrier height (BH) in these structures. The addition of an oxide layer between semiconductor and metal has been widely used to modify the capacitance–voltage (C – V), conductance–voltage (G – V) and current–voltage (I – V) characteristics of the diode where it generally results in increasing the BH of the structure [1]. Analysis of these behaviors of the MIS structures in the narrow voltage range and at only room temperature does not give detailed information about the nature of barrier formed at metal/semiconductor interface and the conduction process. The characteristic plots of G – V , C – V and I – V have been ensured to achieve correct and certain knowledge concerning electrical properties of the MIS diodes.

In literature, there are several works on metal/GaAs and metal/insulator/GaAs diodes [10, 36–41]. Among them, Ozdemir et al. have studied the effects of the time-dependent and exposure time to air on Au/ n -GaAs diode where n values were reported in between 1.089 and 1.46 at room temperature [37]. On the other hand, Biber et al. have studied BH enhancement in Au–Ge/ n -GaAs diode with anodization process. The values of BH and n were found in a range of 0.730 to 0.667 eV and 1.09 to 1.46, respectively [38]. With different rectifying contact, Biyikli et al. have studied electrical characteristics of Au/Ti/ n -GaAs diode and the value of BH was presented in an interval of 0.75–0.76 eV and n values were in between 1.07 and 1.08 [36]. As an MIS diode interlayered with HfO_2 , Budhraj et al. have fabricated the Ti/Au/ HfO_2 /GaAs annealed structure and interface density for this diode structure was determined $6.48 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ and the Be/Au/ HfO_2 /GaAs as-deposited $2.28 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ [41]. In addition, Karabulut has

investigated conduction mechanisms of Au/Ti/ n -GaAs with HfO_2 layer in the temperature range of 60–400 K and in this work, barrier of the Au/Ti/ HfO_2 / n -GaAs diode has modeled by double-Gaussian distribution (GD) [10].

In the present study, the electrical characteristics of the Al/Ti/ HfO_2 /GaAs diode structure were investigated where HfO_2 layer was deposited by ALD technique on chemically cleaned polished GaAs wafer, and the Au/Ti top-ohmic contact was obtained with elemental evaporation. The main diode parameters as saturation current (I_0), Φ_{B0} and n were derived from the conventional thermionic emission (TE) model applied to the I – V values measured over the temperature range of 60–320 K under dark. Besides, the results of G – V and C – V measurements of Al/Ti/ HfO_2 /GaAs MIS diode were studied to determine R_s , Z and phase angle at 1000 kHz over temperature range of 60–320 K. In addition, the D_{it} of Al/Ti/ HfO_2 /GaAs diode were calculated from C – V and I – V measurements. In addition, the Q_{eff} and N_{eff} values were evaluated.

2 Experimental procedure

An Au/Ti/ HfO_2 / n -GaAs MIS diode was fabricated on an n -type GaAs sample with the carrier concentration of $6.8 \times 10^{15} \text{ cm}^{-3}$, the (100) crystal orientation, diameter of 2 in. and having a thickness of 300 μm , $7.43 \times 10^{15} \text{ cm}^{-3}$ carrier concentration and 1.2 $\Omega \text{ cm}$ resistivity (given by the manufacturer). Initially, the GaAs substrate was cleaned [10, 36] and the optimized deposition procedure to form back contact (ohmic contact) for the GaAs semiconductor was applied as given in Ref. [35]. Ohmic contacts with low resistance are necessary for high performance in many III–V devices. In fact, the efficiency of light-emitting diodes (LEDs) and lasers is strongly influenced by contact resistance, and the noise behavior and the gain of a field-effect transistor (FET) are significantly affected by the electrical response of ohmic contacts. Therefore, depending on its contact resistance, pure In metal has been used to form a low-resistance contact to n -type GaAs and an alloy of In–Zn has been presented as being a best choice for contacting p -type GaAs [42–46]. However, In-ohmic contact resistance can be tuned to $1.5 \times 10^{-5} \Omega \text{ cm}^2$ at annealing temperature of 380 $^\circ\text{C}$ [42]. The similar results can be seen in the specific contact resistance of In/GaN where the contact resistivity of the In-contact on GaN was as low as $2.2 \times 10^{-5} \Omega \text{ cm}^2$ after annealing at 300 $^\circ\text{C}$ [43]. In the current work, the resistivity of In-metal contact on n -GaAs was determined using ohmic J – V curve of In/ n -GaAs structure and it was found as about $3 \times 10^{-4} \Omega \text{ cm}$. This value can be used to verify the ohmic nature of this metal contact on GaAs substrate. In addition, the contact resistivity of the In-contact was calculated as $1.5 \times 10^{-4} \Omega \text{ cm}$ which is similar with literature [42–44]. To

construct MIS diode structure, HfO₂ interfacial layer was deposited on the GaAs sample by an ALD system (Savannah S100 ALD). Deposition was performed at 200 °C [10, 47–49] and after this deposition step, Au/Ti rectifier front contacts were formed on HfO₂ layer. In this process, Ti (10 nm) and Au (90 nm) contacts were sequentially evaporated on HfO₂/n-GaAs structure by the magnetron DC sputtering technique in a high-vacuum system of 10⁻⁶ Torr [10, 36]. Au/Ti contact was preferred to obtain low barrier formation, since work function of Au/Ti is smaller than Au. At this point, there are some works to analyze BH of Ti and Au/Ti Schottky contacts on n-InAlAs and these values were reported 0.64 and 0.55 eV, respectively [50, 51]. In the current MIS structure, the Au thin film was used as a top layer to protect the Ti metallic layer on the GaAs substrate. In other words, Au was selected as the second layer to prevent oxidation and also to promote current spreading, and to provide good smoothness to the contact [36, 49]. It is a common technique that Au overlayer is deposited on top to enhance conductivity and prevents resistance problems [52]. Therefore, Au/Ti layer was preferred instead of one-type metal contact such as Au or Ti. Figure 1a, b shows the schematic model and energy band diagram of the MIS, respectively.

After the fabrication process, I–V, C–V and G–V measurements of the MIS diodes were performed in a wide temperature range of 60–320 K. To investigate the surface morphology of the GaAs substrate and HfO₂ layer, atomic force microscopy (AFM) images were obtained by PARK system XE 100E AFM. The electrical measurements were carried out by a Leybold Heraeus closed-cycle helium cryostat, a Keithley 487 Picoammeter voltage source and a HP model 4192A LF impedance analyzer under dark conditions.

3 Result and discussion

The 2D and 3D images AFM images of the GaAs substrate are shown in Fig. 2a, b, respectively. From 2D planar view, root-mean-square (RMS) roughness value of the GaAs substrate was obtained as 895 pm. In addition, the 2D and 3D AFM images of the HfO₂ are presented in Fig. 3a, b, respectively. The HfO₂ layer exhibited uniform and homogenous surface and the RMS roughness value of this film layer was obtained 1.2 nm.

Figure 4a shows the measured I–V characteristics for Au/Ti/HfO₂/n-GaAs MIS diode in the temperature range of 60–320 K. The main electrical parameters were determined from the linear part of these I–V curves at each temperature according to TE equation [10, 26, 36, 38, 40, 53]:

$$I = I_0 \left[\exp \left(\frac{q(V - IR_s)}{nkT} \right) - 1 \right] \tag{1}$$

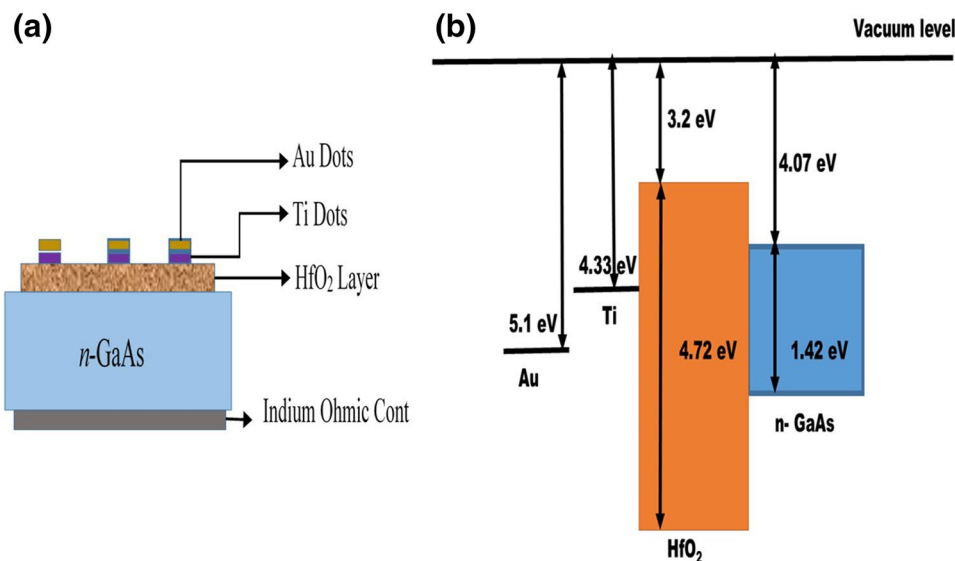
where I₀ is the saturation current in a relation with temperature as

$$I_0 = AA^*T^2 \exp \left(-\frac{e\Phi_{Bo}}{kT} \right) \tag{2}$$

and Φ_{Bo} is the zero bias effective BH, A is the rectifying contact area of the diode, A* is the effective Richardson constant, n is the ideality factor and T is the absolute temperature. Using the intercept of the linear I–V relation for each temperature step in Fig. 4a, the values of Φ_{Bo} were extracted and tabulated in this figure.

From Eq. (1), the n can be determined from

Fig. 1 (Color online) **a** Schematic model and **b** energy band diagram of the Au/Ti/HfO₂/n-GaAs diode



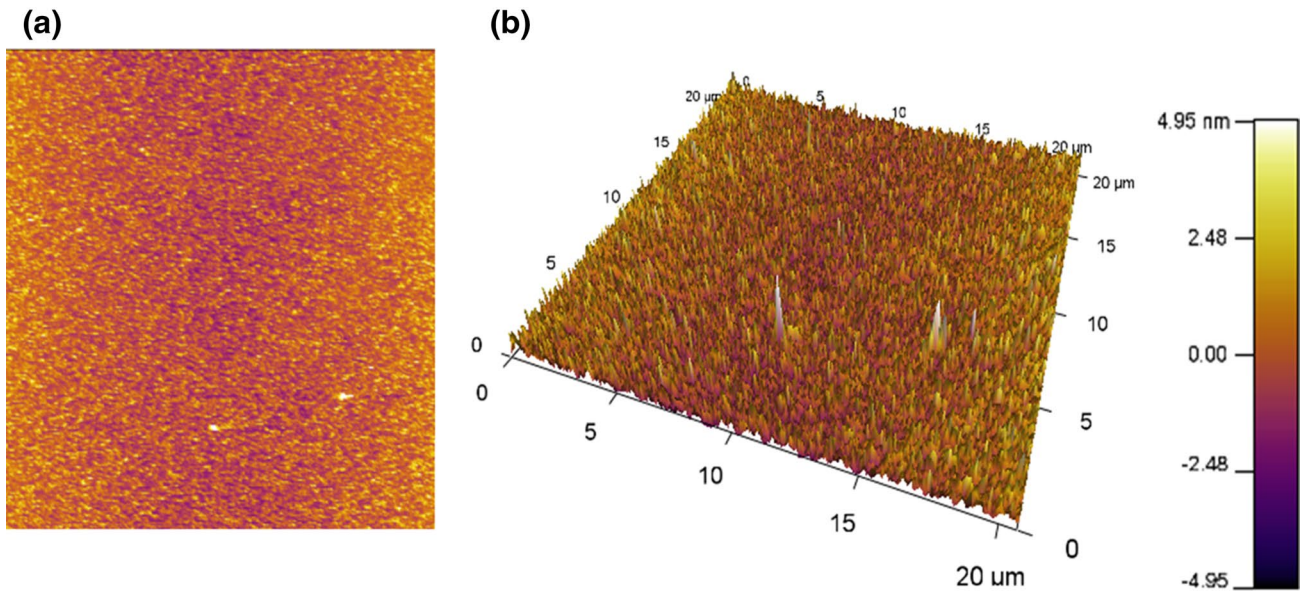


Fig. 2 (Color online) **a** 2D and **b** 3D for the surface morphology of GaAs substrate, the RMS value is 895 pm

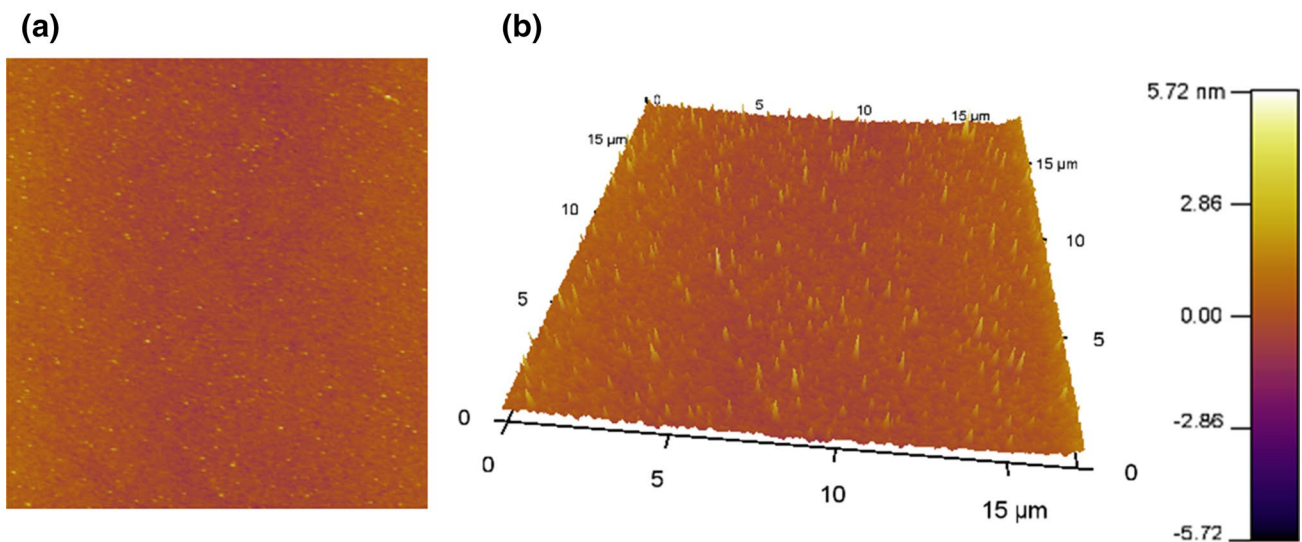


Fig. 3 (Color online) **a** 2D and **b** 3D for the surface morphology of deposited 5 nm HfO₂ on substrate, the RMS value is 1.20 nm

$$n = \frac{q}{kT} \frac{dV}{d(\ln(I))}. \quad (3)$$

The results of n for each temperature were deduced from the linear region of Fig. 4a using Eq. (3) and listed in the figure. Thus, the values of n for this MIS diode were determined as 1.08 and 2.58 at 320 and 60 K, respectively. These results derived for Au/Ti/HfO₂/ n -GaAs MIS diode are higher than n of Au/Ti/ n -GaAs MS diode [36] and it indicates that the presence of the HfO₂

interfacial layer triggers deviation from ideality. As seen from the Table inset in Fig. 4a, n values decrease with increasing temperature and it is similar with literature where Biyikli et al. [36] reported that n of Au/Ti/ n -GaAs MS diode is between 1.074 and 2.221 in the temperature range of 300–60 K. The higher than unity value of n was the indication of laterally inhomogeneity in the MIS diode [10, 26, 38].

The barrier height at zero bias point Φ_{B_0} could be obtained from the I_0 value as

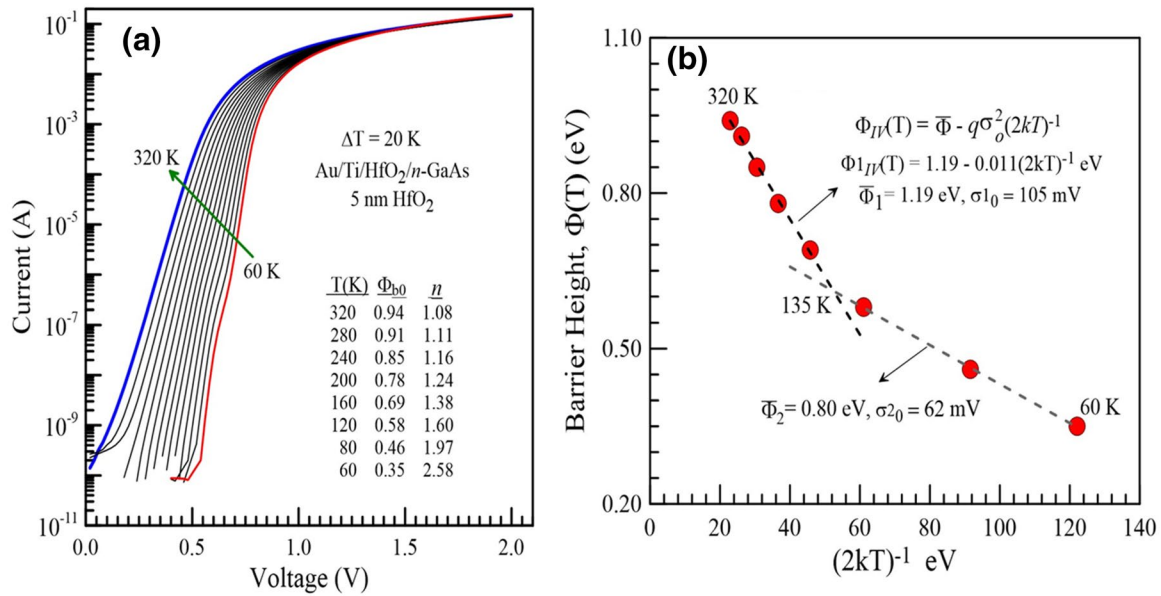


Fig. 4 (Color online) **a** Experimental forward bias current versus voltage characteristics with the sample temperature as a parameter for the Au/Ti/HfO₂/n-GaAs diode, **b** Φ_{B0} versus $(2kT)^{-1}$ Gaussian plot

$$\Phi_{B0} = \frac{kT}{q} \ln \left(\frac{AA^*T^2}{I_0} \right) \tag{4}$$

Using Eq. 4, Φ_{B0} values were found as 0.35 and 0.94 eV at 60 and 320 K, respectively. In Au/Ti/n-GaAs MS diode form, it was reported in between 0.770 and 0.475 eV in the temperature range of 300–60 K [36]. Some researchers [10, 38, 40] have obtained an approximate Φ_{B0} value of 0.76 eV at 300 K for Au/Ti/n-GaAs MS diode. At room temperature, Au/Ti/HfO₂/n-GaAs MIS diode gives higher Φ_{B0} values than Au/Ti/n-GaAs MS diode. Thus, it is an obvious fact that HfO₂ interfacial layer causes the modification and increase of the Φ_{B0} and the rise in Φ_{B0} could be related to the free carriers having enough energy to pass over the barriers so they have the additive to the conduction with increasing T [10, 54]. As seen Fig. 4b, the temperature-dependent data of Φ_{B0} vs. $(2kT)^{-1}$ plot obey the Gaussian Distribution (GD) of the BHs for the Au/Ti/HfO₂/n-GaAs MIS diodes in the 60–320 K range. The intercepts and slopes of the straight lines of the Φ_{B0} vs. $(2kT)^{-1}$ plot for MIS diodes give the average Φ_{B0} and σ_{s0} values of 1.19 eV and 105 mV in the 135–320 K region and 0.80 eV and 62 mV in the 60–135 K region, respectively.

As seen Fig. 4a, the downward curvature in the I - V plots is attributed to a continuum of D_{it} at high forward bias values, which are in equilibrium with the semiconductor, apart from the effect of R_s . It is an important factor especially in the downward curvature of the forward bias I - V plots [55]. In addition, R_s impresses performance of the MIS diodes. Therefore, initially parasitic resistances (R_i) were

investigated. To estimate this effect of R_i in the MIS diode, R_s and R_{sh} were calculated. In the case of Au/Ti/HfO₂/n-GaAs MIS diode performance, to obtain high power and high speed of diodes, R_s is expected to be in low values due to the fact that it is attributed to the resistance effects of both diode and structure and contact regions, and interface state effects in the junction [56–59]. On the other hand, R_{sh} values are expected to be high and it can be associated with high leakage current due to the contacts and the surface inhomogeneities in the Au/Ti/HfO₂/n-GaAs MIS diode structure as a result of current component affected by localized states and an accumulation layer at the surface [60]. According to R_i relation as $R_i = dV_i/dI_i$, the obtained R_i are plotted in Fig. 5. As given in this figure, R_i increases with decreasing the bias voltage and the low voltage region (0.2–0.4 V) $R_i = R_{sh}$ (about 10^8 – $10^7 \Omega$). At this time, the high-voltage region (1.6–2 V) $R_i = R_s$ and R_s values for the MIS diodes approach to constant values as about 7.2 Ω at high-voltage region.

Then, second, the R_s of the diode was determined using the technique proposed by Cheung [61]. Cheung’s function can be expressed as

$$\frac{dV}{d(\ln(I))} = IR_s + n \left(\frac{kT}{q} \right) \tag{5}$$

where the term IR_s is the voltage drop across R_s in the diodes. As seen from Fig. 6, $dV/d(\ln(I))$ vs I plots are in linear characteristics and according to Eq. (5), R_s were determined for the MIS diode from the slope of Fig. 6 as 7.57 Ω

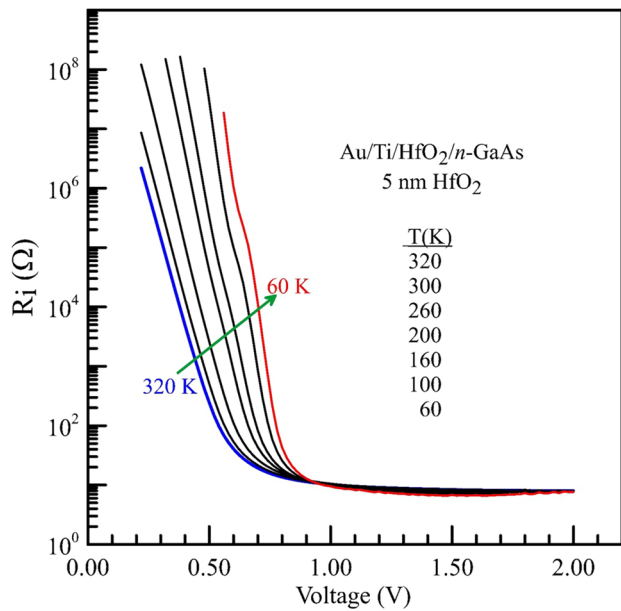


Fig. 5 (Color online) Voltage-dependent resistance from the current–voltage characteristics at some temperatures in Fig. 2

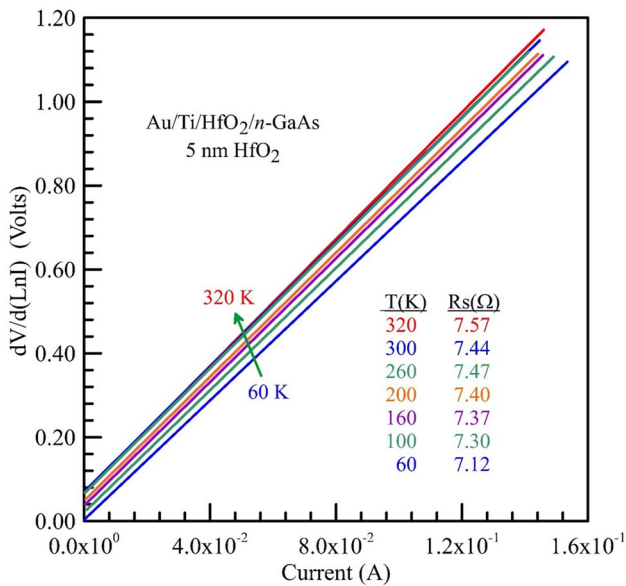


Fig. 6 (Color online) $dV/d(\ln(I))$ versus I plots from the current–voltage characteristics using Cheung and Cheung method at same temperatures in Fig. 1

and 7.12Ω at 320 K and 60 K, respectively and all values are given in Fig. 6. As listed in this figure, these values are in close good agreement with each parasitic resistance at high forward bias voltage region.

The variation of R_s with temperature, from 7.57 to 7.12Ω at 320 K and 60 K, depicts a decrease in its value with increase in temperature. The reason for this, the R_s value change from

7.57 to 7.12Ω with temperature with no great influence from the change in temperature can be explained the diffusion of GaAs atoms into the metal oxide layer, HfO_2 . Furthermore, the origin of the oxide charges in the HfO_2 thin layer can be ascribed to high density of defects induced by the presence of the oxygen vacancies and broken bonds. In general, the oxygen vacancies take place in the oxide film and/or at the oxide/GaAs interface [45, 62–65]. The n values of diode are in a narrow range and it can be associated to R_s [66]. In addition, to determine these values, Chengs' method was applied only to downward curvature region of $\ln I-V$ characteristic. On the other hand, Norde and generalized Norde functions were applied to the full forward bias region of the $\ln I-V$ characteristic plots. Therefore, R_s values obtained by Norde plots are larger than those determined from Cheung functions [67].

The origin of the oxide charges in the HfO_2 thin layer is ascribed to the high density of defects induced by the presence of the oxygen vacancies and broken bonds. In general, the oxygen vacancies take place in the oxide film and/or at the oxide/GaAs interface. The non-ideal behavior as obtained of $I-V$, $C-V$ and $G-V$ characteristics dominantly depends on R_s , D_{it} , Q_{eff} and N_{eff} , and their variations as a result of changing applied voltage and temperature of the Au/Ti/HfO₂/n-GaAs MIS diode. The D_{it} of MIS diode is affected from the nature of Q_{eff} and N_{eff} in the diodes. Therefore, together with D_{it} , these values were obtained for the Au/Ti/HfO₂/n-GaAs MIS diode. The D_{it} ($I-V$), D_{it} ($C-V$), and N_{eff} values of the Au/Ti/HfO₂/n-GaAs diode can be seen in Fig. 7.

For MIS diode having D_{it} in equilibrium with the semiconductor, the values of n become greater than unity, as proposed by Card and Rhoderick [68, 69], and it is given by

$$n = 1 + \frac{\delta}{\epsilon_i} \left(\frac{\epsilon_s}{w_D} + qD_{it} \right) \quad (6)$$

where ϵ_s and ϵ_i are the permittivity of semiconductor and interfacial layer, respectively, w_D is the space charge width.

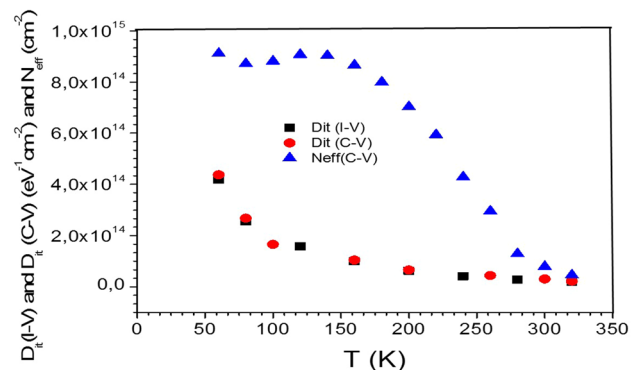


Fig. 7 (Color online) The D_{it} ($I-V$), D_{it} ($C-V$), and N_{eff} for the Au/Ti/HfO₂/n-GaAs diode

For each temperature, the values of n were determined from I - V plot and the variation of w_D was extracted from C^{-2} - V characteristics. In addition, the values of D_{it} were obtained from Eq. (6) and the results are given in Fig. 7. As presented in this figure, the D_{it} decreases with increasing temperature where the values at 60 and 320 K are 1.179×10^{14} and $2.05 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$, respectively.

In addition, at high frequencies ($f > 500 \text{ kHz}$) the interface states do not contribute to the capacitance since they are in equilibrium with the semiconductor. The relation of the theoretical carrier density N'_D and the experimental carrier doping density N_D is known.

$$C_2 = \frac{N'_D}{N_D} \tag{7}$$

The density of interface state density D_{it} was calculated at different temperature using

$$C_2 = \frac{1}{1 + \beta} \tag{8}$$

where $\beta = \frac{q\delta D_{it}}{\epsilon_i}$ [68–71]. The D_{it} were derived at different temperatures from Eq. (8), by taking the δ value as 5 nm. The obtained D_{it} values are $2.21 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ at 320 K and $4.37 \times 10^{14} \text{ eV}^{-1} \text{ cm}^{-2}$ at 60 K. The obtained values of D_{it} (C - V) at temperature are presented in Fig. 7. As shown in Fig. 7, the obtained D_{it} value decreases with increasing temperature and it is in a close agreement with D_{it} calculated from I - V characteristics (Fig. 7).

Using the flat band voltage (V_{FB}) values caused by the non-ideal effects, N_{eff} and Q_{eff} were calculated for Au/Ti/HfO₂/ n -GaAs MIS diode [72]. The flat band voltage, V_{FB} , can be expressed as

$$V_{FB} = V_{FB}^o - \Delta V \tag{9}$$

where V_{FB}^o for the MOS capacitor without oxide or interface charge as

$$V_{FB}^o = \Phi_m - \Phi_s = \left(\Phi_m - \frac{q\chi + E_g - (E_F - E_v)}{q} \right) \tag{10}$$

where $q\chi$ is the semiconductor electron affinity, $q\Phi_m$ the semiconductor work function, E_g the semiconductor energy gap, and $q\Phi_s$ the metal gate work function and is the position of the semiconductor Fermi level above the valance band in the neutral semiconductor bulk [72].

The measure of V_{FB} using high-frequency C - V method provides an information about the level of charges present inside the oxide layer and V_{FB} is directly obtained from the experimental and theoretical C - V curves and from the intercept of experimental $1/C^2$ vs. V_G curve as explained in the previous section. Once the flat band voltage V_{FB} is determined using

one of the methods explained, its value is used to calculate the Q_{eff} and N_{eff} using the following equation [72],

$$N_{eff} = \frac{Q_{eff}}{q} = \frac{C'_{ox} (V_{FB}^o - V_{FB})}{q} \tag{11}$$

where C'_{ox} is the oxide capacitance per unit area measured at strong accumulation.

The Q_{eff} of Au/Ti/HfO₂/ n -GaAs MIS diode was determined $1.46 \times 10^4 \text{ cm}^{-2}$ and $7.24 \times 10^{-6} \text{ cm}^{-2}$ for 60 K and 320 K, respectively, which shows a significant decrease in Q_{eff} depending on increase in temperature. At this time, the N_{eff} of Au/Ti/HfO₂/ n -GaAs MIS diode was calculated for $9.11 \times 10^{14} \text{ cm}^{-2}$ and $3.52 \times 10^{13} \text{ cm}^{-2}$ for 60 K and 320 K, respectively, which shows a significant decrease in N_{eff} due to increasing temperature as seen from Fig. 7. The D_{it} values for Au/Ti/HfO₂/ n -GaAs diode were around $2 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ at 300 K, which are much lower than that of the Ti/Au/HfO₂/GaAs ($D_{it} = 6.48 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$) and the Be-Au/HfO₂/GaAs ($D_{it} = 2.28 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$). In addition, the interface states and the effective oxide charges were affected by increasing temperature. It can be seen from the results, the Q_{eff} , N_{eff} and D_{it} decrease with the increasing temperature.

The D_{it} cannot follow the ac signal at enough high frequencies ($f \geq 1 \text{ MHz}$) and consequently, the contribution of D_{it} capacitance to the total capacitance can be ignored [73, 74]. For that reason, the G - V and C - V measurements of the MIS diodes were performed at 1000 kHz. The temperature-dependent C - V and the G - V measurements for the MIS diodes are given in Fig. 8a, b, respectively. As seen from Fig. 8a, the values of C give a peak in each temperature, shifting to forward voltage region with decreasing temperature. This peak behavior of C was investigated for MIS structures by some researchers [27, 75–78]. Such a behavior is usually referred to the R_s , and reordering of the interface state density D_{it} . G - V characteristics of the MIS diode are shown in Fig. 8b. As given in Fig. 8b, the G values of the MIS diode increase rapidly in the interval of 0.25 and 1 V, whereas there is a slow increase in behavior between -3 and 0.25 V. In addition, the crossing of the G - V plots appears at about 1 V and this is an abnormal behavior for ideal SD. The R_s keeps this intersection unobservable in homogeneous SDs [75]. In Fig. 8a, the capacitance value increases from -3.0 V to 0.54 V in the temperature range of 60–320 K.

The R_s profile was evaluated from the results in C - V and G - V measurements in the strong accumulation region [79–82],

$$R_s = \frac{G_m}{(G_m)^2 + (\omega C_m)^2} \tag{12}$$

and the R_s is determined according to Eq. (12) and demonstrated in Figs. 9 and 10 for each temperature, and the

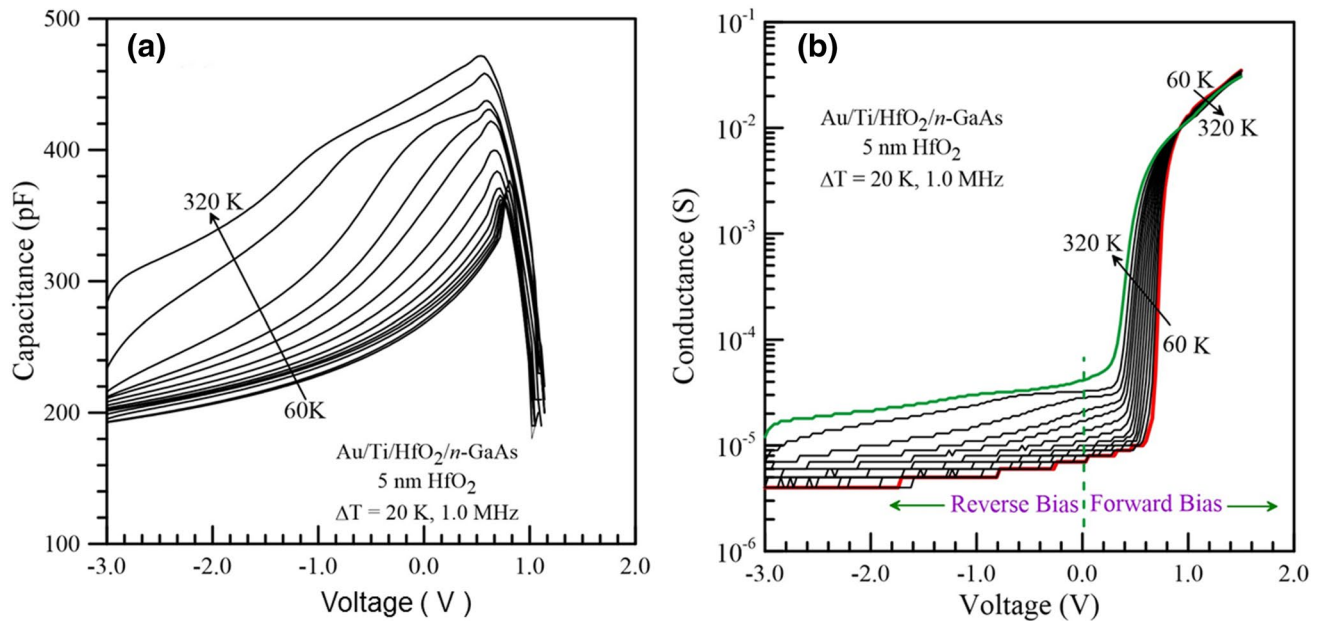


Fig. 8 (Color online) Experimental reverse and forward bias **a** capacitance–voltage and **b** conductance–voltage characteristics with the sample temperature as a parameter for the Au/Ti/HfO₂/n-GaAs structure at 1000 kHz frequency

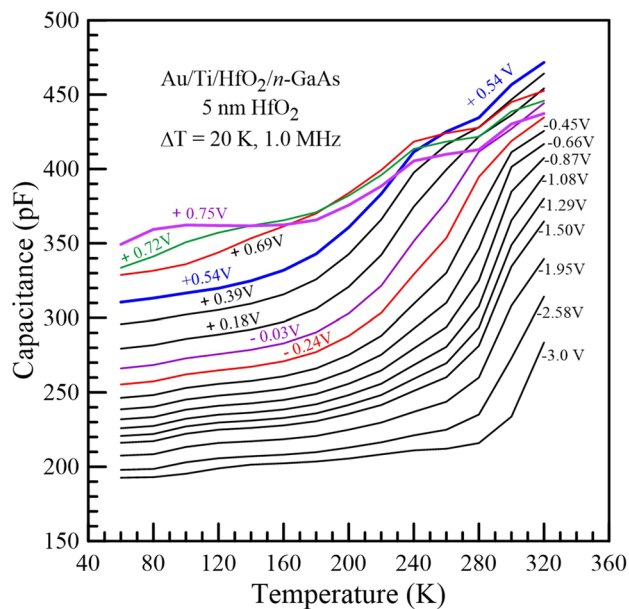


Fig. 9 (Color online) Experimental capacitance versus sample temperature characteristics with the bias voltage as a parameter for the Au/Ti/HfO₂/n-GaAs structure at 1000 kHz frequency

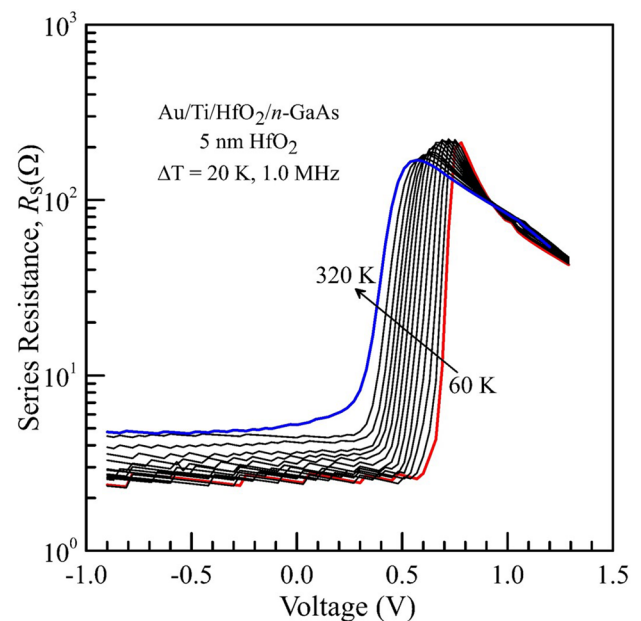


Fig. 10 (Color online) Experimental reverse and forward bias series resistance–voltage characteristics with the sample temperature as a parameter for the Au/Ti/HfO₂/n-GaAs structure at 1000 kHz frequency

temperature dependence of R_s for different voltages at 1000 kHz is also plotted in Fig. 11. It is clearly seen in Fig. 10 that the R_s is constant in the voltage range of -1.0 – 0.3 V for each temperature. Then, the R_s values of the MIS diodes increase rapidly in the interval of 0.3 and 0.55 V. As seen in Fig. 10, the series resistance gives a peak

in the voltage range of 0.55 – 0.9 V depending on temperature. In addition, the temperature dependence of R_s in Fig. 11 indicates that there is an increase with increasing voltage in the voltage range of 0.33 – 0.72 V.

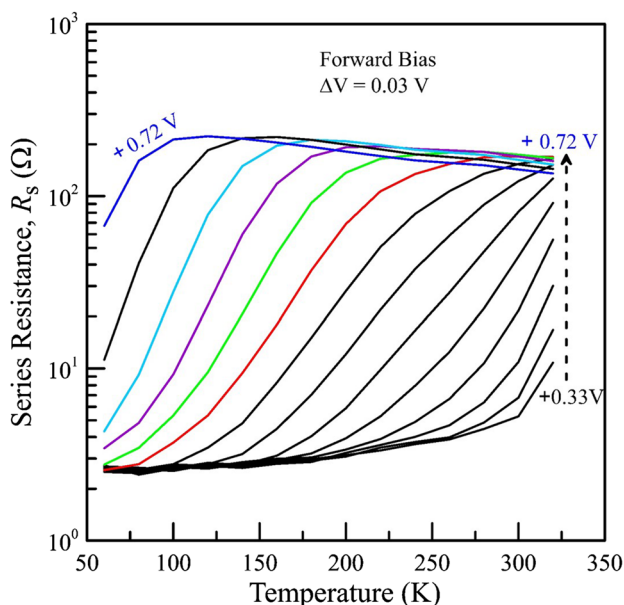


Fig. 11 (Color online) Experimental forward bias series resistance versus sample temperature characteristics with the bias voltage as a parameter for the Au/Ti/HfO₂/n-GaAs structure in the bias voltage range of 0.33–0.72 V

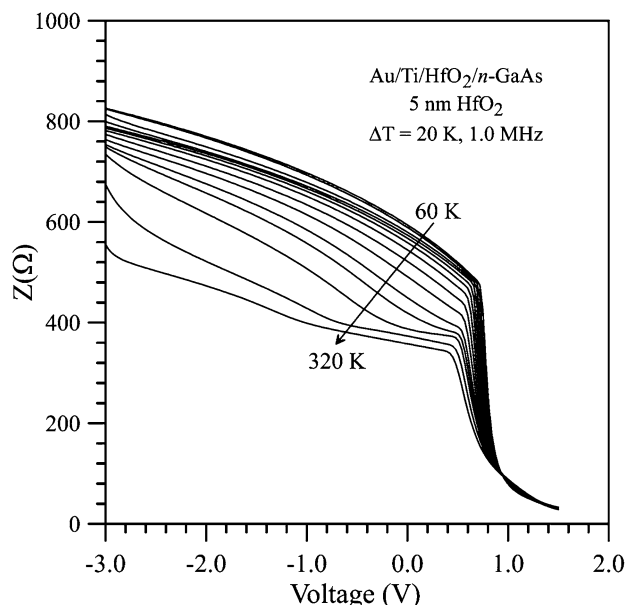


Fig. 12 (Color online) Experimental reverse and forward bias impedance–voltage characteristics with the sample temperature as a parameter for the Au/Ti/HfO₂/n-GaAs structure at 1000 kHz frequency

The Z is the ratio of the phasor voltage to the phasor current in an equivalent circuit of Schottky diodes [81, 83]. The total impedance can be expressed as

$$Z = Z_{Re} + jZ_{Im} = \frac{1}{\left(\frac{1}{R}\right) + j\omega C} \tag{13}$$

where Z_{Im} is its imaginary part and Z_{Re} the real part of the total impedance. Thus, from this relation, the imaginary and real parts for the impedance of a circuit with capacitance (C) and resistance (R) can be recomposed by

$$Z = \frac{R}{1 + (\omega RC)^2} - \frac{j\omega R^2 C}{1 + (\omega RC)^2} \tag{14}$$

As seen from Eqs. (13) and (14), while $\omega \rightarrow \infty$, Z_{Im} goes to zero and Z_{Re} approaches R . Figure 12 exhibits the voltage-dependent plots of the impedance of the MIS diodes in the temperature range of 60 K. This figure also indicates that the impedance value of the MIS diodes decreases with increasing temperature at a given voltage. It is obvious from Fig. 12, the total impedance curves behave independent of voltage in high-voltage region and the voltage-dependent at low voltages. The voltage range of the voltage-independent part of the MIS diodes decreases with increasing temperature. Figure 13 shows the phase angle versus voltage plots for the MIS diode at different temperatures at 1000 kHz. As seen from these plots in Fig. 13, the phase angle has the same value in the voltage range -3.0 to 0.4 V as being

temperature-independent; and at the forward bias voltages above 0.4 V, the phase angle sharply reduces at each temperature, and decreases with increasing temperature at a given bias voltage. However, an intersection point at phase

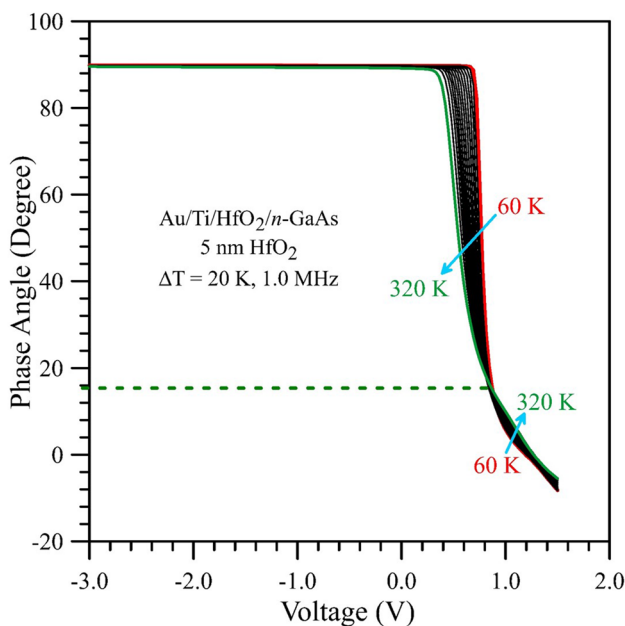


Fig. 13 (Color online) Experimental reverse and forward bias phase angle versus voltage characteristics with the sample temperature as a parameter for the Au/Ti/HfO₂/n-GaAs structures at 1000 kHz frequency

angle curves was observed as independent of temperature and the phase angle increases with increasing temperature at a given bias voltage.

4 Conclusions

The MIS diodes were fabricated using ALD technique, which provides as an effective technique for HfO₂ deposition. This fact was verified from the AFM images that the uniform and smooth morphology was achieved on the surface of this layer. Investigation of electrical properties revealed that n , Φ_{Bo} , R_s , Z and phase angle of the MIS diode depend on both applied voltage and temperature. The decrease in n value with increasing temperature was found to be in a direct relation with particular distribution of interface states and insulator layer between metal and semiconductor. Incremental Φ_{Bo} values with increasing temperature and reduction in n values with increasing temperature can be evaluated as an indication of deviation from TE theory. In addition, C , G and R_s were observed in decreasing behavior with decreasing temperature. At this point, Z decreases with increasing temperature. The MIS diode behaves more capacitive in the bias voltage range of -3 V and about 0.4 V. In addition, D_{it} , Q_{eff} and N_{eff} values of the MIS diodes were decreasing with increasing temperature over temperature range 60 – 320 K.

References

- B.L. Sharma, *Metal-Semiconductor Schottky Barrier Junctions and Their Applications* (Plenum Press, New York, 1984)
- Y. Jiao, A. Heliman, Y. Fang, S. Gao, M. Kall, *Sci. Rep.* **5**, 11374 (2015)
- I.A. Digdaya, B.J. Trzesniewski, G.W.P. Adhyaksa, E.C. Garnett, W.A. Smith, *J. Phys. Chem. C* **122**, 5462 (2018)
- M. Uma, N. Balaram, P.R.S. Redd, V. Janardhanam, V. R. Reddy, H-J. Yun, S.-N. Lee, C-J. Choi., *J. Elect. Mater.* **48**(7), 4217 (2019).
- H.H. Gullu, D.E. Yildiz, *J. Mater. Sci: Mater. Electron.* **30**, 19383 (2019)
- D.A. Muller, T. Sorsch, S. Moccio, F.H. Baumann, K. Evans-Lutterodt, G. Timp, *Nature* **399**, 758 (1999)
- A. Tataroglu, *Microelect. Eng.* **83**, 2551 (2006)
- A. Ashery, M.M.M. Elnasharty, *Silicon* **11**, 1875 (2019)
- S. Bengi, M.M. Bülbül, *Curr. Appl. Phys.* **13**, 1819 (2013)
- A. Karabulut, *Bull. Mater. Sci.* **42**(5), 1 (2019)
- J.H. Kim, V.A. Ignatova, P. Kucher et al., *Curr. Appl. Phys.* **9**, 104 (2009)
- J.H. Choi, Y. Mao, J.P. Chang, *Mater. Sci. Eng. R* **72**, 97 (2011)
- S. Rudenja, A. Minko, D.A. Buchanan, *Appl. Surf. Sci.* **257**, 17 (2010)
- J.B. Park, W.S. Lim, B.J. Park, I.H. Park, Y.W. Kim, G.Y. Yeom, *J. Phys. D Appl. Phys.* **42**, 055202 (2009)
- Yu Tao, C. Jin, X. Yang, Y. Dong, H. Zhang, L. Zhuge, Wu Xumei, *Wu Zhaofeng, Appl. Surf. Sci.* **258**, 2953 (2012)
- M.H. Cho, Y.S. Roh, C.N. Whang, K. Jeong, S.W. Nahm, D.H. Ko, J.H. Lee, N.I. Lee, K. Fujihara, *Appl. Phys. Lett.* **81**, 472 (2002)
- B.K. Park, J. Park, M. Cho, C.S. Hwang, K. Oh, Y. Han, D.Y. Yang, *Appl. Phys. Lett.* **80**, 2368 (2002)
- S. Sayan, S. Aravamudhan, B.W. Busch, W.H. Schulte, F. Cosandey, G.D. Wilk, T. Gustafsson, E. Garfunkel, *J. Vac. Sci. Technol. A* **20**, 507 (2002)
- Y. Wang, J. Zhang, G. Liang, Y. Shi, Y. Zhang, Z.R. Kudrynski, Z.D. Kovalyuk, A. Patane, Q. Xin, A. Song, *Appl. Phys. Lett.* **115**, 033502 (2019)
- B.H. Lee, L. Kang, R. Nieh, W.J. Qi, J.C. Lee, *Appl. Phys. Lett.* **76**, 1926 (2000)
- L. Kang, B.H. Lee, W.J. Qi, Y. Jeon, R. Nieh, S. Gopalan et al., *IEEE Electron Device Lett.* **21**, 181 (2000)
- S.Y. Lee, S. Chang, J.S. Lee, *Thin Solid Films* **518**, 3030 (2010)
- G. He, L.Q. Zhu, M. Liu, Q. Fang, L.D. Zhang, *Appl. Surf. Sci.* **253**, 3413 (2007)
- K.P. Bastos, J. Morais, L. Miotti, R.P. Pezzi, G. Soares, I.J.R. Baumvol, R.I. Hegde, H.H. Tseng, P.J. Tobin, *Appl. Phys. Lett.* **81**, 1669 (2002)
- S. Sayan, E. Garfunkel, S. Suzer, *Appl. Phys. Lett.* **80**, 2135 (2002)
- S. Altındal, A. Tataroglu, I. Dokme, *Sol. Energy Mater. Sol. Cells* **85**, 345 (2005)
- P. Chattopadhyay, B. Raychaudhuri, *Solid State Electron.* **35**, 605 (1993)
- J. Shewchun, M.A. Geen, F.D. King, *Solid State Electron.* **17**, 563 (1974)
- F. Hirose, Y. Kinoshita, K. Kanomata, K. Momiyama, S. Kubota, K. Hirahara, Y. Kimura, M. Niwano, *Appl. Surf. Sci.* **258**, 7726 (2012)
- K.Y. Lee, W.C. Lee, M.L. Huang, C.H. Chang, Y.J. Lee, Y.K. Chiu, T.B. Wu, M. Hong, R. Kwo, *J. Cryst. Growth* **301–302**, 378 (2007)
- L. Khomenkova, X. Portier, J. Cardin, F. Gourbilleau, *Nanotechnology* **21**, 285707 (2010)
- A. A. Sokolov, E. O. Filatova, V.V. Afanas'ev, E.Y. Taracheva, M.M. Brzhezinskaya, Ovchinnikov, *J. Phys. D-Appl. Phys.* **42**, 035308 (2009).
- M.S.P. Reddy, P. Puneetha, V.R. Reddy, J.H. Lee, S.H. Jeong, C. Park, *J. Electron. Mater.* **45**, 5655 (2016)
- D.A. Aldemir, A. Kökce, A. F. Özdemir, *Bull. Mater. Sci.* **40**, 1435 (2017)
- K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen, M. Leskela, *Thin Solid Films* **416**, 72 (2002)
- N. Biyikli, A. Karabulut, H. Efeoglu, B. Guzeldir, A. Turut, *Phys. Scr.* **89**, 095804 (2014)
- F. Ozdemir, A. Kokce, A. Türüt, *Appl. Surf. Sci.* **191**, 188 (2002)
- M. Biber, C. Temirci, A. Türüt, *J. Vac. Technol. B* **20**(1), 10 (2002)
- V. Budhruja, D. Misra, *ECS Trans.* **16**(5), 455 (2008)
- O. Kahveci, A. Akkaya, E. Ayyildiz, A. Turut, *Surf. Rev. Lett.* **24**, 1750047 (2017)
- W.B. Bouiadjra, A. Saidane, A. Mostefa, M. Henini, M. Shaf **71**, 225 (2014)
- Y. Wang, Y. Wang, L. Li, Y. Zhao, G. Feng, X. Wang “Research on rapid thermal annealing of ohmic contact to GaAs” International Conference on Optoelectronics and Microelectronics (ICOM), 23–25 Aug, 2012.
- S.Y. Moon, J.H. Son, K.J. Choi, J.L. Lee, *Appl. Phys. Lett.* **99**, 202106 (2011)
- D.W. Davies, D.V. Morgan, H. Thomas, *Semicond. Sci. Technol.* **14**, 615 (1999)
- A. Karabulut, H. Efeoglu, A. Turut, *J. Semicond.* **38**(5), 054003 (2017)

46. G.Y. Robinson, *Physics and Chemistry of III–V Compound Semiconductor Interfaces*, ed. by C. W. Wilmsen, (Plenum Press, New York, 1995).
47. K. Kolanek, M. Tallarida, M. Michling, D. Schmeisser, J. Vac. Sci. Technol. A **30**(1), 01A143 (2011)
48. S.-J. Jeong, Y. Gu, J. Heo, J. Yang, C.S. Lee, M.H. Lee, Y. Lee, H. Kim, S. Park, Hwang Sci. Rep. **6**, 20907 (2016)
49. A. Christou, W.M. Web “Reliability of Compound Analogue Semiconductor Integrated Circuits” RIAC, University of Maryland, New York
50. W. Gao, P.R. Berger, R.G. Hunsperger, G. Zydzik, W.W. Rhodes, H.M. O’Bryan, D. Sivco, A.Y. Cho, Appl. Phys. Lett. **66**, 3471 (1995)
51. I.B. Chistokhin, M.S. Aksenov, N.A. Valisheva, D.V. Cmitriev, A.P. Konchavtsev, A.K. Gutakovskii, I.P. Prosvirin, K.S. Zhuravlev, Mater. Sci. Semicond. Process. **74**, 193 (2018)
52. V.R. Reddy, Y.M. Reddy, R. Padmasuvarna, T.L. Narasappa, Procedia Mater. Sci. **10**, 666 (2015)
53. H.H. Gullu, D.E. Yildiz, A. Kocyigit, M. Yildirim, J. Alloy Compd. **827**, 154279 (2020)
54. V. Janardhanam, H.K. Lee, K.H. Shim, H.B. Hong, S.H. Lee, K.S. Ahn, C.J. Choi, J. Alloys Compd. **504**, 146 (2010)
55. S. Altındal, H. Kanbur, D.E. Yıldız, M. Parlak. Appl. Surf. Sci. **253**, 5056 (2007)
56. A. Bengi, S.J. Jang, C.I. Yeo, T. Mammadov, S. Ozcelik, Y.T. Lee, Solid State Electron. **61**, 29 (2011)
57. I.S. Yahia, M. Fadel, G.B. Sakr, F. Yakuphanoglu, S.S. Shenouda, W.A. Farooq, J. Alloy. Compd. **509**, 4414 (2011)
58. D.E. Yildiz, H.H. Gullu, A. Sarilmaz, F. Ozel, A. Kocyigit, M. Yildirim, J. Mater. Sci **31**, 935 (2020)
59. C.R. Crowell, Solid State Electron. **8**, 395 (1965)
60. P. Chattopadhyay, J. Phys. D **29**, 823 (1996)
61. S.K. Cheung, N.W. Cheung, Appl. Phys. Lett. **49**, 85 (1986)
62. H. Saghrouni, S. Jomni, W. Belgacem, N. Hamdaoui, L. Beji, Phys. B **444**, 58 (2014)
63. M. Fanciulli, G. Scarel, *Rare Earth Oxide Thin Film: Growth, Characterization, and Applications* (Springer, Berlin, 2007)
64. M. Wu, Y.I. Alivov, H. Morkoc, J. Mater. Sci. **19**, 915 (2008)
65. H. Kim, Y. Cho, D.-W. Kim, D.H. Kim, Y. Kim, B.J. Choi, J. Korean Phys. Soc. **73**(3), 349 (2018)
66. M. Soylu, B. Abay, Microelectron. Eng. **86**, 88 (2009)
67. D.A. Aldemir, A. Kökce, A.F. Özdemir, Sakarya Univ. Inst. Sci. J. **21**(6), 1286 (2017)
68. E.H. Roderick, R.H. Williams, *Metal-Semiconductor Contacts* (Clarendon, Oxford, 1988)
69. Ş. Altındal, S. Karadeniz, N. Tugluoglu, A. Tataroglu, Solid-State Electron. **47**, 1847 (2003)
70. A. Sing, Solid-State Electron. **28**, 223 (1985)
71. B. Akkal, Z. Benamara, B. Gruzza, L. Bideux, Vacuum **57**, 219 (2000)
72. P. Ozdag, *Capacitance-Voltage Spectroscopy in Metal-Tantalum Pentoxide (Ta2O5)-Silicon MOS Capacitors* (Izmir Institute of Technology, Izmir, 2005)
73. F. Yigiterol, H.H. Gullu, O. Bayrakli, D.E. Yıldız, J. Electron. Mater. **47**(5), 2979 (2018)
74. F.M. Coşkun, O. Polat, M. Coşkun, A. Turut, M. Caglar, Z. Durmus, H. Efeoğlu, J. Appl. Phys. **125**, 214104 (2019)
75. S. Mahato, RSC Adv. **7**, 47125 (2017)
76. B. Sahin, H. Cetin, E. Ayyıldız, Solid State Commun. **135**, 490 (2005)
77. P. Chattopadhyay, S. Sanyal, Appl. Surf. Sci. **89**, 205 (1995)
78. A. Tataroglu, Ş. Altındal, Y. Azizian-Kalandaagh, Phys. B: Cond. Matter. **582**, 411996 (2020)
79. S.M. Sze, *Physics of Semiconductor Devices*, 2nd edn. (Wiley, New York, 1981)
80. D.E. Yıldız, J. Mater. Sci. **29**(20), 17802 (2018)
81. C.H. Kim, O. Yaghmazadeh, D. Tondelier, Y.B. Jeong, G. Yvan Bonnassieux, Horowitz. J. Appl. Phys. **109**, 083710 (2011)
82. H.H. Gullu, O. Bayrakli Surucu, M. Terlemezoglu, D.E. Yildiz, M. Parlak, J. Mater. Sci. **30**, 9814 (2019)
83. H. Dogan, N. Yıldırım, I. Orak, S. Elagöz, A. Turut, Phys. B **457**, 48 (2015)

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