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Dark and illuminated electrical characteristics of Si-based photodiode interlayered with $CuCo_5S_8$ nanocrystals

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Abstract

Derived from the traditional dichalcogenide CuS structure, ternary transition metal chalcogenide nanoparticles in the form of $CuCo_5S_8$ are investigated under the aim of photodiode application. In addition to the detailed analysis on material characteristics of $CuCo_5S_8$ thin-film layer, the work is focused on the electrical characteristics of Au/$CuCo_5S_8$/Si diode to investigate its current–voltage, capacitance–voltage, and conductance–voltage characteristics under dark and illuminated conditions. $CuCo_5S_8$ nanocrystals with an average size of 5 nm are obtained using hot-injection method, and they are used to form thin-film interfacial layer between metal (Au) and semiconductor (Si). Under dark conditions, the diodes show about four orders in magnitude rectification rate and diode illumination results in efficient rectification with increase in intensity. The analysis of current–voltage curve results in non-ideal diode characteristics according to the thermionic emission model due to the existence of series resistances and interface states with interface layer. The measured current–voltage values are used to extract the main diode parameters under dark and illumination conditions. Under illumination, photogenerated carriers contribute to the current flow and linear photoconductivity behavior in photocurrent measurements with illumination shows the possible use of $CuCo_5S_8$ layer in Si-based photodiodes. This characteristic is also observed from the typical on/off illumination switching behavior for the photodiodes in transient photocurrent, photocapacitance, and photoconductance measurements with a quick response to the illumination. The deviations from ideality are also discussed by means of distribution of interface states and series resistance depending on the applied frequency and bias voltage.

1 Introduction

Chalcogenides are an extraordinarily interesting group of semiconductor compounds in a wide variety of electronic and optoelectronic applications [1, 2]. In the photovoltaic area, thin-film technologies based on this type of compounds have been grown faster in competition with the conventional wafer-based solar cells [3]. It is mostly related to the economical point of view where the use of these compounds can offer less requirement of source material and also simpler fabrication processes with respect to the traditional solar cell technologies. Together with the ternary compound chalcogenide $CuInSe_2$ as a pioneer in this field, ternary and quaternary Cu chalcogenides have gained great interest for various applications, especially in photovoltaics due to their promising material properties for thin-film devices under solar radiation [4–6]. On the other hand, recent development in the photovoltaic area has been directed to new and better technologies with increasing demand for cheap device applications. In order to fulfill the future demand of solar cells, non-toxic, earth-abundant, and low-cost elements attract

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significant interest as an alternative material for the rare elements in the well-known chalcogenide structures [6–8]. Similar to the process in these p–n junction photovoltaic devices, photodiodes have also a potential to be used in solar light conversion to current with having a depletion region to separate photogenerated carriers in a high electric field. Therefore, in place of semiconductor/semiconductor heterojunctions, metal/semiconductor (Schottky) junctions are also used with interfacial layers to gain superior properties for many applications. Metal–semiconductor type diodes are used in many electronic devices, and their electrical properties can be tuned for specific applications by a native insulator layer at the interface and/or an extrinsic interfacial layer stacked between metal and semiconductor [9, 10]. Performance and reliability of these Schottky-type diodes depend on the formation of an interfacial layer and its effects on the diode as the interface states distribution at the interfacial layer and the semiconductor, and inhomogeneous barrier heights together with parasitic resistances. In this approach, in addition to the novel material of SiO_2, insulator layer of semiconductor substrates, especially low-dielectric insulator layers such as SnO_2, TiO_2, and Si_3N_4, gain importance as potential materials in such applications [11–17]. Due to the open problems in passivation of the active dangling bonds at the semiconductor surface, several inorganic and organic interfacial layers have been employed to improve and also tune their electronic characteristics of these devices [16–18]. In this field, chalcogenide nanocrystals present new developments with material engineering on their optical and electrical properties with size and shape variations that cannot be achieved with changing composition and surface characteristics of their thin-film counterparts [19–21]. Potential optical characteristics in solar light absorption and high charge carrier functionalities in optoelectrical applications make Cu chalcogenide nanocrystals particularly suitable materials for photodiodes [21].

Ternary transition metal chalcogenides offer great potential in a variety of applications including photovoltaic devices and photodetectors, and their nanocrystals gain high level of interest due to superior electrical and optical properties [21–23]. Under the aim of future applications, these materials have presented many research opportunities in low-cost and large-area compatibilities together with preferable energy conversion efficiency and device stability [23]. There are several methods to synthesize these nanocrystals such as solvothermal, hydrothermal, and hot-injection methods [22, 24, 25]. On the other hand, they can be deposited in monolayer form using several techniques such as atomic layer deposition and atomic layer chemical vapor deposition [21, 26, 27]. They are generally used in the diodes as a thin-film layer at the interface, and in this process, several methods such as vacuum evaporation, chemical vapor deposition, and solution-based techniques are used [21]. Among these methods, low-cost solution-based technologies have motivated interest in the deposition of nanocrystals on substrates [21, 28–30]. In the hot-injection synthesis method, which is one of the colloidal nanocrystalline production methods, nanocrystals are obtained by degradation of the compounds that make up this material in surfactants and/or organic solvents. In this method, the particle size, shape, and composition of the particles can be controlled [29, 30]. In addition, homogeneous size distribution and good crystallinity can be achieved in this method. However, there are a few disadvantages, such as the difficulty in developing procedures suitable for commercial production and the use of relatively expensive chemicals.

In this study, the electrical characteristics of the metal (Au)/semiconductor (Si) diode with Cu-based nanocrystal interfacial layer were investigated. This layer was deposited using $CuCo_5S_8$ nanocrystals synthesized by hot-injection method with the advantages of easy processing and control in order to obtain high-quality and low-cost materials. These nanocrystals were adopted to the diode as an interfacial layer in the thin-film form deposited on Si surface by spin-coating technique. Derived from the dichalcogenide CuS structure, ternary transition metal chalcogenide nanoparticles in the form of CuX_2S_4 and their alternatives in different elemental ratios have gained research interest with their effective optical and electronic characteristics [28, 29, 31–33]. In this case, the development in this area has been concentrated on the use of transition metals such as Co, W, and Ni in these compounds to improve the charge storage characteristics of the diodes [33–35]. Therefore, as a member of this family, the work was focused on the diode characteristics of Au/$CuCo_5S_8$/Si diode to investigate its current–voltage (I–V), capacitance–voltage (C–V), and conductance–voltage ($G/\omega - V$) characteristics under dark and illuminated conditions.

2 Experimental details

The synthesis of $CuCo_5S_8$ nanocrystals was carried out in 1-octadecene (ODE, 90% tech) by the hot-injection method. To synthesize nanocrystals, $(Cu(CO_2CH_3)_2$ and $Co(CO_2CH_3)_2$ chemicals with different purities, 99.995% and 99.99%, were used in 0.2 mmol and 1 mmol, respectively. This solution of $Co(Ac)_2$ was mixed with 10 ml ODE in a 25-mL two-necked, round-bottomed flask and heated to 210 °C with magnetic stirring under argon flow. When the reaction medium was reached to 120 °C, freshly prepared S-precursor solution (0,125 mL 1-dodecanethiol (DDT, 98%) and 0.875 ml tert-dodecanethiol (t-DDT, 98%)) were rapidly injected into the hot reaction mixture under vigorous stirring. Under these conditions, the reaction was continued for 30 min and cooled down to room temperature. Finally,

the nanorods were precipitated adding a mixture of ethanol and toluene (99%) and centrifuged at the rate of 3000 r/min for 1 min.

The cleaning procedure of (100) p-type Si wafer was carried out by shaking it in acetone and propanol by an ultrasonic cleaner, separately. After that, Si wafer was immersed in HF/H_2O (1:1) solution to remove impurities and native oxide layer from its surface. A 100-nm-thick Al layer was thermally evaporated to the back surface of the wafer as an ohmic contact, and it was annealed for 5 min in N_2 atmosphere at 500 °C to enhance its ohmic contact behavior. The synthesized $CuCo_5S_8$ solution was deposited on the front surface of the semiconductor substrate as in 180-nm thin-film form by a spin coater. In order to complete the diode structure, Au rectifying contact was thermally deposited on the front surface of $CuCo_5S_8$/p-Si using Au trace metals (99.99%).

Figure 1a, b shows transmission electron microscope (TEM) images of the as-synthesized nanocrystals. Figure 1a, b clearly shows that the nanocrystals have non-homogeneous size and shape distribution. The average sizes of the $CuCo_5S_8$ nanocrystals are about 5 nm with a standard deviation of 1.5 nm. In addition, high-resolution TEM (HR-TEM) analysis was performed to further confirm the crystallinity and structure of the nanocrystals. Figure 1c shows HR-TEM images of the nanoparticles, and the lattice fingers of the nanocrystals reveal their highly crystalline nature. The interplanar spacing of $CuCo_5S_8$ was measured and found to be 2.36 Å. These can be attributed to the (400) crystallographic planes. The selected area electron diffraction (SAED) patterns agree well with the structure of the $CuCo_5S_8$ as shown in Fig. 1d. The polycrystalline SAEDs are indexed with rings to (511), (551), and (822). As shown in this figure, the diffraction rings are discontinuous and consist of sharp spots, which indicate that the nanocrystals are well crystallized. Figure 1e, f shows the typical field emission scanning electron microscope (FE-SEM) images of these nanoparticles. As shown in these images, the nanocrystals exhibit agglomerated morphology. Figure 1g displays the elemental mapping images for the $CuCo_5S_8$ structures. As revealed by Fig. 1g, the distributions of the transition metals (Co and Cu) and S in the $CuCo_5S_8$ are well in accordance with the element profiles. These results clearly emphasize that highly homogeneous $CuCo_5S_8$ structures are achieved by the use of hot-injection method.

Powder X-ray diffraction (XRD) analysis was employed to investigate the crystallographic structure of the $CuCo_5S_8$ nanocrystals. Figure 2a displays the XRD pattern of the synthesized nanocrystals. The pronounced peaks at 26.6, 31.3, 38.0, 47, 50, and 54.8 correspond to the (022), (113), (004),

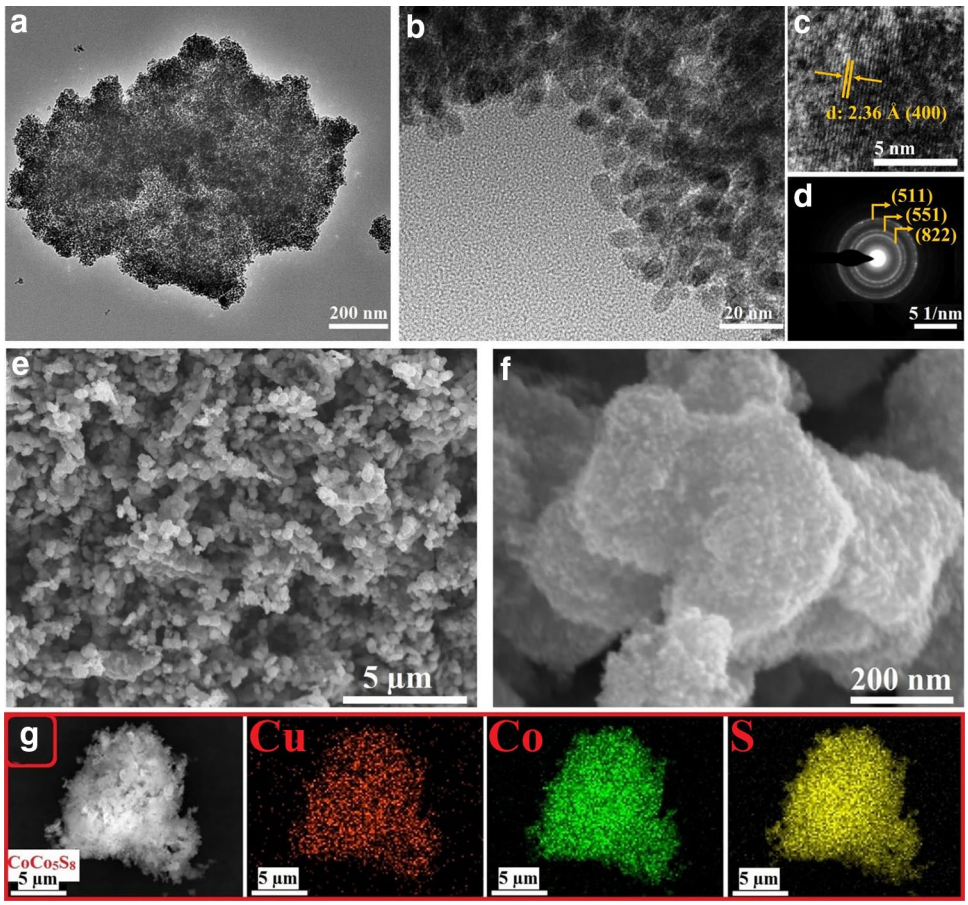

Fig. 1 **a**, **b** TEM, **c** HR-TEM, and **d** SAED, **e, f** SEM, and **g** elemental mapping images of the $CuCo_5S_8$ nanocrystals

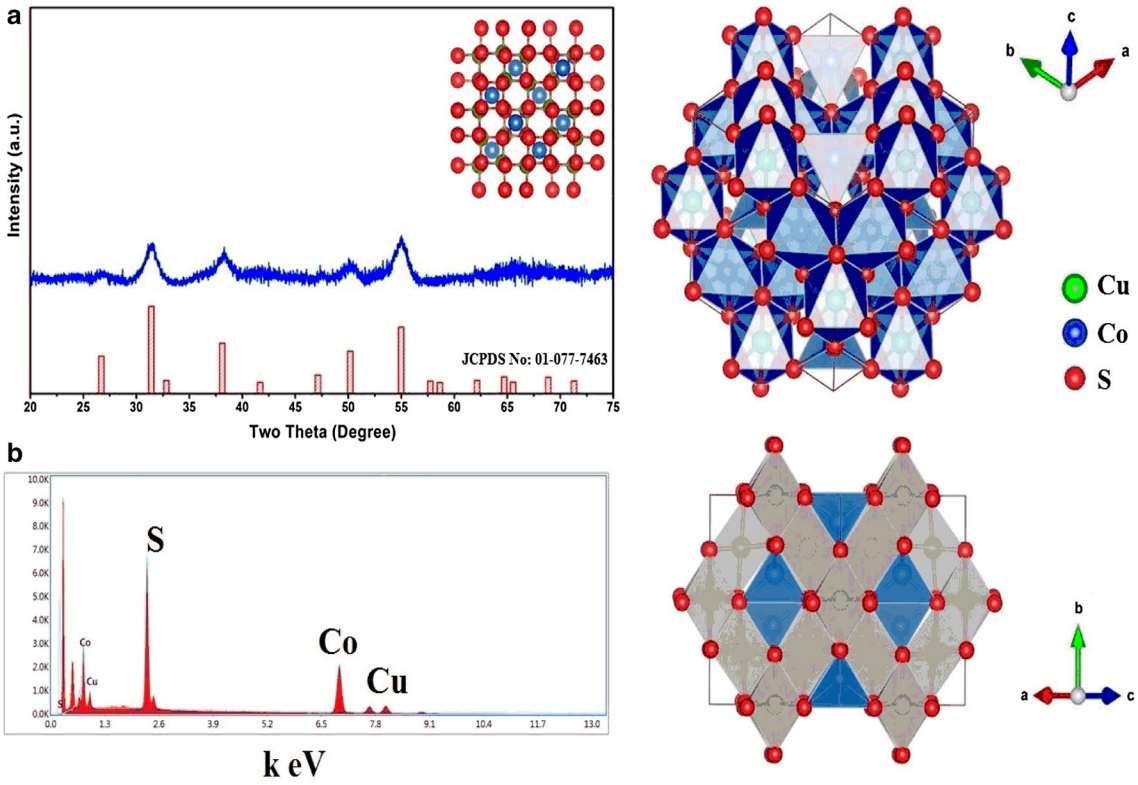

Fig. 2 **a** X-ray diffraction pattern, **b** EDX pattern, and corresponding crystal structure of the $CuCo_5S_8$ nanocrystals

(224), (115), and (044) planes of the Cu–Co–S structure, respectively. All diffraction peaks match well with the cubic structured Cu–Co–S (JSPDS No. 00.77-7463). The XRD result was also used to estimate the nanoparticle diameter, using the Scherrer's equation analysis of the strongest XRD peak at 55° revealed an average diameter of 5 nm, in reasonable agreement with that obtained from SEM and TEM measurements [36]. In addition, the energy-dispersive X-ray spectroscopy (EDS) spectrum includes all constituent elements of the final structure, and it confirms the stoichiometry of $CuCo_5S_8$ (Fig. 2b).

The *I–V* characteristics of fabricated photodiodes were measured using a FYTRONIX 7000 solar simulator which adjusts the light intensity automatically from 20 to 100 mW/cm^2 under cold light lamp. The $C-V$ and $G/\omega-V$ measurements were performed by a computer-controlled Keithley 4200 semiconductor characterization system.

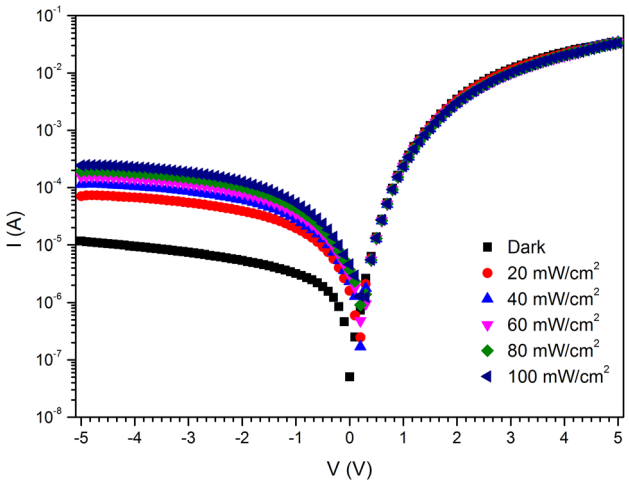

Fig. 3 *I–V* characteristics of the Au/$CuCo_5S_8$/Si diode under dark and illumination with different illumination intensities

3 Results and discussion

Diode characteristics of the Au/$CuCo_5S_8$/Si diode are investigated by room-temperature *I–V* measurements under dark and different solar illumination intensities in the range of 20–100 mW/cm^2. In Fig. 3, diode shows a rectifying behavior where current can flow in the forward-bias region; however, the diode blocks the reverse current transport. It is the indication of good rectifying behavior with four orders of magnitude rectification rate of forward- and reverse-biased currents (RR). On the other hand, there is no remarkable change in forward current value under solar illumination. RR

of the diode decreases with an increase in light intensity due to the increase in the reverse-bias current values, and it can be occurred due to the possible contribution of photogenerated charge carriers to the dark current under illumination [37]. The increase in the carrier concentration because of the generation of electron–hole pairs at the interface is the indication of the photoconducting behavior of the diode, and this light response with good rectifying behavior can be used in the photodiode applications [38, 39]. The sensitivity to light is comparable with previous works on different photodiodes based on Au/Si in terms of change in the current values, especially in reverse-bias region [29, 40]. Although this response is the indication of capacity to be used in photodiode applications, the barrier occurred at the interface to the current flow, and photoinduced carriers from the localized trap states possibly in the interface layer that contribute to the flow can be the reason of the low response in the forward region. The observed *I–V* characteristics under illumination is directly related to the Schottky diode barrier between the rectifying Au contact and the semiconductor Si layer, and also the possible effects of $CuCo_5S_8$ layer at the interface. The low response at the forward-bias region can be attributed to the interface layer characteristics where the existence of it at the interface change the junction barrier together with its bulk resistance, structural defects, and interface states, whereas these states can increase the tunneling current at the reverse-bias region [41, 42]. In addition, the weak absorption characteristics of the interface layer can be attributed to this low response compared to the diodes including semiconducting interface film layers [40, 42].

According to the thermionic emission (TE) model, the forward-biased *I–V* behavior of the diode can be expressed as:

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{1}$$

where the variations on the TE currents (I) flowing from the metal to semiconductor at barrier depletion are neglected [9, 10]. Based on the rectifying behavior of the diode, the electrical parameters as saturation current (I_0), ideality factor (n), and barrier height (Φ_b) can be extracted using this relation. The other parameters in Eq. (1) are electronic charge q, Boltzmann constant k, and absolute temperature T in Kelvin unit. In this relation, n is named as the ideality factor for an ideal Schottky barrier, and it is assumed to be independent of V [12, 43]. Therefore, pure TE indicates that I flows only due to TE of carriers with the case of $n = 1$. In the ideal Schottky diodes, this mechanism can be assumed with defect-free interface between metal and semiconductor, and the deviation from linearity in logarithmic *I–V* curve can only be attributed to series resistance (R_s). As a common evaluation, this transport method can be applied to the ohmic region where the measured current values are in expected linear behavior. This characteristic can also be observed as an experimental result for the Au/n-Si/Al Schottky diodes where *I–V* data conform with ideal TE as a dominant transport mechanism [44]. Although it can be expected as a dominant factor in the transport mechanism of the diodes with weak deviations from the ideal case neglecting the other contributions by the different mechanisms, *I–V* characteristics can be found in different transport mechanisms in the conduction with larger n values [9, 43]. Considering the ideal interface-free diode structure, the possible shift in the work function of the rectifying metal and also in the electron affinity of the active semiconductor layer under the effect of interfacial layer formation at the metal–semiconductor interface can be resulted in such deviations [45, 46]. Considering the limit of V, where $V > 2kT/q$ in order to eliminate possible effects of reverse current contribution, Eq. (1) is modified as [43]:

$$I = I_0\exp\left(\frac{qV}{nkT}\right) \tag{2}$$

According to Eq. (2), linearity in the forward-bias *I–V* relation (Fig. 3), where TE of majority carriers in the diode is dominant in the carrier diffusion, can be used to extract the main diode parameters [9, 44]. From the intercept of this straight line in the ln(I) versus V graph (Fig. 3) at zero-bias point, the I_0 value is found as 2.62×10^{-7} A and listed in Table 1. It is the parameter related to the reverse current occurring by the diffusion of the minority charge carriers. This behavior is formulated in the Schottky-type diodes as:

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_b}{kT}\right), \tag{3}$$

where I_0 is expected to be almost independent of the reverse-bias voltage, and the parameters A is the active diode area defined by the Au–metal contact region on top of the $CuCo_5S_8$ layer (3.14×10^{-2} cm^2), and A^* is the effective Richardson constant of the active semiconducting layer with the assumption of uniform barrier height formation

Table 1 Diode parameters under dark and illumination conditions

Condition	I_0 ($\times10^{-7}$ A)	n	Φ_b (*I–V*) (eV)	Φ_b (Cheung) (eV)
Dark	2.62	6.72	0.687	0.670
20 mw/cm^2	1.79	5.70	0.697	0.684
40 mw/cm^2	1.39	5.42	0.704	0.701
60 mw/cm^2	1.05	4.74	0.711	0.717
80 mw/cm^2	0.79	4.25	0.719	0.721
100 mw/cm^2	0.75	3.82	0.720	0.732

(32 A/cm^{2}K^2 for the p-Si) [9, 47]. Introducing the obtained I_0 to Eq. (3), apparent Φ_b value at zero bias is calculated as 0.69 eV. Compared to the literature works on Au/p-Si Schottky diodes, it is higher than the reported values of 0.33 eV [43] and 0.34 eV [48] where difference in deposition methods and/or deposition conditions may cause this small difference between these values. It was also studied in Au/n-Si form; however, the obtained values are higher than the ones found using p-Si [13, 44]. This occurred because barriers on p-type semiconductors are generally lower than those on n-type of the same semiconducting material [48]. Thermal deposition of Au metal on p-Si can also be effective in this barrier formation where the existence of the defects on the Si surface, and its effects to the effective barrier height of Si in the Au/p-Si Schottky barriers can be evaluated as the possible reasons for different barrier heights [49]. In a metal–semiconductor diode, the band gap of the semiconductor is the dominant factor in the formation of the barrier height and the existence of natural and/or deposited interface layer can affect the value of barrier height [44]. At this point, free carrier concentration and better conductivity of the p-Si layer compared to $CuCo_5S_8$ layer indicates the dominant effect of p-Si layer on the current flow mechanism in the diode [38, 50]. The value of Φ_b derived from $CuCo_5S_8$ interlayered Au/p-Si diode is in a good correlation with the similar comparisons between Au/p-Si structure with and without oxide/dielectric/insulator interface layer [13, 41, 42, 46]. The increase in Φ_b with $CuCo_5S_8$ layer can be the result of increasing charge carriers at the interface due to the existence of localized trap states at the semiconductor interface [13]. Additionally, in most of the cases, it is in the range of the reported values for different interface layers such as α-PbO_2 [40], FePc [41], InP quantum dots [42], and several other organic layers [46, 51]. The observed barrier height between Au metal and Si semiconductor with interface film layer can be also evaluated in the same electrical response of Au/n-Si together with different interface layers such as TiO_2 [14], SnO_2 [52], Si_3N_4 [13], and SiO_2 [53]. On the other hand, as compared to the effect of Cu_2WSe_4 nanosheet layer, the obtained value is smaller than the reported one as 0.82 eV even if both are in nanostructural form [29].

In addition to Φ_b, n is calculated as the main diode parameter from the slope of linear region in the forward-biased semilogarithmic I–V plot (Fig. 3) as:

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln(I)}\right), \tag{4}$$

and it is found as to be 6.72, which is greater than unity. It can be evaluated as one of the highest values in Au/p-Si-based Schottky diodes with an intentional interlayer. Although the values are expected to be in the range of 1–2 for the applicability of TE mechanism [40, 42, 46], there are higher values ($n > 2$) in the literature, as being observed in the present work, depending on the structural differences in the interface layers [41, 51]. This larger value indicates the bias dependence of Φ_b depending on the non-ideal I–V behavior in the diode [7, 54]. It can be related to the presence of R_s, image force effects, electron tunneling at the interface, non-uniform distribution of the carriers in the interface, carrier recombination within the depletion region, inhomogeneities in Φ_b depending on possible interface states in the junction, and native interface layer between metal and semiconductor separation [52–55]. The current across the Au/Si can be greatly influenced by the existence of barrier inhomogeneity depending on the possible low-barrier patches distributed at the Au/Si interface [45, 46, 55]. This fact is reported in several works as being the deviation from the ideality and the observed barrier homogeneity is explained by the possible shift in the work function of Au and in the electron affinity of Si under the effect of interface layer in the metal–semiconductor junction region [46]. In addition to giving excess barrier to the charge transport, this deviation from ideality can result in different carrier mechanisms dominant in different bias regions [13]. Within the junction, the diode can operate under the possible effects of generation–recombination currents within the space-charge region contributing to TE current conduction mechanism [7, 56]. Deviation from ideality with the observed n values can be also attributed to the secondary carrier transport mechanism in addition to TE where lateral inhomogeneous distribution of barrier heights due to the existence of interface layer and also interface defect dominant in the current flow [53]. Based on the TE theory, this type of abnormal I–V characteristics can be explained Gaussian distribution of the system of discrete regions imbedded in a uniform barrier [13, 14, 53].

The I–V plots of the diode under different solar illumination intensities from 20 to 100 mW/cm^2 are given in Fig. 3. The increments in the reverse-bias current value with illumination and direct proportionality with the illumination intensity can be attributed to the effects of photogenerated carriers in the interface [29]. In fact, change in the electrical response of the Au/p-Si diode with interface layer, and as a result, barrier height modification due to the effect of localized charge carriers at the interface trap states can be related to this observation in the photoresponse of the diode [40, 42]. In addition to the dark analysis, electrical parameters given in Eq. (2) are extracted for the illumination conditions and the results are tabulated in Table 1. As listed in this table, it is found that there is a decrease in n to 3.82, whereas an increase in Φ_b to 0.72 eV was observed. Therefore, the illumination response and carrier transport process across the diode can be explained by the dominant effect of photogenerated carriers together with the decrease in recombination of the electron–hole pairs due to the presence of interface layer [29, 56].

The expression given in Eq. (2) is the case of TE regardless of the effect of R_s; however, the saturation behavior at high-forward-bias region is related to the dominant effect of R_s in the current flow. Therefore, the general equation in Eq. (1) can be modified by changing the voltage V across the diode in the exponential relation as $qV - IR_s$, where IR_s term is the voltage drop under the effect of R_s according to the Cheung and Cheung method [57]. The method is proposed the saturation region where $V > 3kT/q$ and revised the diode equation as:

$$I = I_0\left[\exp\left(\frac{qV - \mathrm{IR_s}}{nkT}\right) - 1\right] \tag{5}$$

It is an alternate approach to determine R_s values corresponding to Norde (proposed for $n = 1$ case) and Sato and Yasumura (for the $n > 1$ case) in the differential form as [57–59],

$$\frac{dV}{d\ln(I)} = \mathrm{IR_s} + n\frac{kT}{q} \tag{6}$$

This relation directs the use of $dV/d\ln(I)$ versus I plots and the current-dependent junction in the form as,

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{1}{AA^*T^2}\right) \tag{7}$$

where $H(I) = \mathrm{IR_s} + n\Phi_b$. The results obtained from the analysis of both $dV/d\ln(I)$ and $H(I)$ functions are shown in Fig. 4a, b, respectively. The straight lines observed from these plots are modeled by a linear fitting process. As a result, the calculated Φ_b values are given in Table 1 and also R_s values obtained from both of the linear plots are shown in Fig. 4c with respect to the dark and illumination conditions. Under dark, the values are about 150–200 Ω that can be feasible in possible photodiode applications [29], and this value is in the same order of magnitude with the other reported diodes based on Au/p-Si with an insulator/oxide layer [46, 51]. However, in comparison with metal–semiconductor structure, this resistance value is expected to be higher than the value without interface layer [13]. It can be due to the possible natural resistance to the current flow with the existence of interface states and the possible change in current transport mechanism under the effect of a wide distribution of these states [13, 41]. There is a consistency in the Φ_b values with TE and Cheung approaches in the change of dark to illumination conditions and the slight difference can be attributed to the working range of bias voltage and also the effect of R_s [60]. On the other hand, use of both the Cheung functions gave consistent values in the same order of magnitude, and they are found to be quite sensitive to illumination intensity. As shown in Fig. 4c, there is a decrease in the R_s values with increasing illumination intensity under the effect of photogenerated carriers [61]. This photoresponse of the diode can be detailed with the photocurrent and illumination intensity relation as:

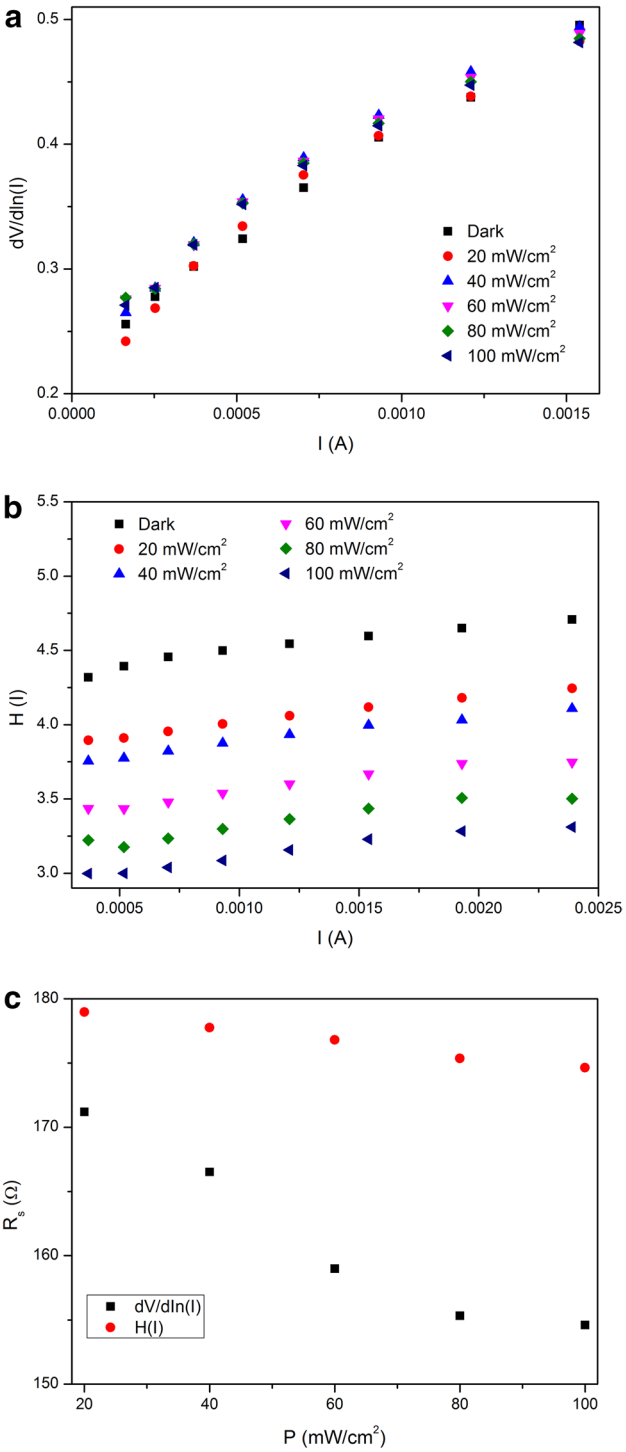

Fig. 4 R_s values derived from I–V results according to **a** $dV/d\ln(I) - I$ and **b** $H(I) - I$ analyses for different illumination conditions; **c** $R_s - P$ plot of the Au/$CuCo_5S_8$/Si diode

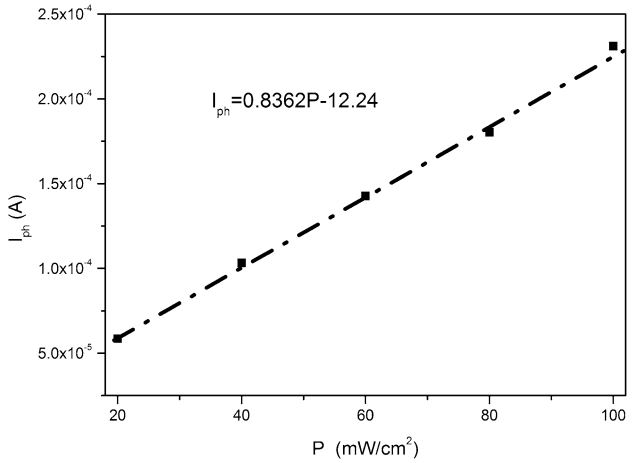

Fig. 5 $\ln(I_{ph})$ versus $\ln(P)$ plot of the Au/$CuCo_5S_8$/Si diode

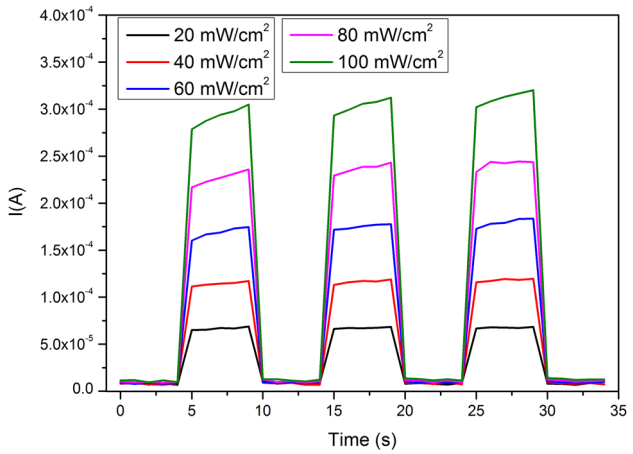

Fig. 6 $I(t) - V$ plots of the Au/$CuCo_5S_8$/Si diode

$$I_{ph} = BP^m \tag{8}$$

where I_{ph} is the photocurrent generated by solar light illumination on the diode, P is the applied illumination intensity, m is the illumination coefficient, and B is the proportionality constant [62]. The plot of $\ln(I_{ph})$ versus P is generated, and according to Eq. (8), the expected linear relation is achieved as shown in Fig. 5. The observed straight line behavior indicated the linear photoconductivity behavior, and therefore, photoconduction mechanism in the diode can be explained with the value of m [56, 62]. In this analysis depending on lifetime of the photocarriers, if the monomolecular recombination is dominant, it results in the case of $m = 1$. On the other hand, the higher values are originated from the low-density uninvaded trap levels. From the linear fitting process, this value is found to be 0.84 in $0 < m < 1$ interval. As a result, the existence and also continuous distribution of the localized states can be verified in the diode [52, 63].

Additionally, in order to discuss the photoconduction mechanism, the reaction time measurements are performed. The obtained results in transient I_{ph} measurements at constant −5 V bias are shown in Fig. 6 in the form of current–time ($I_{ph} - T$) depending on the applied illumination intensity. The plots as a response to each of the illumination conditions shows a quick response and I_{ph} values reach maximum value in about a second. The change in illumination intensity does not change the response time significantly, whereas it is observed that there is a direct relation between the peak value and illumination intensity. The recorded maximum I_{ph} value increases with increasing intensity. Due to the contribution of photogenerated carriers to the current flow and the increase in the concentration of the free charge carrier, high I_{ph} values can be obtained with intense illumination. Under continuous illumination, the observed certain I_{ph} values in each plot can be attributed to the possible tapping/detrapping of the charge carriers where these carries can be trapped by the defect states and re-excited from the other states to the conduction band [50, 64]. The transient plots are completed by following a typical on/off illumination switching process. During illumination, I_{ph} values increase in a very short time up to a certain level and the saturation condition is reached. Following a similar way in the illuminated case, after turning of the illumination, I_{ph} values return back to the initial value and the observed sudden decay can be related to the trapping carriers into the deep impurity levels [50].

In addition to the *I–V* analysis, the transient photocapacitance (C_{ph}) and photoconductance (G_{ph}) measurements are performed as a function of time in order to detail the effects of the photogenerated carriers. The corresponding plots at 100 kHz of frequency given in Fig. 7a, b. As in the illuminated *I–V* behavior, a strong illumination intensity dependence of C_{ph} and G_{ph} values is observed. During illumination, both of these values increase up to certain values under a similar approximation for the contribution of generated carriers to the conduction process [56]. Additionally, these values increase with the increase in illumination intensity and the highest values are obtained at the highest illumination intensity condition. After illumination is turned off, the values at maximum point decrease and drop back to their initial values possibly due to trapping of the charge carriers into the deep levels [56, 65].

Under dark and room conditions, the frequency-dependent capacitance–voltage (*C–V*) graph of the diode is shown in Fig. 8a. The data are collected between −4 and +4 V bias voltage and 10 kHz to 1 MHz frequency regions. In this plot, starting from the reverse-bias case, saturation capacitance values are observed in the high-reverse-bias region. With increasing frequency, these values increase and reach a maximum value at low-forward-bias region. On the other hand, increasing bias voltage in the forward-bias region causes a decrease in the capacitance values, and they

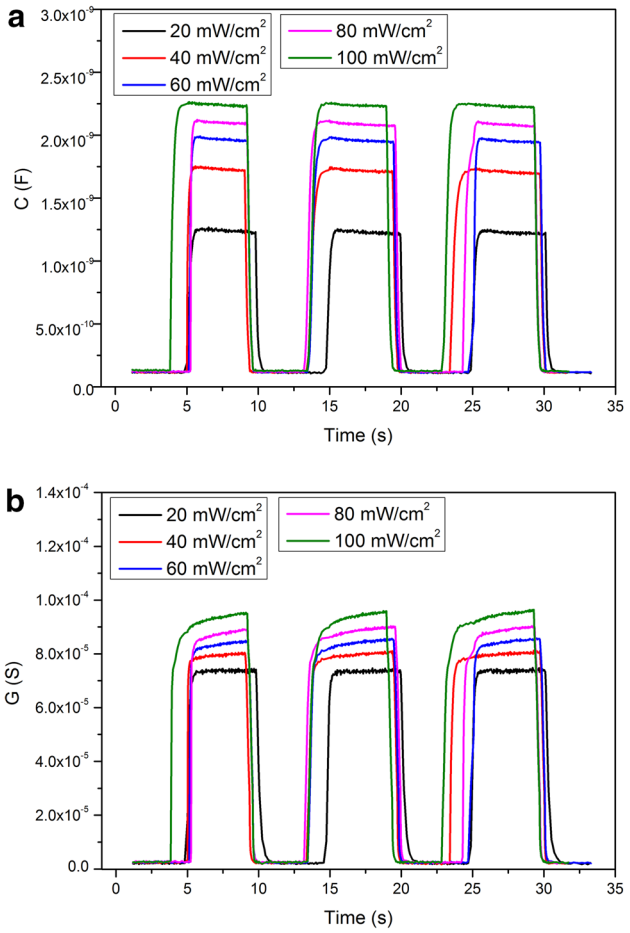

Fig. 7 **a** $C(t) - t$ and **b** $G(t) - t$ plots of the Au/$CuCo_5S_8$/Si diode

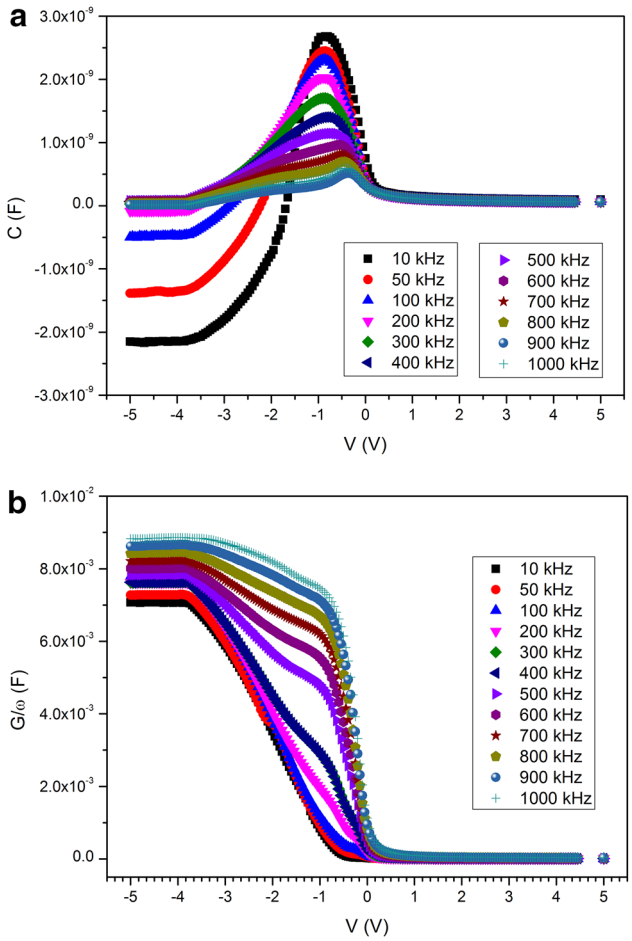

Fig. 8 Frequency-dependent (**a**) *C–V* and **(b)** *G–V* plots of the Au/$CuCo_5S_8$/Si diode

exhibit saturation behavior around the zero-capacitance point. Under the effect frequency, the values are low in high-reverse-bias region, whereas the magnitude of the peak is obtained at the lowest frequency. This behavior can be explained by the effect of R_s and also the indication of the existence and response of interface charges to the change in alternating current (AC) [16, 29]. A decrease in the values at each frequency plots at the high-forward- and high-reverse-bias regions is related to the effect of R_s [66]. On the other hand, frequency effects on these measured values are observed strongly at low frequencies. Together with the effects of R_s, the observed variations mostly in depletion and accumulation zones can be related to the presence of the interface states. At this point, resistance can be related to the bending behavior of these curves in the accumulation region with the contribution of interface traps in the depletion region [16]. The higher capacitance values are obtained at low frequencies where the density of interface states (D_{it}) is in equilibrium with the semiconductor [16, 67]. At these frequencies, under the effect of interfacial space-charge formation, interface state capacitance contributes to the total diode capacitance causing observed excess capacitive behavior. In addition, the particularly distributed interface states can follow the applied AC signal and the response to the change in frequency is the case depending on the intrinsic characteristics of the interface states as relaxation time of charges [68]. This behavior can also be attributed to the time-depending response of the diode with the dielectric polarization of the interface layer under the effect of applied electric field [67]. The conductance (G) characteristics of the diode are shown in Fig. 8b in the form of $G/\omega - V$ plots at different frequencies. G/ω values are sensitive in the forward-bias region at low frequencies related to the ability of the interface states to follow the applied AC signal and the contribution of charges to the conductive behavior. Similar to the capacitive behavior, the interlayer variations as D_{it} and also the existence and possible effects of R_s depending on the change in frequency limit the conductive behavior. At high frequencies, D_{it} cannot follow the AC signal, and conductance values decrease with the elimination of charges in these states [69, 70]. These observed frequency-dependent

variations in Fig. 8 can also be expected from metal–semiconductor diode with different interface layers and without them at the Au–Si interface [15, 16, 29]. Although the observed decreasing behavior with increasing frequency can be evaluated as a general behavior, the peak formation generally in $C-V$ curve can be attributed to the existence of D_{it} in the depletion region due to the interface state [15, 16]. In addition, the single peak observed in this curve can be the indication of localization of these states in one region [16].

Due to the experimental nature, non-ideality behaviors are observed in these $C-V$ and $G/\omega-V$ spectra as in the case of $I-V$ characteristics. Therefore, similar to the $I-V$ analysis, inhomogeneities in the interfacial layer and barrier height depending on the presence of an interfacial insulator layer on Si surface, interface states between Si and metal Au as D_{it}, and R_s can be evaluated based on these data to discuss these deviations [71–73]. At this point of view, the semiconductor/insulator interface and also the effects of R_s and D_{it} have become indicative characteristic parameters in the analysis of the origin of these frequency-dependent variations [73]. Although there are several techniques to extract R_s, the method developed by Nicolian presents a theoretical expression generally acclaimed in the literature [71]. At sufficiently high frequencies and in the strong accumulation region, R_s is expected to be dominant in the current flow. Therefore, these voltage- and frequency-dependent values can be extracted as:

$$R_s = \frac{(G/\omega C)^2}{\left[1+(G/\omega C)^2\right]G} \tag{9}$$

where ω is the angular frequency of the AC signal ($\omega = 2\pi f$) [7]. According to Eq. (9), the R_s values are calculated with bias voltage dependence at each frequency, and the results are given in Fig. 9a. As seen in this figure, the values are in the same order in magnitude with the obtained values from I–V analysis. The calculated values strongly depend on frequency and decrease with an increase in bias voltage at constant frequency [16, 29]. There are peak points dominant at lower frequencies and the intensity of these peaks decrease together with positional shift toward lower voltages with an increase in the applied frequency. This behavior is observed in all frequency-dependent R_s profiles, and it can be attributed to the localized interlayer states and possible interface layer formation on Si surface [8, 70]. It is also the fact correlating with the frequency-dependent characteristics of the measured C–V and $G/\omega-V$ plots [16]. On the other hand, there is a weak response of the R_s values to the variation in high-frequency region. In addition, these values are presented as a function of frequency under constant bias voltage in Fig. 9b. As shown in Fig. 9, these values change under the dependence of both frequency and voltage. Furthermore, there is a strong response at low bias voltage and

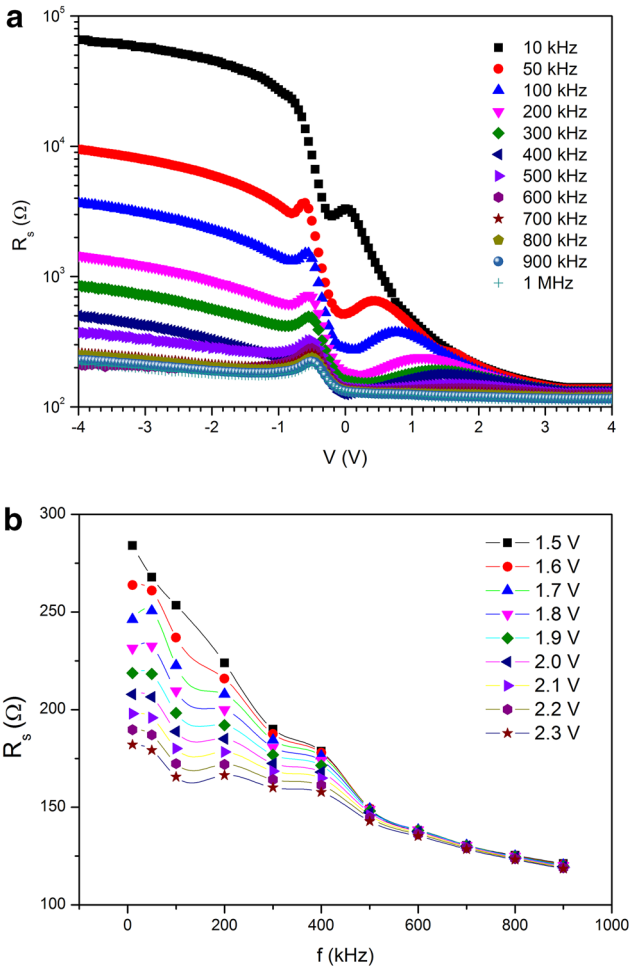

Fig. 9 Variations of **a** frequency- and **b** voltage-dependent R_s values of the Au/$CuCo_5S_8$/Si diode

low-frequency region in these plots. In a similar behavior observed in R_s–V plot, R_s values decrease with increase in frequency in addition to the decrease with increasing bias voltage. It is the trapped charge effect on R_s values, and these variations depending on both voltage and frequency changes can be related to the inhomogeneity in the diode interface and the distribution of D_{it} [70]. In accordance with the interface layer nature, the saturation behavior at the high-forward-bias region can be observed due to the its passivation effect [16]; however, the obtained resistance values are expected to be greater than the values in the diode without interface layer depending on the physical barrier of this layer to the current flow. Together with R_s analysis, the frequency and voltage-dependent D_{it} characteristics of the diode can be investigated in order to detail the electrical quality of the interface layer. Therefore, the change in D_{it} under frequency is investigated using Hill–Coleman conductance method as:

$$D_{it} = \frac{2}{qA}\left(\frac{(G/\omega)_{max}}{\left((G/\omega)_{max}C_i\right)^2 + \left(1 - C_{max}/C_i\right)^2}\right) \quad (10)$$

In this expression, C and G are the measured capacitance and conductance values at each frequency where $(G/\omega)_{max}$ denotes the peak value in the conductance profile (at 1 MHz) and C_{max} is the value corresponding to this peak point [74]. According to Eq. (10), the possible effects of the interfacial layer can be examined using $D_{it} - f$ graph where the profile strongly depends on the C_i values in the strong accumulation region. C_i values can be expressed as [75]:

$$C_i = C_{max}\left(1 + \left(\frac{G_{max}}{\omega C_{max}}\right)^2\right). \quad (11)$$

The obtained frequency-dependent distribution profile of D_{it} is shown in Fig. 10a. As shown in this figure, D_{it} values decrease with the increment in frequency where the parabolic decrease is in a good accordance with the literature and also these values close to a constant value at the higher frequency region [15, 16]. Based on the non-ideal diode characteristics, this fact can be related to the high-frequency response of D_{it} to the change in the external AC signal [67, 76]. Another way to determine the D_{it} profile is the high–low-frequency capacitance (C_{HF}–C_{LF}) method in the form as:

$$D_{it} = \frac{C_{it}}{qA} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_i}\right)^{-1}\right]. \quad (12)$$

This expression gives the bias voltage-dependent distribution of D_{it} values where C_{HF} and C_{LF} are the values observed at the highest-frequency capacitance (1 MHz) and lowest-frequency capacitance steps (at 50 kHz), respectively [77]. The voltage-dependent profile with a peak around 0.1 V is shown in Fig. 10b, and the obtained values using both Hill–Coleman and C_{HF}–C_{LF} methods are in the same order in magnitude. In comparison with the literature, these values are in the same range with the values reported as a result of both I–V and C–V analyses [13, 16, 29, 46]. However, the effect of the interface layer can be observed in the decrease in these values with respect to the diode without this layer formation at the interface [13, 16]. It is due to the interface states originating from this layer and also the remedial effect on the interfacial trapped charges can be occurred at the interface [16]. The peak profile in the D_{it}–V plot indicates a certain D_{it} between the metal (Au) and the semiconductor (Si) due to the interruption of the structural periodicity, and therefore, it can be concluded that these traps are uniformly distributed inside the band gap of the semiconductor layer [68, 78]. In order to evaluate the effects of D_{it}, the conductance of interface states (G_{it}) can be formulated according to the Nicollian and Goetzberg model as:

$$G_{it} = \frac{qI_{dc}}{kTA}\frac{C_i\left(C - C_{HF}\right)}{(G/\omega)^2 + \left(C - C_{LF}\right)^2}, \quad (13)$$

where I_{dc} is used to donate the forward-bias current flow in the diode [71]. The obtained $G_{it}/\omega - f$ plots are presented in Fig. 11a with a peak profile at the low-frequency region. This peak behavior can be ascribed with the existence of interface traps and the profile is strongly dependent on the occupancy of the interface trap levels [78]. In fact, the existence of these maximum G_{it}/ω values indicates the uniform distribution of D_{it} which affects the value of capture cross sections of traps [78, 79]. As seen in Fig. 11a, the peak intensity decreases and the peak position shifts toward higher frequencies with increasing bias voltage. The observed shift can be related to the characteristic time of the interface states to fill and

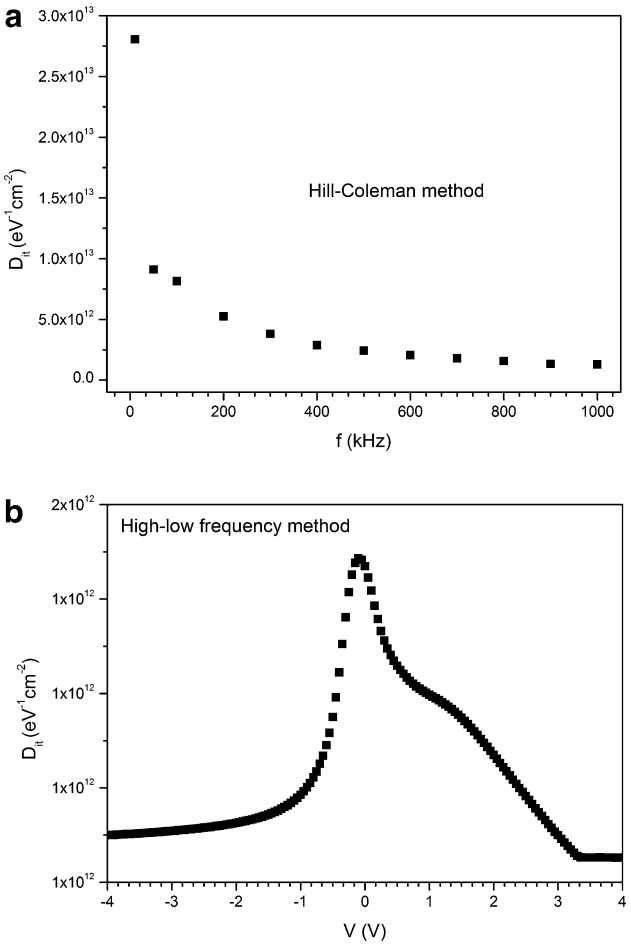

Fig. 10 D_{it} profiles of the Au/$CuCo_5S_8$/Si diode according to **a** Hill–Coleman and **b** high–low-frequency methods

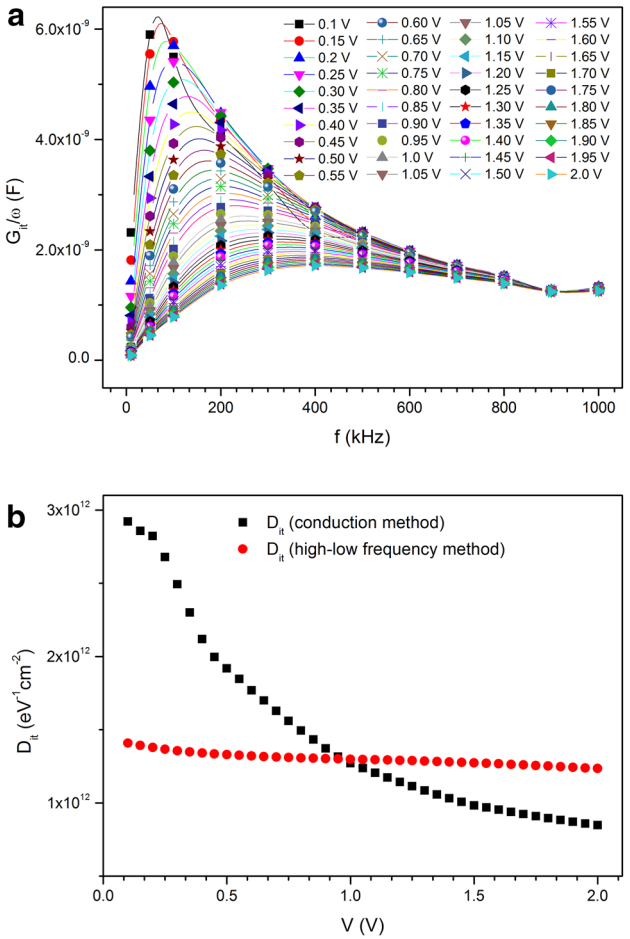

Fig. 11 **a** $G_{it}/\omega - V$ plot of the Au/$CuCo_5S_8$/Si diode and **b** comparison of the D_{it} profiles obtained from conductance and high–low-frequency methods

empty with the electrons exchanging by the valence band of the semiconductor [78]. From the peak points observed in Fig. 11a, D_{it} values can be found as a function of voltage as,

$$D_{it} = \left(G_{it}/\omega\right)_{max}/0.402qA \tag{14}$$

where G_{it} values can be related to the time constant of interface states (τ) as:

$$G_{it} = \frac{AqD_{it}}{2\tau} ln\left(1+\omega^2\tau^2\right), \tag{15}$$

and the maximum condition $\omega\tau = 1.98$ $\left[\partial G_{it}/\partial(\omega\tau) = 0\right]$ is applied to determine D_{it}–V profile shown in Fig. 11b. Comparing with the experimental results found in Fig. 10a, although there exists an almost continuous distribution of D_{it} values based on the high–low-frequency method, the values obtained from the conduction method given in Eq. (15) decrease with increasing bias voltage. This result indicates that the primary capture and emission processes occurred at traps, and the response of these traps at a different frequency dominates the behavior of these values [80, 81].

4 Conclusion

In this work, together with the detailed structural and morphological analysis of $CuCo_5S_8$ thin-film layer, the electrical characteristics of spin-coated $CuCo_5S_8$ film interlayered Al/$CuCo_5S_8$/Si diode are discussed in terms of current and capacitance measurements under dark and solar-illuminated conditions. Dark *I–V* characteristics show a good rectifying behavior with about Φ_b and n of 0.69 eV and 6.72, respectively. Under illumination, the reverse current values increase with the contribution of photogenerated carriers to the current flow, and it results in an increase in Φ_b but in a decrease in n values. The saturated regions in the forward-bias region are evaluated with the possible effects of R_s, and the values are obtained based on Cheung functions. Photoconducting and photocapacitive behaviors of the diode are discussed by transient measurements and the potentials of this diode in several optoelectronic applications are verified. Depending on the applied bias voltage and frequency, capacitance and conductance profiles are evaluated considering the possible effects of R_s and D_{it}. The calculated R_s values show a strong dependency to the change in frequency and voltage. The R_s profiles exhibit peaks as a response to the frequency change due to the localized states and possible native interface layer formation on Si surface. Because the photoresponse behavior of the diode indicates the existence of these states, the D_{it} profiles are discussed according to the high–low-frequency, Hill–Coleman, and conductance methods.

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