Experimental investigations in the intermetallic and microvoid formation in sub-200 °C Cu–Sn bonding

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Abstract

This paper reports the intermetallic growth and microvoid formation in the Cu–Sn layers, which were annealed at low temperatures (sub-200°C) for durations varying from 120 to 1440 min. A 10 μm thick tin was electrodeposited on copper samples. Both Cu_6Sn_5 and Cu_3Sn IMCs were formed and had a non-uniform scalloped shaped profile but with different scallops sizes. Void growth was studied at three different locations, i.e., the $Cu–Cu_3Sn$ interface, within the Cu_3Sn, and at the $Cu_3Sn–Cu_6Sn_5$ interface. The void size in these locations increased with increasing annealing durations and temperatures due to the coalescence of nearby voids. The void fraction at the $Cu–Cu_3Sn$ and $Cu_3Sn–Cu_6Sn_5$ interfaces was observed to decrease, whereas the void fraction within the Cu_3Sn IMC increased with increasing annealing durations. The largest voids were seen at the $Cu–Cu_3Sn$ interface, while the highest void fraction was found within the Cu_3Sn IMC. The overall void size and void fractions for all experimental conditions were always smaller than 3 $μm^2$ and 1.44 $μm^{-1}$, respectively. The obtained results can be used in the hermetic packaging of MEMS devices performed at sub-200 °C. Processing at these low temperatures result in reduced thermo-mechanical stress and also eliminate the molten tin squeezing-out from the bonding zone, which is a known issue in Cu–Sn solid–liquid inter-diffusion bonding performed at temperature > 232 °C.

1 Introduction

Achieving hermetic packaging is an absolute necessity to maintain long term reliability in Micro-electro-mechanical-systems (MEMS) inertial sensors such as accelerometer, gyroscopes, and digital micromirror, etc. Hermetic packaging not only provides a controlled environment but also protects the moving structures from the external contaminants, and moisture, and thus, preventing the devices from the corrosion.

Anodic bonding, glass-frit bonding, eutectic bonding, and thermocompression bonding are some of the popular hermetic packaging techniques used in MEMS applications; however, these techniques have certain limitations. Anodic bonding requires high electrical potential (> 300 V), which may not be suitable for many commercial applications [1]. In the glass-frit bonding, the processing temperature is around ~ 400 °C, which results in higher thermo-mechanical stresses. The re-melt temperature of the glass-frit bond is around the original bonding temperature, which restricts its application to multiple stacking. Fusion bonding is not suitable for MEMS packaging applications due to its extremely high bonding temperature (> 600 °C). Higher bonding temperatures generate higher thermo-mechanical stresses since the materials used in MEMS sensors and packaging has different coefficients of thermal expansion (CTE), which often results in failure and reliability risks. To improve the long-term reliability, there are continuous demands to develop cost-effective packaging methods having lower processing temperatures, leading to reduced thermo-mechanical stresses [2].

Metal-based hermetic bonding techniques are being explored for the MEMS packaging applications. The metals have extremely low helium leakage rate compared to silicon and glass-based materials, thus implying a very high degree of hermeticity [3, 4]. The metallic bond pads/rings also provide efficient heat dissipation along with rigid mechanical support to the packaged structure. Direct metal-to-metal thermocompression bonding (i.e., Cu–Cu, Au–Au) is used in the packaging of MEMS accelerometers for mobile phone applications. However, in the thermocompression bonding, the pressure is beyond the yield strength of the metals. In some extreme cases where the die thickness is less than

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50 μm, the bonding pressure resulted in the die cracking [3]. It also has a high bonding temperature (~ 350–400 °C), which led to the generation of high thermo-mechanical stresses. Native oxide formation in Cu and the higher cost of Au are other challenges in achieving process-compatible, reliable, and low-cost hermetic packaging by direct metal-to-metal thermocompression bonding [5].

To overcome the limitations of thermocompression bonding while retaining its advantages, soft metal-based Solid–liquid-inter-diffusion (SLID) bonding was explored. In SLID bonding, an intermediate metal (e.g., Sn and In) having low melting temperatures (< 232 °C) is used for bonding purposes. Compared to thermocompression bonding, SLID has lower bonding temperatures and bonding pressures. Cu–Sn based SLID bonding has been used because of their low-cost, readily available, and the lower melting point of tin [6–10]. At bonding temperatures above the melting point of Sn, Cu initially dissolves into the molten Sn till liquid Sn gets saturated with Cu. It results in the formation of solid intermetallic compounds (IMCs), namely Cu_6Sn_5 and Cu_3Sn having higher melting points, i.e., 415 °C and 676 °C, respectively [11, 12]. Since the IMC thicknesses are quite low and are electrically conductive [13], the SLID bonding can also be used to form interconnects simultaneously.

SLID bonding eliminates the requirement of a very smooth and uniform surface since the intermediate soft metal is easily deformed upon low bonding pressures. The mechanical strength of the SLID bonded structures has shown wide variations in the range of 2 to 60 MPa [11, 14–16] which implies that a better understanding of the Cu–Sn SLID bonding process including the IMC growth and void formation and the effect of voids over the IMC growth is required.

Most of the literature related to Cu–Sn diffusion bonding has higher processing temperatures (> 232 °C) [9–11, 17–22], while the studies involving Cu–Sn diffusion study at low temperatures (< 232 °C) are either performed with solders or are very limited [7, 8, 10, 23]. At higher processing temperatures (> 232 °C), the molten tin squeezing out between the die and the substrate are observed when the pressure is applied. This squeezed tin may causes short-circuit and result in reduced reliability [9, 14]. Figure 1 shows the problem of tin squeezing/flowing out when the Cu–Sn samples were heated at 300 °C for 10 min. The molten tin gets in contact with the neighboring copper pad and may cause the short-circuiting of the devices. The squeezing out of Sn also reduces the available amount of Sn, which results in reduced IMC growth. This problem can be eliminated by performing the bonding at sub-200 °C temperature. As

Fig. 1 SEM images showing the electrodeposited copper pads covered with 3 μm tin, **a** molten tin was squeezed out at 300 °C, **b** tin was intact at 200 °C
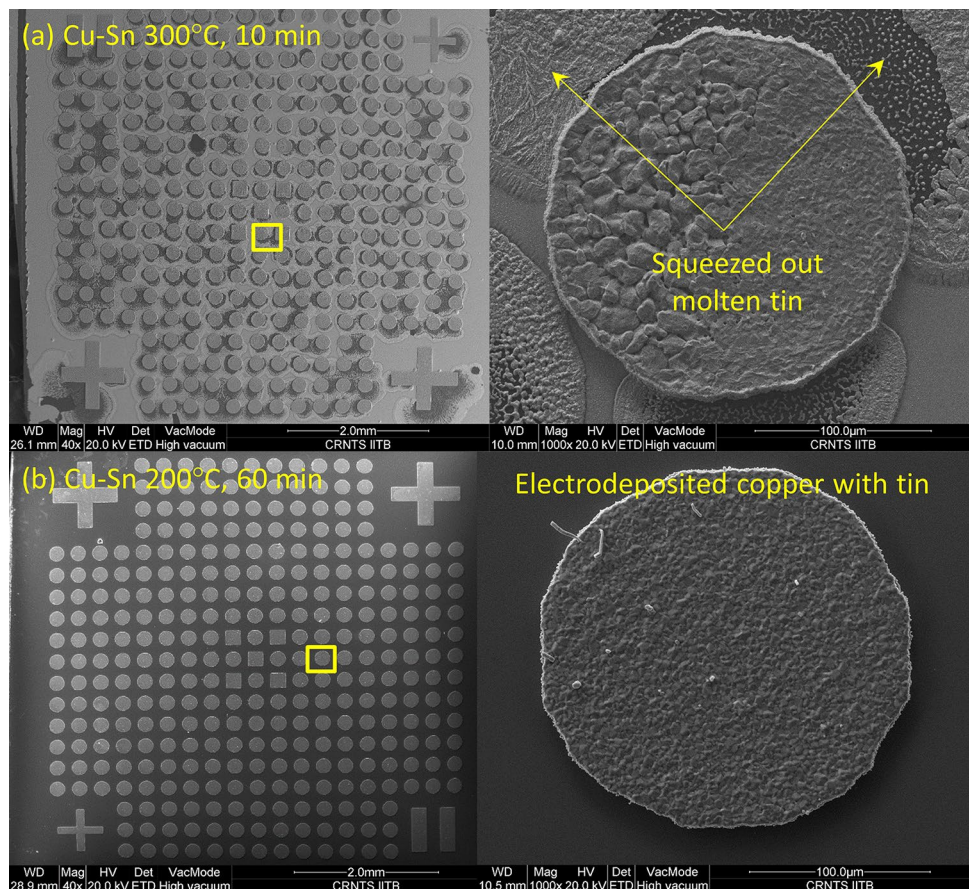
shown in Fig. 1b the electrodeposited tin was still intact when the samples were heated to 200°C for 60 min.

A combined study of IMC growth and void formation for the Cu–Sn bonding at sub-200 °C is essential to address the existing issues of SLID bonding and to achieve a cost-effective, reliable hermetic packaging of MEMS devices. Therefore, IMC growth and void formation in the Cu–Sn solid-state diffusion stacks are investigated at sub-200 °C. In this study, void formation and IMC growth at different annealing temperatures for varying durations are presented in terms of the average void sizes, the void fractions, and the IMC thicknesses. The experimentally measured IMC thicknesses were later compared with the thickness predicted by a MATLAB numerical simulation model using the diffusion parameters from the literature [10]. Variation in the void size and void fraction with their effects on the IMC growth are also reported.

2 Experimental details

2.1 Sample preparation

Copper samples (purity 99.9%) having a diameter of 16 mm and 10 mm length were used as the substrates, which were polished and cleaned with acetone, isopropyl alcohol (IPA) and deionized (DI) water in the ultrasonic bath to remove any organic impurities and airborne particles. A 10 μm thick Sn layer was electrodeposited by using a pulse electrodeposition technique. Both pulse-on and pulse-off periods were kept as 1 ms. Electrodeposition was performed at a current density of 30 mA/cm^2 in a commercial electrolyte (Atotech, Germany), having continuous filtration and agitation to achieve uniform electrodeposition. The Cu substrates before and after the electrodeposition of Sn are shown in Fig. 2.

The samples were annealed at different temperatures (i.e., 150 °C, 175 °C and 200 °C) for varying durations (i.e., 120 min, 420 min, and 1440 min) in a vacuum furnace to
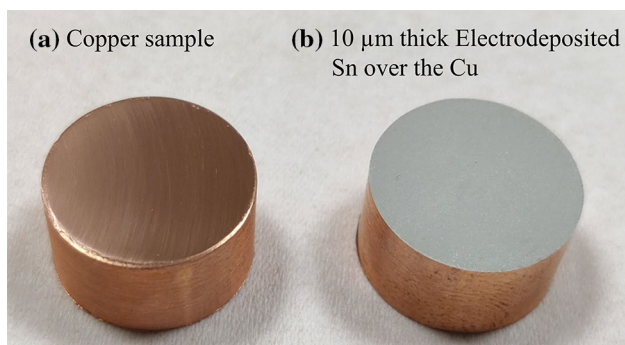

Fig. 2 Fabricated samples for the void and IMC growth in this study, **a** Pure Cu sample, and **b** Electroplated Sn over Cu sample

inhibit the oxidation of copper and tin. The annealed samples were then molded in an epoxy mold and sequentially polished using silicon carbide (SiC) papers and diamond suspensions having 6 μm, 1 μm, and 0.25 μm particle sizes.

2.2 Microstructural characterization

The cross-sectional micrographs of the samples were observed under the field emission gun scanning electron microscope (FEG-SEM) (JEOL JSM-7600F). All FEG-SEM micrographs were analyzed at a ×4000 magnification having a resolution of 0.023 μm pixel^{-1}. Energy dispersive spectroscopy (EDS) was performed to identify the composition of the observed IMCs. The SEM micrographs were analyzed to measure the average thicknesses of Cu_6Sn_5 and Cu_3Sn, void sizes in terms of void areas and void fractions, i.e., the number of voids per unit length. The voiding data was observed at three locations, i.e., at the Cu–Cu_3Sn interface, within the Cu_3Sn, and the Cu_3Sn–Cu_6Sn_5 interface. For each experimental condition, the IMC thicknesses, the void areas, and the void fractions were measured at four different regions in three different samples to get the averaged data. As the void growth is arbitrary, the average data of IMC thickness and void areas will be a fair approximation of the behavior of entire Cu–Sn stack.

3 Experimental results and discussion

3.1 Intermetallic growth in the Cu–Sn stack

Initially, the IMC thicknesses were calculated by a MATLAB-based numerical simulation using the reaction kinetics model for one-dimension diffusion. The diffusion parameters needed in this model were taken from the literature [10]. The thicknesses of IMCs and consumed Sn for any temperature and duration were given by [10]:

$$y_t^2 - y_o^2 = kt^{2n} \tag{1}$$

where

$$k = k_o \exp\left(-\frac{E_a}{RT}\right) \tag{2}$$

where y_t represents the thickness (μm) at time t (min), y_o is the initial thickness at $t = 0$ min, i.e., $y_o = 0$, k is the diffusion rate constant (μm^2 min^{-1}), k_o is the diffusion coefficient (μm^2 min^{-1}), E_a is the activation energy (kJ mol^{-1} K^{-1}), R is the gas constant (kJ mol^{-1}), T is the absolute temperature (K), t is the annealing time (min), and n is the dimensionless empirical time constant. The Cu_6Sn_5 thickness was calculated by using the mass conservation of Sn as the amount of consumed Sn will be equal to the total amount of Sn present in the Cu_3Sn and the Cu_6Sn_5 [21]. The total IMC

thickness was calculated as the summation of the Cu_3Sn and the Cu_6Sn_5 thicknesses.

Figure 3 shows the composition of the top surface of an electrodeposited sample annealed at 200 °C for 1440 min as obtained by the EDS. The results confirmed that the top surface in all the samples still had Sn, which was not entirely converted into the IMCs. The thickness of IMC layers predicted from the simulation model indicates that even at extreme experimental conditions (200 °C and 1440 min) only a 5.98 μm thick Sn would be consumed to form a 6.67 μm thick Cu_6Sn_5 and a 2.56 μm thick Cu_3Sn. The simulation model predicted that the complete conversion of a 10 μm thick Sn into Cu_6Sn_5 and Cu_3Sn IMCs would require more than 4600 min at an annealing temperature of 200 °C. Performing experiments for such a prolonged duration is not practically possible, and therefore, the lower thickness of electrodeposited tin should be used for sub-200 °C bonding applications.

Figure 4 shows the formation of IMCs in the samples annealed at different experimental conditions. The cross-sectional SEM micrographs also confirmed that the Sn was not completely consumed to form the IMCs. Both Cu_6Sn_5 and Cu_3Sn IMCs have non-uniform scallops, but the variation of scallop size in the case of Cu_6Sn_5 was higher than that in the Cu_3Sn. Since, it has been reported that Cu_6Sn_5 has

monoclinic lattice structure at temperatures below 186 °C and hexagonal lattice structure above 186 °C [24, 25], the diffusion rates would be different in the different crystallographic directions. Therefore, a scallop shape growth was noticed in the Cu_6Sn_5 IMC. The small scallops of Cu_3Sn could be due to the selective and rapid dissociation of Cu_6Sn_5 into Cu_3Sn at specific locations. The IMC thicknesses were observed to increase with increasing durations for all annealing temperatures (Fig. 4a–i).

Since the IMC growth is parabolic [26], the square of IMC thickness was plotted against the annealing duration (Fig. 5). A linearly increasing trend was noticed for the Cu_6Sn_5 and Cu_3Sn growth with the increasing durations at the given annealing temperature. These results have verified the parabolic growth behavior of both IMCs. The slope of Cu_6Sn_5 growth was lower than that of the Cu_3Sn. It implies that the Cu_3Sn growth occurs at a slower rate than the Cu_6Sn_5 growth at the initial stages of annealing. However, as the annealing duration increases, the growth rate of Cu_3Sn is higher than Cu_6Sn_5 IMC. It was clearly observed for the samples annealed at 150 °C, i.e., for 120 min, the average Cu_3Sn thickness was lower (0.63 μm) than average Cu_6Sn_5 thickness (1.02 μm) and for 1440 min, the average Cu_3Sn thickness was higher (1.86 μm) than that of the Cu_6Sn_5 (1.63 μm) (Fig. 5a). A similar trend was also observed for
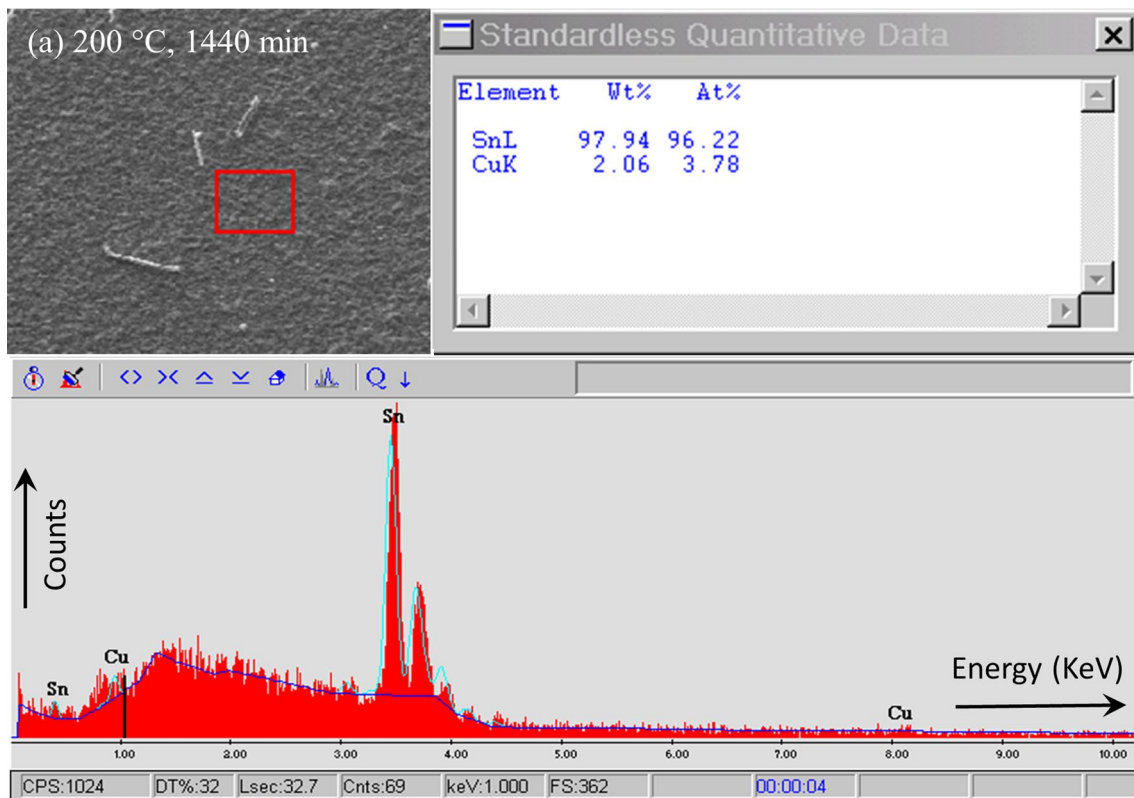

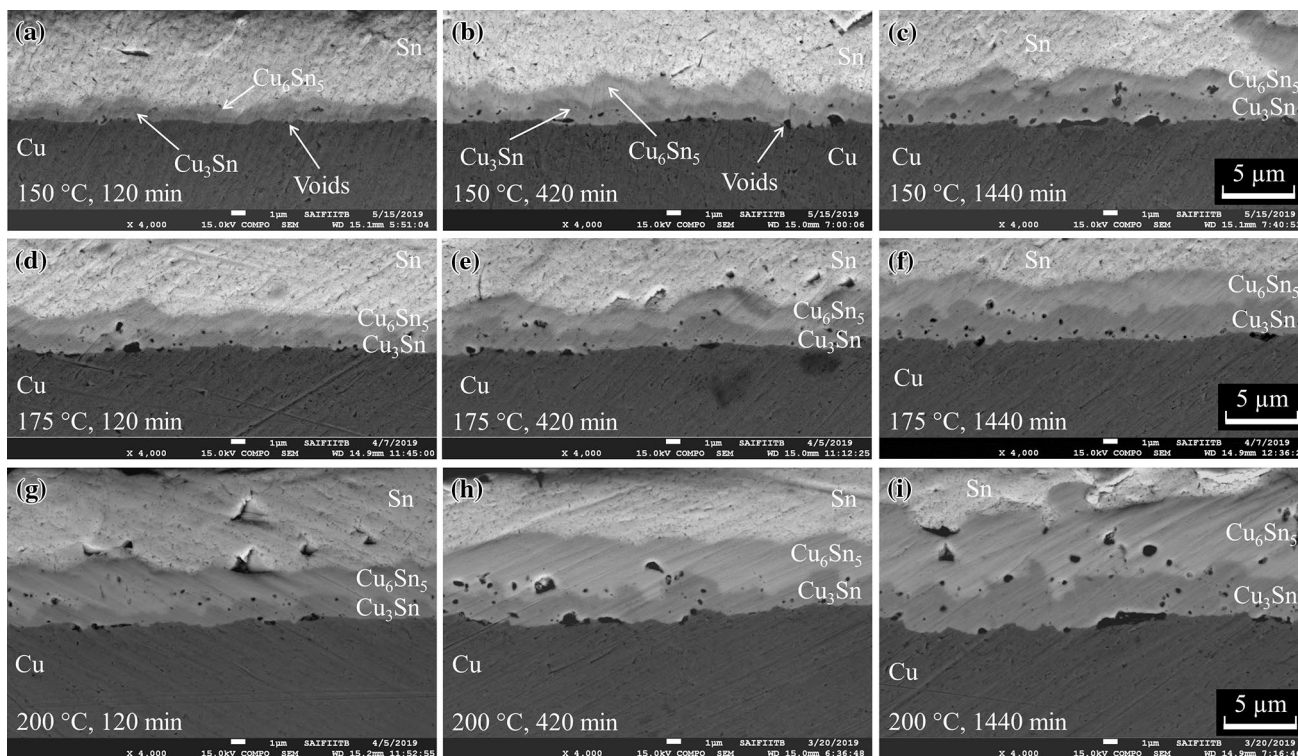**Fig. 3** EDS of Cu–Sn samples annealed at 200° for 1440 min

Fig. 4 SEM micrographs showing cross-sections of the samples annealed at different temperatures and time durations. **a–c** 150 °C, for 120 min, 420 min and 1440 min; **d–f** 175 °C, for 120 min, 420 min and 1440 min; **g–i** 200 °C, for 120 min, 420 min and 1440 min, respectively. (Same scale for all the SEM micrographs)

Fig. 5 Variation of the square of the IMC thickness with time to show parabolic growth of Cu–Sn IMC for different temperatures, i.e. **a** 150 °C, **b** 175 °C, and **c** 200 °C
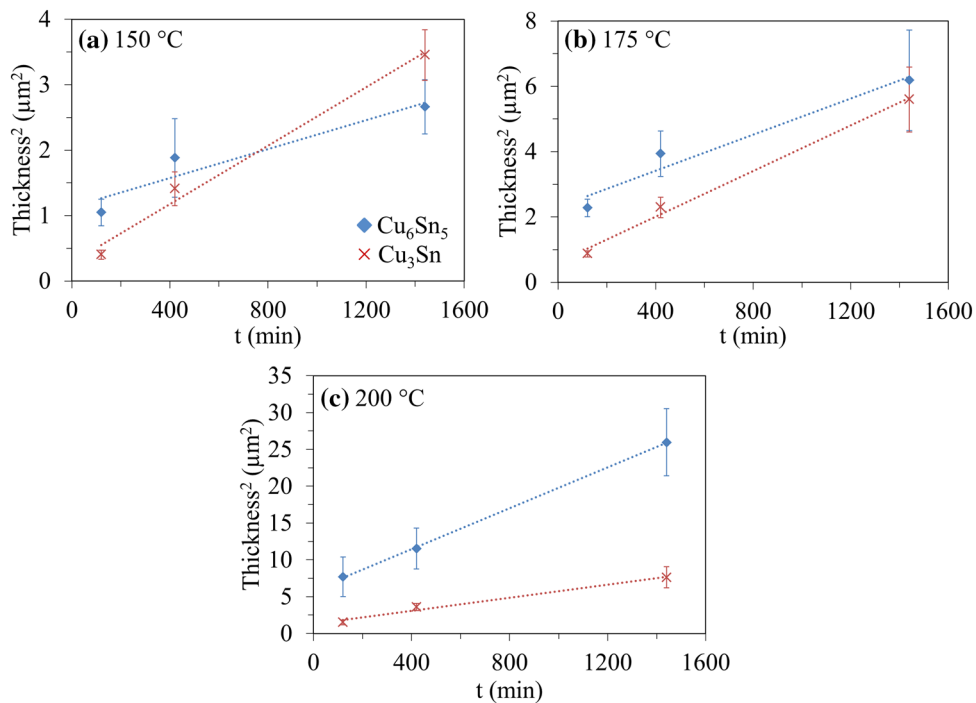
samples annealed at 175 °C (Fig. 5b). However, the samples annealed at 200 °C showed deviation from the above trend in which the growth rate of Cu_3Sn IMC was measured to be lower than the growth rate of Cu_6Sn_5 (Fig. 5c). The reduced growth rate of Cu_3Sn was due to the larger voids formed in the samples annealed at 200 °C compared to the other experimental conditions. These voids acted as a barrier layer for diffusing Cu atoms resulting in reduced Cu_3Sn IMC growth at 200 °C. However, the fraction of the interface that voids cover is relatively smaller, so another reason for lower Cu_3Sn thickness than Cu_6Sn_5 at 200 °C could be the higher stability of Cu_6Sn_5 at higher temperatures [27].

The IMC thicknesses were also observed to increase with increasing annealing temperatures for a given duration, as shown in Fig. 4a, d, g for 120 min of annealing. The variation of IMC thicknesses as a function of annealing temperature for a given duration is presented in Fig. 6. The slope of Cu_6Sn_5 was higher than that of the Cu_3Sn for a given duration. The difference in the Cu_3Sn and Cu_6Sn_5 thicknesses increased with the increasing annealing temperatures. It indicates that the growth of Cu_6Sn_5 was faster at higher temperatures than that of Cu_3Sn for a given annealing duration. Figure 6a illustrates that for a 120 min annealing duration, the difference between the Cu_6Sn_5 and Cu_3Sn IMC thickness was less at 150 °C, but was comparatively higher at 200 °C. This implies that the growth of Cu_6Sn_5 occurs more rapidly at higher annealing temperature than that of the Cu_3Sn IMC for the given annealing duration. The slope of the Cu_6Sn_5 IMC growth was nearly three times higher than that of the Cu_3Sn IMC growth. Another reason for the dominant growth of Cu_6Sn_5 IMC was the significant

void growth at the Cu–Cu_3Sn interface at higher temperatures, which retarded the Cu diffusion and eventually reduced the Cu_3Sn growth. Therefore, at higher temperatures, the Cu_6Sn_5 growth dominated over the Cu_3Sn growth for the given annealing duration.

For a constant annealing temperature, the IMC growth results imply that the formation of Cu_6Sn_5 occurs at a faster rate, but as the annealing process continues the Cu_3Sn growth takes over. For longer annealing durations at a given temperature, the thickness of Cu_3Sn IMC increases at a rapid rate at the Cu_3Sn–Cu_6Sn_5 interface by consuming the already formed Cu_6Sn_5 and at Cu–Cu_3Sn interface by the reaction of diffused Sn with the available Cu. For a constant annealing duration, the Cu_6Sn_5 showed a higher growth rate for higher annealing temperatures. It shows that the annealing performed at a higher temperature favors the growth of Cu_6Sn_5 subjecting to the availability of pure Sn. The annealing for longer duration favors the growth of Cu_3Sn since the Cu_6Sn_5 reacts with the diffusing Cu atoms and decomposes to form Cu_3Sn.

The diffusion rate constants and the activation energy for the IMCs growth were calculated from the measured IMC thicknesses obtained at different annealing temperatures and durations using the simplified version of Eq. (1) and Eq. (2) as:

$$\ln\left(y_t^2 - y_o^2\right) = \ln(k) + 2n\ln(t) \tag{3}$$

$$\ln(k) = \ln(k_o) - \frac{E_a}{R}\left(\frac{1}{T}\right) \tag{4}$$

The diffusion rate constant and the empirical time constant were measured as the intercept, and the slope of the

Fig. 6 Variation of IMC thickness as a function of annealing temperatures for a given annealing time duration, i.e. **a** 120 min, **b** 420 min, and **c** 1440 min
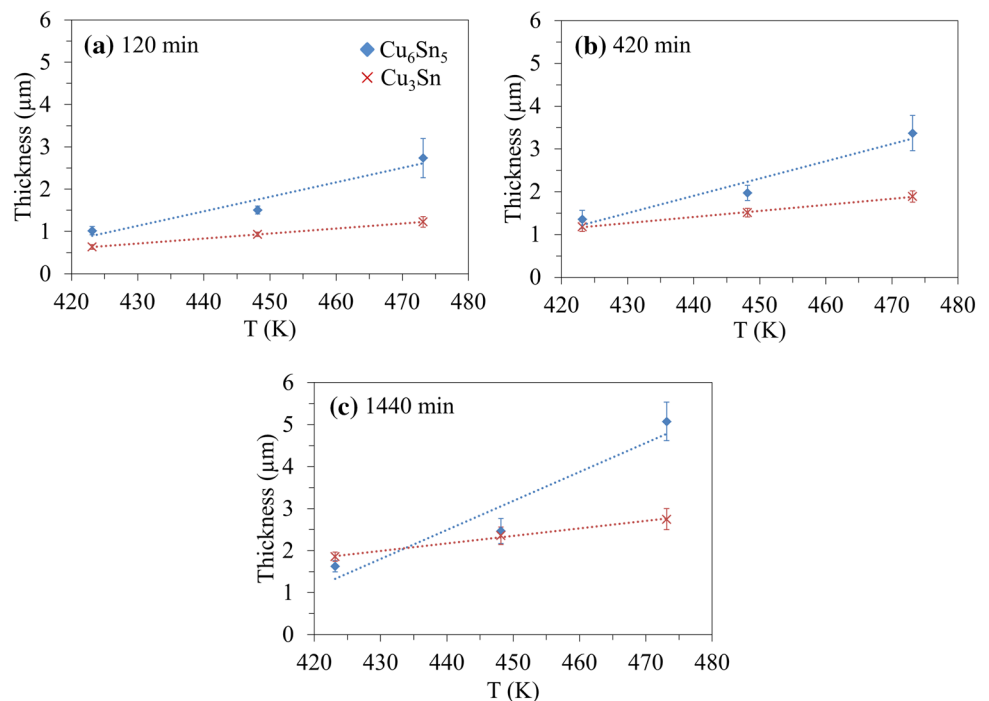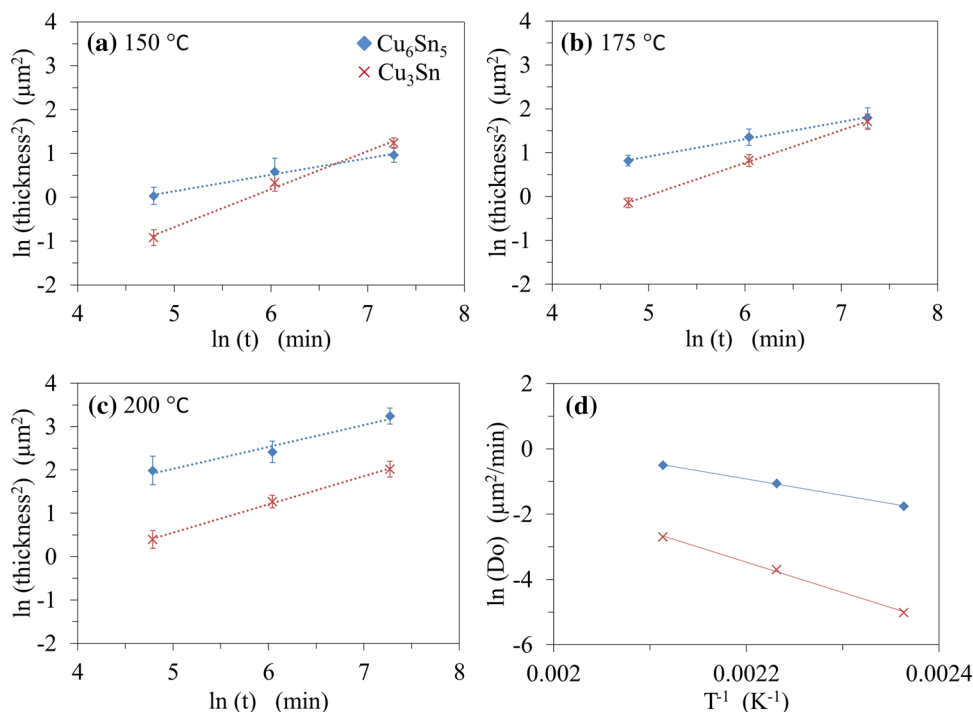
Fig. 7 Variation of the IMC thickness with the annealing time durations in the logarithmic scales to evaluate the diffusion coefficient (k_o), activation energy (E_a) and empirical time constant (n) for different temperatures, i.e. **a** 150 °C, **b** 175 °C, and **c** 200 °C

graphs plotted in Fig. 7a–c using Eq. (3), respectively. Similarly, the diffusion coefficient and activation energy were found by Eq. (4) as the intercept and slope of the graphs plotted in Fig. 7d, respectively. The diffusion coefficient and activation energy for Cu_3Sn and Cu_6Sn_5 IMCs were experimentally calculated to be 2.35×10^7 μm^2 min^{-1}, 77.26 kJ mol^{-1} K^{-1}, and 2.479×10^4 μm^2 min^{-1}, 41.72 kJ mol^{-1} K^{-1}, respectively. The diffusion coefficient and activation energy for consumed Sn thickness was measured to be 1.81×10^6 μm^2 min^{-1}, 59.73 kJ mol^{-1} K^{-1}, respectively. The comparison of the diffusion coefficient and activation energy obtained in this study with those available in the literature is presented in Table 1. Since different units were used in the literature, all values were converted to SI units for the sake of comparison. The diffusion coefficient obtained in this study was comparatively higher than the other studies, which can be attributed to the quality of the used Cu substrates. In this study, 99.9% pure Cu was employed rather than the thermal deposited or electroplated Cu samples, which were used in
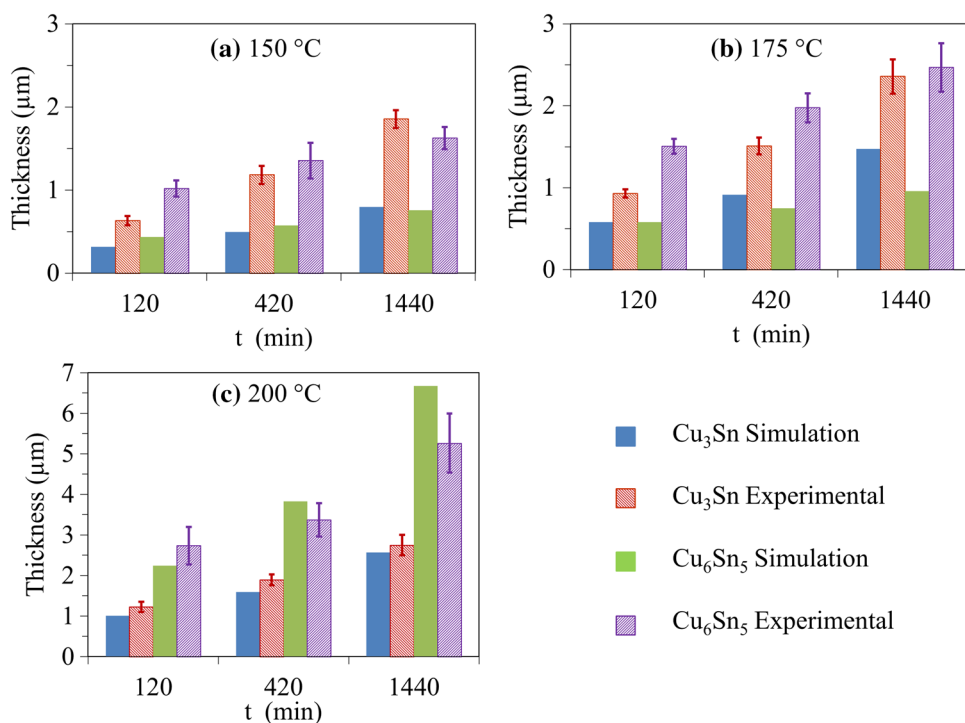
the reported publications. The commercial electrolytes use several additives such as brightener, leveler, suppressor, etc., which introduces certain impurities (carbon, sulfur, chlorine, phosphorus, etc.) into the electrolyte. These impurities from the electrolytes get transferred to the electrodeposits [28], which results in excess void formation. The diffusion process is thus degraded since void formation reduces the actual diffusion area. The activation energy was observed to be in close agreement with the literature having electroplated Cu as the base material.

The experimentally obtained IMC thicknesses were compared with the IMC thicknesses calculated by the simulation model using diffusion parameters from the literature [10] (Fig. 8). It was noticed that the experimentally obtained IMC thicknesses were more than the ones predicted by numerical simulation. It was due to the higher diffusion coefficient for the IMCs growth in this study, which itself was due to the high purity Cu base material. For samples annealed at 200 °C, the experimental Cu_6Sn_5 IMC thickness was lower

Table 1 Comparison of the obtained diffusion coefficients and the activation energy with the earlier reported values in the literature

Temp. range (K)	Cu₃Sn		Cu₆Sn₅		Reference
	Diffusion coefficient (m^2 s^{-1})	Activation energy (kJ mol^{-1} K^{-1})	Diffusion coefficient (m^2 s^{-1})	Activation energy (kJ mol^{-1} K^{-1})	
463–493	1.43×10^{-8}	70.71	1.55×10^{-8}	64.85	[7]
423–498	1.04×10^{-9}	61.98	3.47×10^{-12}	40.29	[8]
423–573	1.32×10^{-7}	78.00	3.24×10^{-11}	39.78	[10]
373–473	3.11×10^{-10}	64.40	1.62×10^{-8}	76.20	[23]
423–473	3.91×10^{-7}	77.26	4.13×10^{-10}	41.72	This study

Fig. 8 Comparison of IMC thickness obtained experimentally in this study and calculated from the numerical simulation using diffusion parameters from literature [10] corresponding to the different annealing temperatures and time durations, i.e. **a** 150 °C, **b** 175 °C, and **c** 200 °C

3.2 Void growth in the Cu–Sn stack

Void growth was investigated in terms of the average void size and the average void fraction at different locations within the Cu–Sn samples, i.e., at the Cu–Cu_3Sn interface, within Cu_3Sn, and at Cu_3Sn–Cu_6Sn_5 interface. Voids within the Cu_6Sn_5 layer were not analyzed in this study since the Cu_6Sn_5 is thermodynamically unstable, and finally gets transformed to the stable Cu_3Sn in the Cu–Sn diffusion bonding.

3.2.1 Void size

Figure 9 presents the variation in the average void size as a function of the annealing time duration at given annealing temperatures. The subset of the individual plot shows the SEM micrographs corresponding to experimental conditions for minimum (i.e., 150 °C, 120 min), in-between (i.e., 175 °C, 420 min) and largest void sizes (i.e., 200 °C, 1440 min). The average void sizes were in the sub-μm range. The average void sizes at different locations were observed to increase with increasing annealing duration (Fig. 9). The voids nucleate at thermodynamically favorable sites like the

vicinity of incorporated impurities or grain boundaries and then increase in size with time due to the merging of the nearby voids [20]. The voids in the Cu–Sn layers are due to the impurities in the base metals and the Kirkendall's effect, i.e., void formation due to the vacancy diffusion because of the differences in the diffusion rate of Cu and Sn into each other as well as their IMCs. The impurities in the base Cu layer result in the void formation at the Cu–Cu_3Sn interface. The impurities, like carbon, chlorine, sulfur, phosphorus, in base Cu diffuses to the Cu grain boundaries and further with diffusion it moves to Cu–Cu_3Sn interface and gets accumulated at the interface aiding void formation at Cu–Cu_3Sn interface [28, 29]. In this study, the base Cu was 99.9% pure, and thus it would not be that much dominant in void formation, but it has still assisted the void formation due to Kirkendall's effect at Cu–Cu_3Sn interface resulting into the high voiding at Cu–Cu_3Sn interface.

The average void size at the Cu–Cu_3Sn interface was significantly larger than the voids within the Cu_3Sn and Cu_3Sn-Cu_6Sn_5 interface (Fig. 9). The void growth rate for voids at Cu-Cu_3Sn interface was also higher than the void growth rate at other locations. The Cu-Cu_3Sn interface acts as the sink for the diffusing vacancies since the vacancies move towards Cu from Sn due to the higher diffusion rate of Cu than Sn into each other and their IMCs [12]. Therefore, the diffusing vacancies move through the Cu_3Sn–Cu_6Sn_5 interface and Cu_3Sn layer to finally get stopped and accumulated at the Cu–Cu_3Sn interface with gradually increasing in size. The Cu–Cu_3Sn interface void sizes for samples
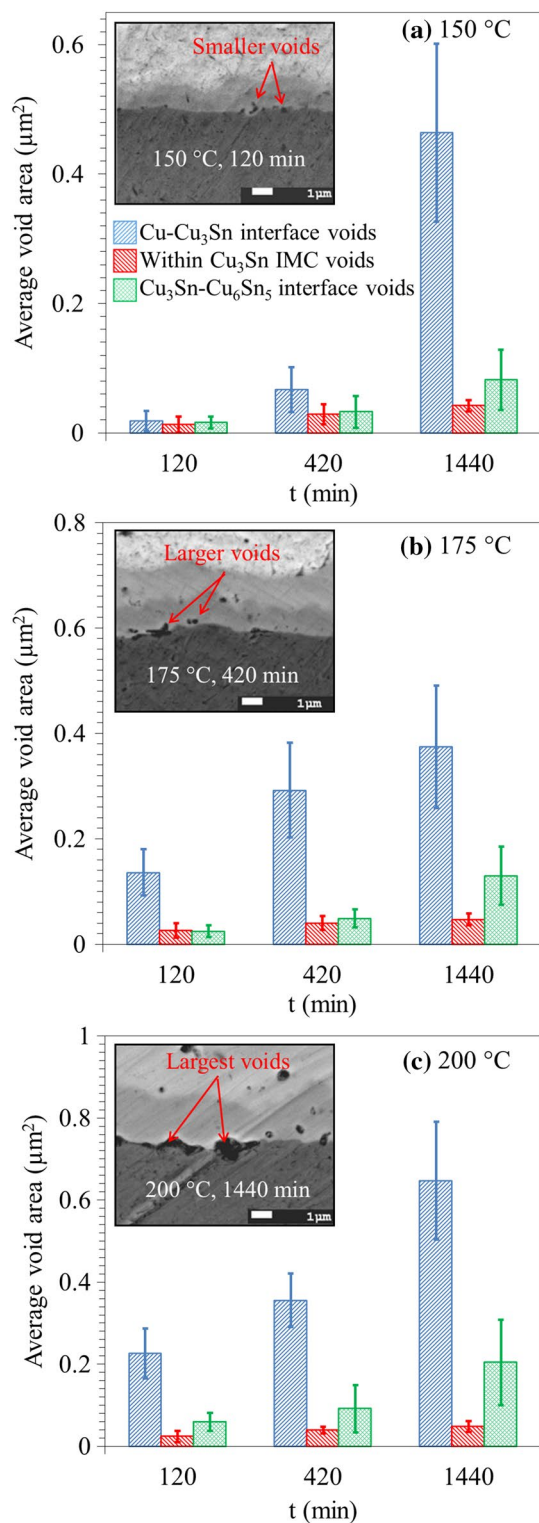
Fig. 9 Variation in the average void size as a function of the annealing durations at the annealing temperatures with SEM micrographs, **a** at 150 °C, **b** 175 °C, and **c** 200 °C. (Same scale for all the SEM micrographs)

annealed at 150 °C for 120 min showed similar void sizes to that at other locations, which can be attributed to the initial stage of void formation at all these locations.

Diffusing vacancies do get accumulated at the Cu_3Sn–Cu_6Sn_5 interface and also within the Cu_3Sn layer, but to a comparatively smaller level than those being diffused through to get accumulated at the Cu–Cu_3Sn interface finally. The average void size and the rate of increase in the void sizes within the Cu_3Sn with the annealing durations were very low. It was due to the higher availability of thermodynamically favorable sites for void nucleation and vacancies getting diffused through the Cu_3Sn layer so that the vacancies did not accumulate significantly within the Cu_3Sn to form larger voids. The void size and the rate of void size increment at Cu_3Sn–Cu_6Sn_5 interface were somehow larger than that of the Cu_3Sn voids but were considerably lower than the voids at Cu–Cu_3Sn interface. Since the vacancies had to diffuse from the Cu_6Sn_5 IMC [monoclinic (> 186 °C) or hexagonal lattice (> 186 °C)] to Cu_3Sn IMC (orthorhombic lattice), the voids would have been stopped at the Cu_3Sn–Cu_6Sn_5 interface due to the mismatch in the crystal lattice structure. This resulted in higher void accumulation at the Cu_3Sn–Cu_6Sn_5 interface and larger void sizes than that within the Cu_3Sn IMC.

The smallest and largest voids were observed to be within the Cu_3Sn IMC and at the Cu–Cu_3Sn interface, in the samples annealed at 150 °C and 200 °C, respectively. The smallest void size was measured to be less than 0.06 μm^2, while the largest void was ~ 3 μm^2 observed at the Cu–Cu_3Sn interface in samples annealed at 200 °C for 1440 min.

3.2.2 Void fraction

Figure 10 shows the variation in the average void fraction obtained for different experimental conditions. For the voids present at the interfaces of Cu–Cu_3Sn and Cu_3Sn–Cu_6Sn_5, the void fraction was observed to decrease with increasing annealing time durations for given annealing temperatures. However, the void fraction for the voids within Cu_3Sn showed an increasing trend with increasing time.

The decreasing trend of the average void fraction at the Cu–Cu_3Sn interface and Cu_3Sn–Cu_6Sn_5 interface was due to the coalescence of smaller voids in the close vicinity to form larger size voids. The increasing trend in the average void fraction for the voids within the Cu_3Sn IMC was different than the voids present at other locations. It was due to the higher number of void nucleation and lower void accumulations near the already formed voids since the newer voids were being formed, resulting in the negligible coalescence of the voids. As the merging of voids did not occur significantly in the Cu_3Sn layer, the number of voids increased with a very slight increment in the void sizes. It resulted in the highest average void fraction in the Cu_3Sn
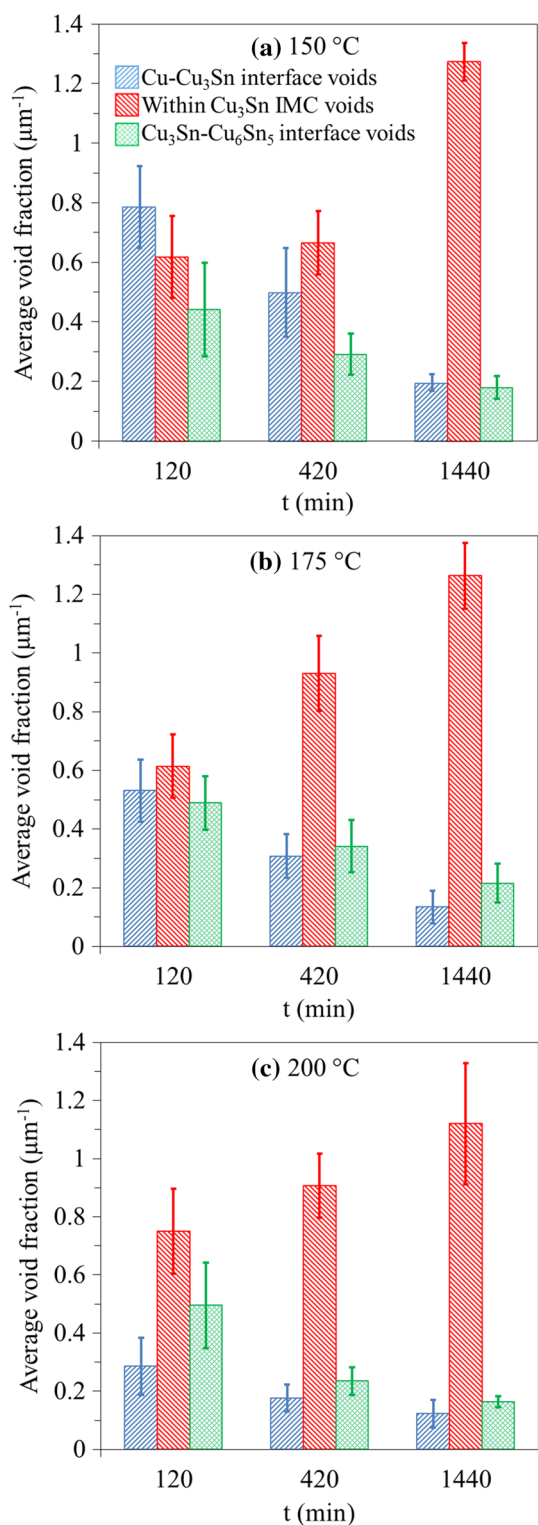
Fig. 10 Variation in the average void fraction with annealing time durations for different annealing temperatures, **a** 150 °C, **b** 175 °C, and **c** 200 °C

layer. For prolonged annealing duration, i.e., > 1440 min, once the prospective thermodynamically favorable sites for void nucleation will be filled with the voids, the void accumulation would occur, which will result in larger void sizes and reduced void fractions.

The average void fraction at $Cu_3Sn–Cu_6Sn_5$ interface was considerably lower than that for voids within the Cu_3Sn and relatively higher than those at the interface of $Cu–Cu_3Sn$ layers. Since the vacancies diffuse from Sn towards the Cu, the diffusing vacancies get partially stuck or stopped at the IMCs interfaces and results in the void formation. The reason for a lower void fraction at the $Cu_3Sn–Cu_6Sn_5$ interface was the coalescence of these partially trapped vacancies while the significant share diffuses into the Cu_3Sn. It resulted in a comparatively larger void size (Fig. 9) and a lower void fraction at $Cu_3Sn–Cu_6Sn_5$ interface than that for the voids within Cu_3Sn (Fig. 10).

The average void fraction was lowest for the voids present at the $Cu–Cu_3Sn$ interface than the voids within the Cu_3Sn layer and at the interface of $Cu_3Sn–Cu_6Sn_5$ layers. The voids at the interface of $Cu–Cu_3Sn$ were accumulated from two sources, i.e., impurities moving from the base Cu resulting in voids and the diffusing vacancies moving from Sn to base Cu due to the higher diffusion rate of Cu than Sn. The different crystal lattice structure of Cu (face-centered cubic) and Cu_3Sn (orthorhombic) having different lattice parameters is believed to be the cause of increased void accumulation at the $Cu–Cu_3Sn$ interface. The rapid coalescence of voids at $Cu–Cu_3Sn$ interface resulted in the large-sized voids and reduced void fraction. The average void fraction of $Cu–Cu_3Sn$ interface voids for samples annealed at 150 °C for 120 min showed a higher void fraction than other locations. At lower annealing temperature and shorter annealing durations, larger numbers of voids have been nucleated at the interface of $Cu–Cu_3Sn$ due to the surface irregularities and impurities present at the Cu surface during electrodeposition of Sn. A similar number of voids would have been formed at different temperatures too but at much lower annealing time durations which would have merged to form larger voids with a smaller void fraction with further annealing.

It was noticed that the average void fraction for the $Cu–Cu_3Sn$ interface voids continuously decreased with the annealing time durations. Initially, the void fraction would be higher at the $Cu–Cu_3Sn$ interface, but as the annealing proceeds, the voids merge and the void fraction decrease to become lowest when compared to the voids formed at the $Cu_3Sn–Cu_6Sn_5$ interface and within the Cu_3Sn. This transition can easily be observed for the samples annealed at 150 °C (Fig. 10a) where the void fraction of the $Cu–Cu_3Sn$ interface is initially the highest and then reduces with the increasing annealing duration. A similar trend was also seen for the samples annealed at 175 °C (Fig. 10b) however, the void fraction at the $Cu–Cu_3Sn$ interface was lesser

than the void fraction obtained at an annealing temperature of 150 °C. It was due to a comparatively higher annealing temperature, which resulted in a relatively faster merging of voids. For samples annealed at 200 °C, the trend was same; however as the annealing temperature was higher than 175 °C, the transition would have occurred at a much earlier stage of the annealing, i.e., < 120 min (Fig. 10c). The highest void fraction was seen in the samples annealed at 150 °C for 1440 min, i.e., 1.44 μm^{-1} for voids within the Cu_3Sn layer. On the other hand, the samples annealed at 200 °C for 1440 min had the lowest void fraction, i.e., 0.03 μm^{-1} at the $Cu–Cu_3Sn$ interface.

Since the voids are arbitrary and cannot be avoided at all in the Cu–Sn diffusion stack, a compromise between the void size and void fraction should be made to obtain higher reliability of the bonding process. For the lower processing temperatures (< 200 °C), the samples had sub-micrometer size voids having a higher void fraction within the Cu_3Sn layer and lower void fraction at the $Cu–Cu_3Sn$ and the $Cu_3Sn–Cu_6Sn_5$ interface. It implies that the voids were randomly distributed in the IMCs and the interfaces. Since the void sizes are small and cover a minor share of the Cu–Sn bonded area, it can be accepted to attain improved reliability of the packaging than the larger voids formed at higher processing temperatures. In the case of high processing temperature, sometimes voids can be so large that the IMC layer gets delaminated from the base Cu [20, 30] resulting in the catastrophic failure of the packaging.

4 Conclusion

Cu–Sn solid-state diffusion stack has been investigated to understand the IMC growth and the void formation with their correlation at temperatures below the melting point of Sn (232 °C), i.e., at 150 °C, 175 °C, and 200 °C. At low annealing temperatures, both Cu_6Sn_5 and Cu_3Sn were observed to have scalloped shaped growth; however, Cu_6Sn_5 IMC had larger scallops, and the Cu_3Sn IMC had smaller scallops. The diffusion parameters and activation energy for both Cu_3Sn and Cu_6Sn_5 were experimentally obtained to be 2.35×10^7 μm^2 min^{-1}, 77.26 kJ mol^{-1} K^{-1}, and 7.55×10^3 μm^2 min^{-1}, 37.46 kJ mol^{-1} K^{-1}, respectively. The diffusion coefficients were compared with those reported in the literature and were observed to be on the higher side since the base copper was 99.9% pure rather than electrodeposited copper. The activation energy was in close agreement with those noted in the literature. Void growth result obtained in this study implies that for low annealing temperatures, the largest void sizes were formed at $Cu–Cu_3Sn$ interface with the least void fraction. The highest void fraction was observed for voids within Cu_3Sn with the least void sizes. Large voids at $Cu–Cu_3Sn$ interface for samples annealed at

200 °C has been observed to retard IMC growth by reducing the active diffusion area. The void size was measured to be less than 3 μm for all the experimental conditions. Cu–Sn diffusion bonding has an optimistic potential for low temperature highly reliable hermetic packaging of MEMS structures. The obtained experimental results can be used in the hermetic packaging of MEMS devices performed at low temperatures (≤ 200 °C). It will not only reduce the problem of molten Sn squeezing out but also reduce the thermomechanical stresses generated during the conventional SLID bonding.

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