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A comparison of electrical parameters of Au/n-Si and Au/($CoSO_4$–PVP)/n-Si structures (SBDs) to determine the effect of ($CoSO_4$–PVP) organic interlayer at room temperature

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Abstracts

In this study, the Au/n-Si structures with and without ($CoSO_4$–PVP) organic interlayer were fabricated on the same n-Si wafer and electrical characteristics of them were analyzed by using current, capacitance, and conductance measurements in forward and reverse bias voltages and experimental results were compared with each other. The values of ideality factory (n), zero-bias barrier height (Φ_{Bo}), and the rectifying ratio (RR at ± 3 V) for Au/n-Si and Au/($CoSO_4$–PVP)/n-Si structures were found as 2.453, 0.732 eV, 2.01×10^3 and 2.489, 0.799, 5.37×10^4 by using the I–V measurements, respectively. The RR of Au/($CoSO_4$–PVP)/n-Si structures at ± 3 V was 26.77 times higher than Au/n-Si structure. The concentration of donor-atoms (N_D), Fermi energy (E_F) and barrier height for these two structures were found as 15.06×10^{14} cm^{-3}, 0.254 eV, 0.744 eV and 2.310×10^{14} cm^{-3}, 0.303 eV, 1.010 eV from the C^{-2}–V characteristics in the reverse bias region at 1 MHz in dark, respectively. These results show that the use of ($CoSO_4$–PVP) polymer interface layer at Au/n-Si interface improves the performance of these structures. Additionally, a simple ultrasound-assisted method has been utilized to grown cobalt sulfide nanostructures. The morphological and structural analyses of them have been investigated by scanning electron-microscopy, and X-ray diffraction methods.

1 Introduction

Metal–semiconductor (MS) structure have very fast switching characteristics and very low forward-voltage drop and usually studies are focused on the increase of performance and reliability of MS type SBDs because they have both the forming fundamental piece of the device technology and important role in electronics and opto-electronics device applications [1–5]. Unless a specially fabricated of MS type SBDs/structures, a native insulator layer can be occurred at M/S interface, and so MS type SBD will be converted to the MIS type SBD like a capacitor which can be stored many charges and shows dielectric properties. The existence such insulator, polymer and ferroelectric interfacial layer in the MIS, MPS, MFS type structures will be strongly influenced both the performance and conduction mechanisms in these type electronic devices [6–10]. But, the formation of a low-dielectric insulator layer (SiO_2, SnO_2, Si_3N_4) by the traditional method cannot act passivate of the active dangling-bonds at the surface of semiconductor. For these reasons, recently, many researchers are focused on the improving the electric, dielectric and optoelectronic properties of these devices [11–14]. An interfacial polymer layer has high- surface area to volume rate, low weight, low cost, low consumption energy, good mechanical strength, the capacity charge-storage, flexibility, big-dielectric-constant, easy and cheap preparing methods including electro-spinning, sol–gel, solid–liquid phase separation and template synthesis [15–21]. Therefore polymers such as PVA and PVP have become more important research subject because of its high-water solubility, high-film formation

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capacity and, thereof its conductivity can be increased by a suitable doping meatal or metal-oxides such as Zn, Co, Ni, $CuSO_4$, ZnO, Bi_2O_3, and SnO_2 via the high-physical interactions between organic chains, and hydrogen-bonding between hydroxyl-groups and dopant-materials [17–24].

The values of Φ_B, n, N_{ss}, series and shunt resistances (R_s, R_{sh}) are used to determine the performance of MS, MIS, MPS, and MFS type structures/SBDs by using the I–V, C–V, and G/ω–V measurements in the wide range of voltage as well as frequency and temperature [9–12]. In recently, there are many studies in the literature on the characterizing and optimizing electrical parameters of polymer based SBDs by using different polymer layers on semiconductors [1–7, 13–27]. Among these researches, Aydemir et al. [20] studied on comparative of the electrical parameters of MS and MPS structures which are performed on the n-Si, Çetinkaya et al. [21] studied on comparative of electrical properties for Au/(GP-doped PVA)/n-Si (MPS) fabricated with different rates graphene and Altındal-Yerişkin et al. [22] studied on comparative of the electrical properties for MS type SDs by using (graphene doped-PVA) polymeric interfacial layer between metal and semiconductor and they reported the RR of the MPS structure at ± 3 V was found at about 493-times higher than the MS structure. Reddy et al. [23] were also observed that the magnitude of N_{ss} Au/polyvinylidene-fluoride/n-InP structure is ten times lower than Au/n-InP type structure due to the dangling-bonds saturation by an organic interlayer. Although all of these studies; the interfacial layer effect on the performance of MS type SBDS and conduction mechanisms and also the origin of N_{ss} and R_s is not enough clarified yet. Additionally, $CoSO_4$ is generally used in storage batteries and electrochemical industries because it has strong absorption in shorter wavelengths and magnetic properties [28–30]. There are very few studies in the literature related to $CoSO_4$ and these are generally related to properties such as optical, thermal, thermodynamic and magnetic of $CoSO_4$ [28–33]. However, there are hardly studies related to electrical properties of $CoSO_4$.

Due to the above explanations, in this study, we aimed to the fabricated both the Au/n-Si and Au/($CoSO_4$–PVP)/n-Si structures and compare their physical characteristics in order to determine the whether or not improve the electric properties by the way of passivation active dangling bonds at the semiconductor. Therefore, I–V, C–V and G/ω–V characteristics were performed in wide range voltages considering the effects of N_{ss}, R_s and organic interlayer. Experimental results show that the used ($CoSO_4$–PVP) interfacial layer improves the performance of MS structure through decreasing the active dangling bonds and the leakage current, N_{ss}, and increasing the rectifying ratio (RR), and BH. Therefore ($CoSO_4$–PVP) interfacial layer can be successfully used instead of the conventional interfacial insulator layer and gives also them capacitor properties, which more and more storage electric charges or energy.

2 Experimental details

2.1 Synthesis of the cobalt sulfate–cobalt sulfide nanostructures and fabrication of Au/(cobalt sulfate–cobalt sulfide/PVP)/n-Si structure

Cobalt acetate hydrate $(CH_3CoO)_2Co{\bullet}4H_2O$ with purity greater than 99%, and sodium sulfide (Na_2S) with purity greater that 99% was purchased from Loba chemie company, double distilled water was used as solvent and washing agent material. Polyvinylpyrrolidone (PVP) was also purchased from Loba chemie. All of the chemicals were used without further purifications.

The cobalt sulfate–cobalt sulfide nanostructures were synthesized by ultrasound-assisted method. In a typical preparation method, 0.10 g of cobalt acetate and 0.96 g of sodium sulfide were dissolved in 20 ml of double distilled water separately. Then these solutions were added together in a flat bottom baker and simultaneously kept under ultrasonic irradiation for 15 min in open air, using a high intensity ultrasonic processor. The result material centrifuged and washed for five times with distilled water, then the powder form of the nanostructures was dried at room temperature and used for fabrication of Au/(cobalt sulfate–cobalt sulfide/PVP)/n-Si structure. For fabrication of Au/(cobalt sulfate–cobalt sulfide/PVP)/n-Si structure, at first, n-type semiconductor Si wafer was cleaning in an ultrasonic-bath and then high-pure Au (99.999%) was grown on the back side of the n-Si wafer at about 10^{-6} torr. Immediately, it annealed at 550 °C at 5 min in the N_2 ambient to get low-resistivity ohmic contact followed by the preparation of (cobalt sulfate–cobalt sulfide)/PVP nanostructures on n-Si wafer by utilizing spin coating method. 0.1 g of the prepared nanostructures in the powder form was dissolved in 2 ml of aqueous solution of PVP polymer (5%). A drop of the solution was coated by spin coating techniques. Finally, Au dots (7.85×10^{-3} cm^2) were thermally grown on the (cobalt sulfate–cobalt sulfide/PVP). I–V and C/G–V measurements were performed by a Keithley 2400 source meter and HP4192A LF impedance analyzer with the help of an IEEE-488 AC/DC converter card.

2.2 X-ray diffraction measurement

The structure of the prepared cobalt sulfate–cobalt sulfide nanostructures is depicted in Fig. 1. The observed XRD

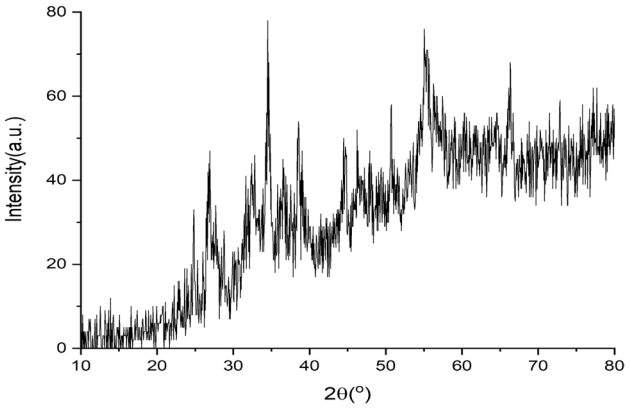

Fig. 1 XRD pattern of the synthesized cobalt sulfate–cobalt sulfide nanostructures

peaks in Fig. 1 are well matched with those of mixture of cobalt sulfate and cobalt sulfide nanostructures.

2.3 FE-SEM and EDS measurement

Both the surface-morphology and elemental-analyses of the prepared samples were characterized by field emission (FE)-SEM and EDS and depicted in Figs. 2 and 3, respectively.

It is hard to see the real particle sizes using FE-SEM, however, an overview from the images depicts formation of polydispersity and agglomerated nanostructures with different geometries. As shown in Fig. 2a, b, there are some small nanoparticles.

The quantitative elemental analyses of the synthesized cobalt sulfate- cobalt sulfide nanostructures were carried

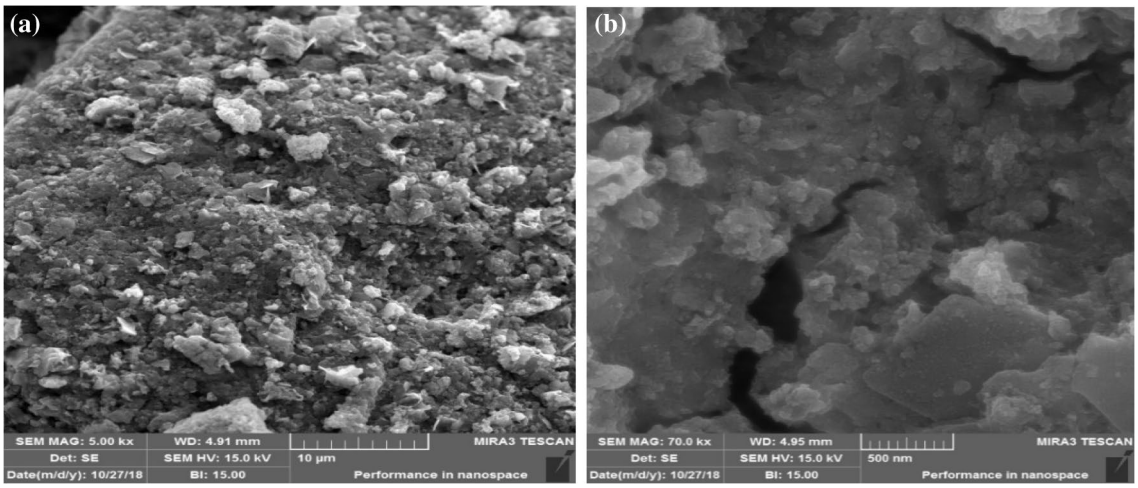

Fig. 2 **a**, **b** FE-SEM images of the synthesized nanostructures in different magnifications

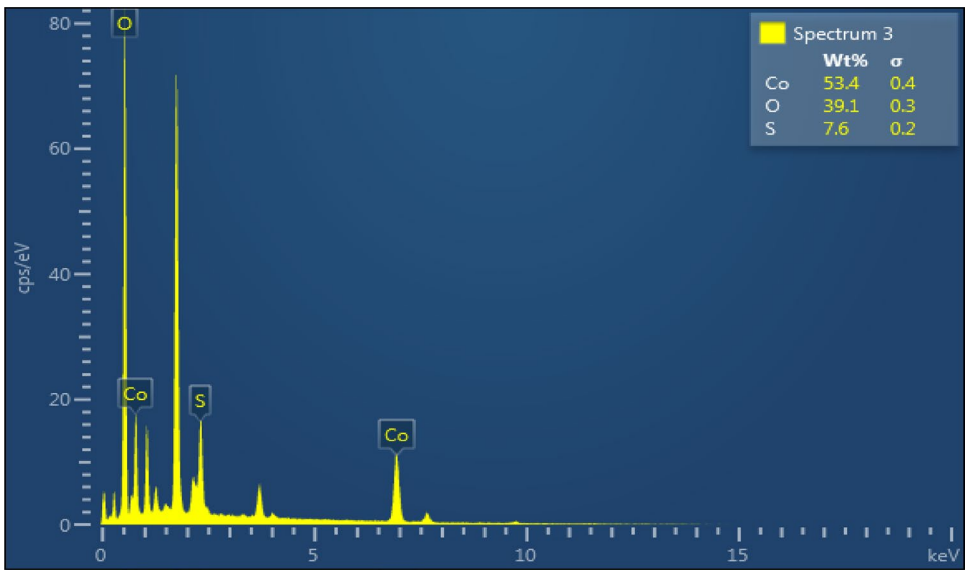

Fig. 3 EDS spectrum of the synthesized cobalt sulfate–cobalt sulfide nanostructures

out using the EDS technique. Figure 3 depicts typical EDS spectrum, which shows the product contains cobalt, sulfur and oxygen materials with ratio 53:8:39 in weight percent respectively.

3 Results and discussion

3.1 Forward and reverse bias I–V characteristics at room temperature

Figure 4 shows the typical semi-logarithmic I–V plots of the Au/n-Si structure with and without ($CoSO_4$–PVP) organic interlayer at ± 3 V, and they show good saturation behavior for the reverse bias voltages and RR (= I_F/I_R at ± 3 V). The value of I_F increases up to ~ 0.5 V almost as exponentially and then deviates from the linearity due to the effects of R_s and interlayer. In general, TE theory is used for the extraction of electrical parameters of SBDs. According to TE theory, the relationship between I_F and V_F (≥ 3 kT/q) can be expressed as following [9–12].

$$I = \underbrace{AA * T^2 \exp\left(-q\varphi_{Bo}/kT\right)}_{Io}\left\{\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right\} \tag{1a}$$

In Eq. (1a), A^* is the Richardson constant (120 A/(cm K)^2 for n-Si) and the other quantities are well-defined in the available literature [9, 11]. The reverse-saturation current ($_o$) which is obtained from the linear part of ln(I)–V plots at zero-bias voltage. On the other and, the values of n can be obtained from the of slope of ln(I_F)–V plots.

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln(I))}\right) \tag{1b}$$

After the extraction of I_o values from the forward bias ln(I)–V plots, the values of zero-bias BH (Φ_{Bo}) can be calculated by using Eq. 1c.

$$\Phi_{Bo} = \frac{kT}{q}\ln\left(\frac{AA * T^2}{I_0}\right) \tag{1c}$$

As shown in Fig. 1, the values of RR of the MPS structure at ± 3 V was found 26.77 times higher than the Au/n-Si (MS) type SBD.

Both the series and shunt resistances (R_S, R_{SH}) are also important parameters of the SBDs which are more affecting the performance and quality of them and they can be calculated from the structure resistance (R_i) versus V plots. Thus, to examine voltage dependent of R_i for two type SBDs, the R_i–V plots calculated by using Ohm's Law ($R_i = dV_i/dI_i$) are presented in Fig. 5. As can be clearly seen in Fig. 5, the values of R_i approach to a constant value which are corresponding the real values of R_S and R_{SH}, respectively. Thus, the obtained experimental values of n, I_o, Φ_{B0}, R_s R_{SH} and RR for the MS and MPS structures were tabulated in Table 1.

In order to evaluate the current-transport in more detail, the In(I_F)–In(V_F) plot of the MS and MPS structures were drawn and given in Fig. 6.

As can be seen in Fig. 6, In(I)–In(V) plots for two type SBDs have three district linear regions in the form of $I \propto V^m$ and the slope of these regions are different from each other.

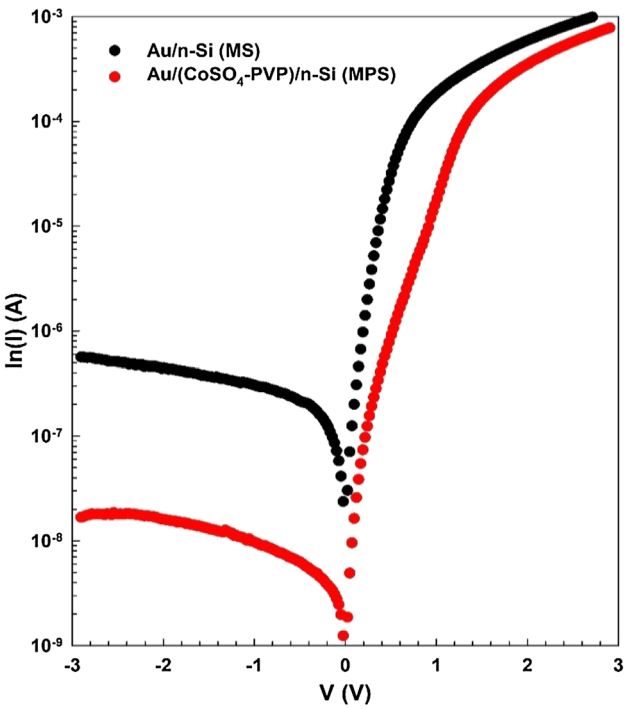

Fig. 4 The lnI–V plots of the MS and MPS structures at room temperature

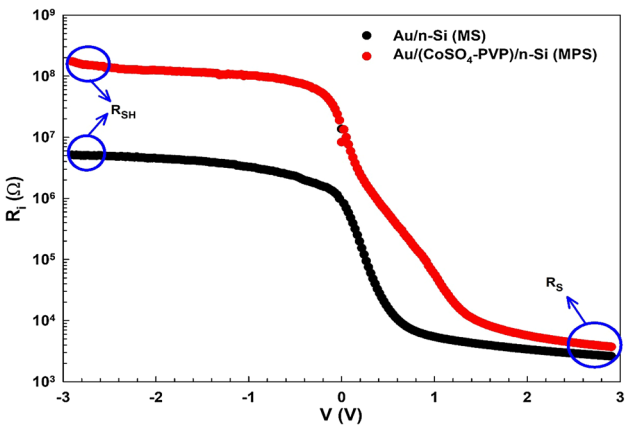

Fig. 5 The lnR_i–V_i plots of the MS and MPS structures at room temperature

Table 1 The values of n, I_o, Φ_{Bo}, R_s R_{SH} and RR for the MS and MPS structures extracted from the I–V characteristics at room temperature

Diodes	n	I_o (A)	Φ_{Bo} (eV)	R_s (kΩ)	R_{SH} (kΩ)	RR (at ± 3 V)
(Au/n-Si) (MS)	2.453	4.43×10^{-8}	0.732	2.57	5.1×10^{3}	2.01×10^{3}
(Au/($CoSO_4$–PVP)/n-Si) (MPS)	2.489	3.30×10^{-9}	0.799	3.64	1.9×10^{5}	5.37×10^{4}

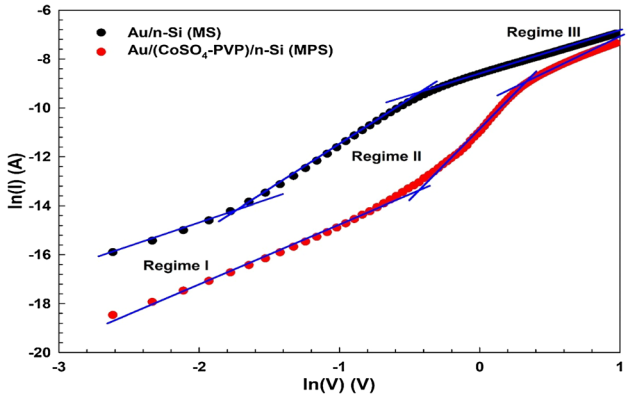

Fig. 6 The $In(I_F)$–$In(V_F)$ plots of the MS and MPS structures at room temperature

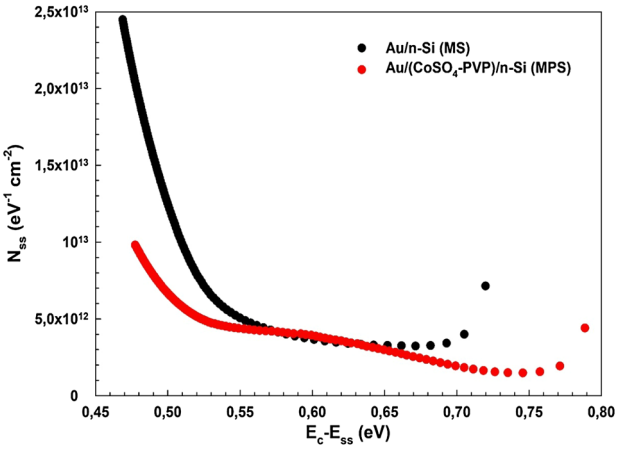

Fig. 7 The energy-dependent profiles of N_{ss} for MS and MPS structures at room temperature

Where, m represents the slope of each linear region. For each SBD, these regions are named as regimes I, II and III, respectively. Region I is corresponding to the low voltages and for MS and MPS type SBDs and in this region the conduction mechanism (CM) exhibits an ohmic behavior [34–37]. Regime II is corresponding to the intermediate voltages and CM is characterized by power law dependence and it can be explained by trap-charge limited current (TCLC) [37, 38]. Regime III is corresponding to the high forward-bias voltages and many electrons can escape from the traps and contributes to space-charge-limited-current (SCLC) [10, 35, 38, 39].

The surface states or interface traps (N_{ss}/D_{it}) play a key role in the conduction mechanism in SBDs. Because, the existence of N_{ss} localized between interfacial layer and semiconductor is dominate on the I–V and C/G–V characteristics in these devices. The energy-dependent profile of N_{ss} as deduced by Card–Rhoderick can be extracted from the forward bias I–V plot considering voltage dependent BH (Φ_e) and n by using Eqs. 2a and 2b, respectively [10, 12, 39, 40]:

$$n(V) = \left(\frac{q}{kT}\right)\left(\frac{V}{\ln(I/I_o)}\right) \tag{2a}$$

$$\varphi_e = \varphi_{Bo} + \left(1 - \frac{1}{n(V)}\right).V \tag{2b}$$

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right] \tag{2c}$$

In Eq. 2c; δ, ε_0, W_D, ε_i and ε_s are corresponding to the interfacial layer thickness, the permittivity of vacuum ($=8.5\times10^{-14}$ F/cm), the width of depletion region, the permittivity of interfacial layer and semiconductor, respectively. The value of W_D was obtained from the intercept of C^{-2}–V plots at 1 MHz for MS and MPS type structures. The energy of surface states (E_{ss}) with respect to edge of conduction band (E_c) for n-type semiconductor is represented as following [12]:

$$E_C - E_{ss} = q(\varphi_e - V) \tag{3}$$

Thus, N_{ss} versus ($E_c - E_{ss}$) plots for the MS and MPS type SBDs were extracted by using Eqs. (2a)–(2c), (3) and presented in Fig. 7. As can be seen in Fig. 7, the N_{ss} values decrease from conduction band towards to the mid-gap of n-Si for two types SBDs. Additionally, the magnitude of N_{ss} for MPS structure is lower than MS structure because of the dangling bonds saturation due to the use of ($CoSO_4$–PVP) organic interlayer.

3.2 The forward and reverse bias C/G–V Characteristics at 1 MHz

Figures 8 and 9 show both the C–V and G/ω–V plots of the MS and MPS structures at 1 MHz, respectively. As shown from the Figs. 8 and 9, both the C–V and G/ω–V curves have inversion, depletion and accumulation regions

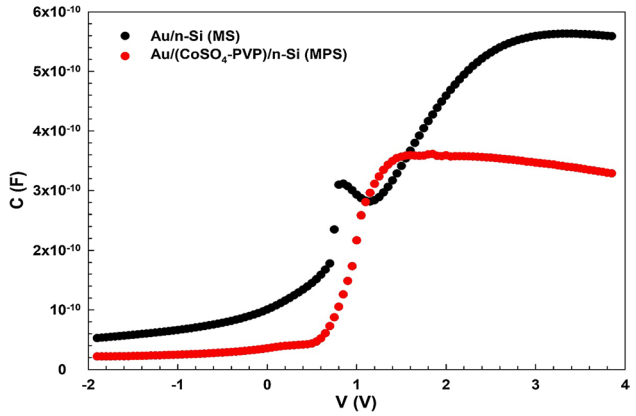

Fig. 8 The C–V plot of the MS and MPS structures for 1 MHz at room temperature

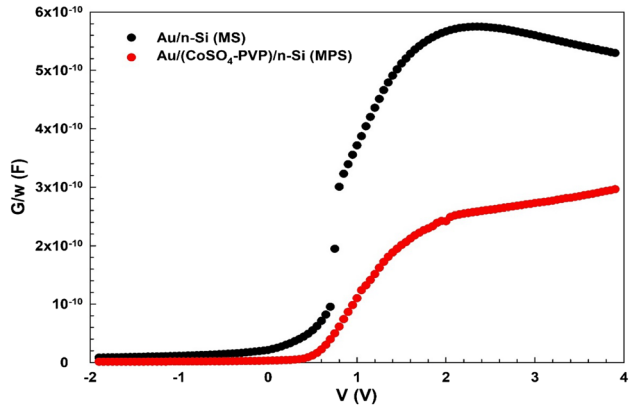

Fig. 9 The G/w–V plot of the MS and MPS structures for 1 MHz at room temperature

similar to a MOS capacitor or structure. It is clear that the C–V plot for the MS structure has a distinctive peak in the depletion region, but it becomes disappeared for the Au/($CoSO_4$–PVP)/n-Si (MPS) type SBD (Fig. 8). Such behavior in the C–V plot for the MPS type SBD is the result of passivation of active dangling-bonds in the semiconductor crystalline thanks to the used of ($CoSO_4$–PVP) interfacial layer. Because, un-passivated surface states (N_{ss}) and bulk traps can be stored and released many charges under forward applied bias voltage, leading to an increase or decrease. Additionally, both the C–V and G/ω–V plots may be given some peaks due to a special density distribution of N_{ss} and dislocations between interfacial layer and semiconductor in the forbidden energy bandgap of semiconductor [10, 12, 13, 39]. The concave curvature in the C–V plots at accumulation region is the results of R_s and interfacial layer. That is while the N_{ss} are especially dominate in depletion and inversion regions, R_s and interfacial layer are dominate only

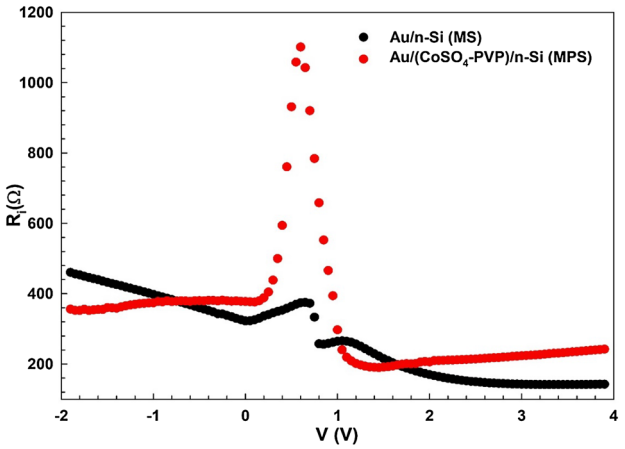

Fig. 10 The R_i–V plots of the MS and MPS structures for 1 MHz at room temperature

at accumulation region. According to Nicollian and Brews [10, 39, 41, 42],

In order to emphasis the effect of R_s both on the C–V and G/w–V characteristics, voltage dependent profiles of R_i was extracted from the Eq. 4, proposed by Nicollian and Brews [41] and were given in Fig. 10. As shown in Fig. 10, the value of R_i becomes almost a constant at accumulation region and so it corresponds the real value of R_s for MS and MPS structures.

$$R_s = G_m / \left[G_m^2 + \left(\omega C_m \right)^2 \right] \tag{4}$$

In Eq. 4, ω is the angular frequency, C_m and G_m values are capacitance and conductance measured at a given bias voltage, respectively. The peak behavior in the R_i–V plot for two type SBDs are results of particular density distribution of N_{ss} between interface layer and semiconductor and their relaxation times, restructure and reordering of N_{ss} under applied bias voltage. The effect of R_s can be neglected low at low frequencies and in inversion region contrary to high frequencies and at accumulation region.

In order to examine the changes in some main electrical parameters such as $\Phi_{B(C-V)}$, the Fermi level (E_F), donor concentration atoms (N_D) and diffusion potential (V_D); the C^{-2}–V plots were also drawn and given in Fig. 11 for the MS and MPS structures for 1 MHz. As shown in Fig. 11, the C^{-2}–V plots for each SBDs have a straight line in the wide range of voltage. Thus, the values V_D, N_D, E_F, $\Phi_{B(C-V)}$, and W_D are calculated from the intercept and slope of these plots for two type SBDS by using following equations [9, 10, 39] and represented in Table 2.

$$\phi_{B_{(C-V)}} = V_D + E_F - \Delta\phi_B \tag{5}$$

In Eq. 5, V_D ($=V_o+kT/q$) is the diffusion potential at zero bias, and $\Delta\Phi_B$ is the image force barrier lowering. After the

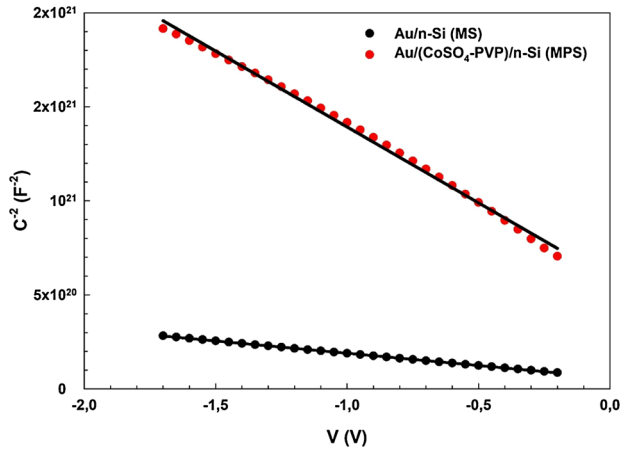

Fig. 11 The C^{-2}–V plots of the MS and MPS structure for 1 MHz at room temperature

obtained value of N_D and V_D; the values of E_F and W_D are calculated by using following relations [39, 41].

$$E_F = \frac{kT}{q} \ln\left(\frac{N_C}{N_D}\right) \tag{6a}$$

$$W_D = \left(\frac{2\varepsilon_s V_D}{qN_D}\right)^{\left(1/2\right)} \tag{6b}$$

In Eq. 6a, N_C is the effective density of states in the Ec band, $m_e^* = 0.98m_0$ for electrons, and h ($=6.62\times10^{-34}$ J s) is the Planck constant, respectively.

$$N_C = 4.82x10^{15}T^{3/2}\left(m_e^*/m_0\right)^{3/2} \tag{7}$$

The values of maximum electric field (E_m) at junction and image force barrier lowering ($\Delta\Phi_B$) is were also calculated by using following relation [10, 39]:

$$E_m = \left(\frac{2qN_D V_0}{\varepsilon_s \varepsilon_0}\right)^{1/2} \tag{8a}$$

$$\Delta\varphi_B = \left(\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}\right)^{1/2} \tag{8b}$$

Thus, the obtained experimental values of V_0, N_D, V_D, E_F, E_m, Φ_B(C–V) and W_D for the MS and MPS type structure extracted from the C–V characteristics at room temperature and were tabulated in Table 2. When compared Tables 1 and 2, the obtained value of Φ_B(C–V) from reverse bias C^{-2}–V plots is higher than the Φ_{Bo}(I–V) from forward bias ln(I)–V plots for two structures due to the nature of measured method and voltage dependent BH. But, the value of BH obtained from both the forward bias I–V data and reverse bias C–V data for MPS structure is higher than the MS structure due to the formation of ($CoSO_4$–PVP) organic interlayer.

4 Conclusion

In order to determine the effect of ($CoSO_4$–PVP) polymer interlayer on the electrical characteristics, the MS MPS structures were performed on the same n-Si wafer. For this purpose, electrical characteristics of them have been investigated by using the I–V, C–V, and G/ω–V measurements in a wide range of voltage and compared with each other. The values of n, Φ_{Bo} and the RR (at ± 3 V) for the MS and MPS type SBDs were obtained as 2.453, 0.732 eV, 2.01×10^3 and 2.489, 0.799, 5.37×10^4 by using the I–V measurements in dark, respectively. The value of RR for MPS is also 26.77 times higher than the MS structure. In addition, the other some experimental values of these SBDs such as N_D, E_F and BH were found as 15.06×10^{14} cm^{-3}, 0.254 eV, 0.744 eV and 2.310×10^{14} cm^{-3}, 0.303 eV, 1.010 eV from the C^{-2}–V characteristics at 1 MHz, respectively. Obtained the value of $\Phi_{B(C-V)}$ from reverse bias C–V data is higher than the $\Phi_{Bo(I-V)}$ from forward bias I–V data for two structures due to the nature of the measured method and voltage dependent BH. Additionally, the value of BH obtained from both the forward bias I–V data and reverse bias C–V data for MPS is higher than the MS structure due to the used of ($CoSO_4$–PVP) organic interlayer. These results show that the use of ($CoSO_4$–PVP) polymer interface layer at Au/n-Si interface improves the performance of the structure and so can be successfully replaced in the insulator layer in the future.

Table 2 The values of V_0, N_D, V_D, E_F, E_m, Φ_B(C–V) and W_D for the MS and MPS structures extracted from the C–V characteristics at room temperature

Diodes	F (MHz)	V_0 (V)	$N_D\times10^{15}$ (cm^{-3})	V_D (eV)	E_F (eV)	$E_m\times10^3$ (V/cm)	Φ_B (C–V) (eV)	$W_D\times10^{-4}$ (cm)
(Au/n-Si) (MS)	1	0.464	1.506	0.489	0.254	14.625	0.744	0.634
(Au/($CoSO_4$–PVP)/n-Si) (MPS)	1	0.681	0.231	0.706	0.303	6.946	1.010	1.961

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