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A comparative study on current/capacitance: voltage characteristics of Au/n-Si (MS) structures with and without PVP interlayer

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Abstract
In order to determine the Polyvinylpyrrolidone (PVP) effect on electrical characteristics, Au/n-Si (MS) structures with and without PVP interfacial layer were fabricated. After that their main electrical parameters were extracted from the forward and reverse biases I–V, and C/G–V measurements at room temperature. The experimental characteristics (I–V) show the MPS structure with high rectification ratio ($RR = I_F/I_R$ at $\pm 4V$), shunt resistance (R_{sh}) and zero-bias barrier height (Φ_{B0}) and lower leakage current, ideality factor (n), surface states (N_{ss}) compared with the MS structure. RR and the reverse saturation current (I_o) for MPS are 55 times higher and 54 times lower than RR and I_o for MS, respectively. The voltage dependent n, effective barrier height (Φe) and energy dependent profile of N_{ss} for two types structures are acquired by considering the forward biases I–V data. They were found vary from 1.074×10^{12} $eV^{-1}cm^{-2}$ (at $E_c - 0.821$ eV) to 3.55×10^{13} $eV^{-1}cm^{-2}$ (at $E_c - 0.409$ eV) for MPS and 3.85×10^{13} $eV^{-1}cm^{-2}$ (at $E_c - 0.724$ eV) to 5.67×10^{13} $eV^{-1}cm^{-2}$ (at E_c-0.405 eV) for MS structure. R_s, n and Φ_{B0} parameters were also found from the Cheung function as 272.4 Ω, 6.17, and 0.964 eV for MPS and 79.2 Ω, 3.38, and 0.708 eV for MS structure as second way. Some electrical parameters of the structures such as concentration of donor atoms (N_D), Fermi energy level (E_F) and BH were also found reverse bias C^{-2}–V characteristics for 100 kHz. The use of PVP polymer interlayer considerably improves the efficiency of the MS structure. The way to replace the traditional insulator interlayer concluded as; reducing the N_{ss} alternatively, leakage current and increase of RR, Φ_{B0}, and R_{sh}, respectively.

1 Introduction

In last two decades, metal–semiconductor (MS) with and without an interlayer such as insulator, polymer and ferroelectric layer (MIS, MPS and MFS) Schottky type structures have been great importance in electronic and optoelectronic applications [1–10]. But, the effects of interlayer, surface states (N_{ss}), series and shunt resistances (R_s and R_{sh}) on the conduction mechanisms and performance is not fully understood yet. Therefore, the investigation of conduction mechanisms and increase of performance in these structures are still an important problem. For these reasons, there are many studies to improve both the electric and dielectric properties by using a high-dielectric interfacial layer such as $BaTiO_3$ [5], $Bi_3Ti_4O_{12}$ [11, 12], $SrTiO_3$ [13]:Aysel and polymer or polymer composite such as NiPc [14], PEDOT:PSS [15], polyvinylidene fluoride (PVDF) [16], Zn-PVA [17, 18], (0.07-graphene doped-PVA) [9] and Ag/(0.03 Ru-PVP) [19]. Among them, especially polymer or polymer composites have been a new and interesting study for physicists and chemists due to their flexibility, cost efficiency, good performance, low molecular weight, wide production area and easy technical process ability compared to traditional inorganic based materials [20]. Among these polymers, especially Polyvinylpyrrolidone (PVP) and PVA are water-soluble and nontoxic polymers and they have wide range of crystallinity, high dielectric strength, lower conductivity and better charge storage capacity. However, providing a high-dielectric interfacial layer in MS structures provides us with some advantages such as maintaining a constant and controllable barrier height (BH), reducing magnitude of N_{ss}, R_s and leakage current, and increasing both the rectifying rate ($=I_F/I_R$) and R_{sh}. Main performance and quality of related structures depend on many factors, but the BH formation, interlayer, and N_{ss} between MS are more effective on the performance of them [1, 9, 11–13].

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Recently, N_{ss} in PVDF interlayered MPS structure was found by Reddy about lower factor of one than that of Au/n-InP MS [16]. Yerişkin et al. [9] were prepared a Au/n-Si metal semiconductor structure with/without graphene doped PVA interlayer and observed that N_{ss}, R_s and leakage currents are remarkably diminished. Gökçen et al. [21] studied the forward bias were also investigated the I–V characteristics of the same MS structure with and without Bi_2O_3 interlayer and they found out that a decrease in MS structure's N_{ss} and leakage currents. Similarly, Aydemir et al. [18] show that the Zn-doped PVA interlayer usage remarkably reduced the structure's surface states and leakage currents. The value of R_s can be occurred from the front and back contacts, the bulk semiconductor's resistance or donor/acceptor atom's doping concentrations, the contact made to the connecting wire by front/rectifier contact, dirty film or the back contact may be due to various reasons [5]:Niccolian/[22]:P. Chattopadhyay 1996 [23]. In recent works, there are many calculation methods for R_s such as Ohm's law, Norde [24], Cheung [25], and Norde functions which are modified by Bohlin [26]. The Ohm Law is the simplest method among the others. According to this method, the calculation of the actual R_s value in sufficiently high biases is generally agreed. However, I–V plot's concave curvature at forward biases is the calculation way of the Norde and Cheung functions. Additionally, Ohms law has a significant advantage to specify the series and shunt resistances estimation.

The first goal of this study is to fabricate Au/n-Si structures with and without polyvinylpyrrolidone (PVP) interlayer to uncover the effect of this layer on electrical characteristics. The second goal is to discuss in detail the role of N_{ss}, R_s and R_{sh} in these structures and to indicate the limitations in the standard evaluation methods which make use of these characteristics for the evaluated of the various electric parameters such as BH, the doping atoms concentration, ideality factor, and depletion layer width. In order for that I–V and capacitance/conductance C/G–V measurements at all biases are carried out in the wide range of voltages. All these results are verified that the PVP polymer interlayer usage at Au/(PVP) interface are considerably improve the MS structure's performances. Hence, it can alternatively be implemented instead of the traditional insulator interlayer for reducing the N_{ss}, leakage current, increase of RR, Φ_{B0}, and R_{sh}.

2 Experimental details

In this study, both MS structures with and without PVA interlayer were produced on the n-type silicon [n-si,(100)] wafer with 350 μm thickness and 1–10Ω.cm resistance as a substrate in the same conditions. Firstly, n-Si wafer was immersed in methanol and then rinsed in de-ionized water with 18MΩ. cm resistivity. Followingly, it was etched in a hot solution of H_2O, NH_4OH and H_2O_2 (65:13:13 v/v). After that, n-Si wafer was again rinsed in de-ionized water at about 10 min in the ultrasonic bath. Secondly, n-Si wafer was etched in a solution of H_2O: HF (24:1 v/v). After that it was rinsed with de-ionized water and dried by dry nitrogen (N_2) gas. After these steps of cleaning process in ultrasonic bath, higher purity Au (99.995%) with 1200 Å thickness was evaporated onto the entirely back side of the n-Si wafer at 10^{-6} Torr pressure in metal evaporating system. To carry on the lower resistivity back contact, for 5 min time at 500 °C, Au coated n-Si wafer was sintered under a N_2 atmosphere. PVP (Polyvinylpyrrolidone) (MW 40.000) was supplied from the Sigma-Aldrich.

After the ohmic contact was performed, high-pure Au dots with diameter of 2 mm were grown on n-Si wafer in the high-vacuum metal evaporation system. In this manner, the fabrication process was completed for first type (Au/n-Si) MS structure. In order to perform the second type MPS structure, PVP solution was prepared by dissolving the PVP in ultra-pure water. Preparation of the solution, 1gr of PVP was added to 9 gr of ultra-pure water and mixed for 5 min with a magnetic stirrer. The coating was carried out in two stages. In the first step, films were spin- coated at 2000 rpm for 30 s, and in the second step it was 4000 rpm for 30 s. Thus, the growing process of the prepared PVP solution was realized on the n-Si wafer's upfront by using spin coating technique (device type Spin 150i version at software polospro v3.16). Finally, Au rectifying contacts as circular dots with 1200 Å thick and 2 mm diameter were evaporated on the top of PVP layer through a metal shadow mask in the same high vacuumed metal evaporating system. So, the fabrication of the second type MPS structures was also finished. The measurements at all biases were completed by Keithley 2400 source meter and HP4192A LF impedance analyser (5–13 MHz).

3 Results and discussion

3.1 Current–Voltage (I–V) characteristics for forward and reverse bias

Usually, thermionic emission (TE) is used to determine the basic electrical parameters of the MS type Schottky barrier diodes (SBDs) with and without an interlayer when $V \geq 3kT/q$. The relation between V and I in the forward bias region can be expressed according to the theory [27–29]:

$$I = \underbrace{AA^{*}T^{2}\exp(-q\Phi_{B0}/kT)}_{I_0}\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \quad (1)$$

Equation (1) represent the pre-factor as reverse-saturation current (I_o), the effective Richardson constant (A^*) (=112 A. $cm^{-2}K^{-2}$ for n-type Si) and well-known quantities are in the

literature [27, 28]. At all biases the LnI vs V characteristics for the fabricated Au/n-Si (MS) and Au /(PVP)/ n-Si (MPS) structures were shown in Fig. 1. As can be seen in Fig. 1, these semi-logarithmic I–V plots for two structures display a good rectification ratio in the voltage range of ±4V. It is clear that these plots have also a straight line for the wide range of applied forward biases and then deviated from the linearity stem from the R_s effect and native or deposited interlayer. On the other hand, the detected non-saturation behavior at reverse biases is the result of the image-force lowering barrier height, generation-recombination (GR), and the interlayer existence. When compared the LnI vs-V plot of MS and MPS structures, RR for MPS structure is about 55 times greater than the MS structure at ±4V. It is indicated that the (PVP) interlayer reduces the leakage current and increase of shunt resistance (R_{sh}).

While the value of I_o for two type diodes (MS and MPS) is subtracted from the intersection of the lnI-V plot at zero bias voltage of the linear part (Fig. 1), the value of n is obtained from the linear part of this plot by using Eqs. (2) and (3), respectively [27, 28].

$$I_0 = AA^*T^2 \exp\left(\frac{q\Phi_{B0}}{kT}\right) \tag{2}$$

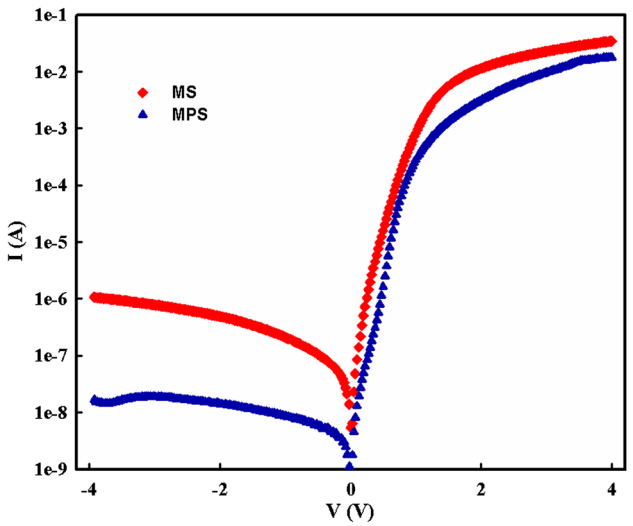

Fig. 1 The LnI vs V graph for non-interlayered and polymer interlayered structures

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln(I))}\right) \tag{3}$$

This experimental value of Io, diode area (A), and the theoretical value of effective Richardson constant (A^*) were obtained; the value of zero-bias barrier height (Φ_{Bo}) can be calculated by using Eq. (2) as following [27–29]:

$$\Phi_{B0} = \frac{kT}{q}\ln\left(\frac{A\cdot A^*T^2}{I_0}\right) \tag{4}$$

Thus, the basic electrical parameters values (I_0, n, Φ_{B0}) for both MS and MPS type structure are tabulated in the Table 1. In order to determine the quality of a diode, the other important parameter is the rectifier rate ($RR = I_F/I_R$ at sufficiently higher forward and reverse biases). For non-interlayered and polymer interlayered structures, this value is found separately as 1.97×10^4 and 1.09×10^6 at ±4V, respectively. It is clear that this value for polymer interlayered MS diode is almost 55 times greater than the non-interlayered MS structure. In other words, this shows that the leakage currents value can be reduced by using a thin interfacial polymer/organic layer instead of conventional/traditional insulator layer. In addition, as presented in Table 1, these values are 4.55×10^{-8} A, 3.13, 0.74 eV, 1.97×10^4 for the MS structure and 8.49×10^{-10} A, 2.53, 0.84 eV and 1.09×10^6 for the MPS structure, respectively. Φ_{B0} value for the MPS structure will be seen to be higher in the MS structure due to the decrement in electron tunneling of the value (PVP)/n-Si interface and the reduction in leakage currents. This interlayer at the M/S interface acts a physical barrier between Au and n-Si and also prevents inter-diffusion and reactions at M/S interlayer. In addition, the obtained experimental value of n for the two diodes is considerably higher than unity. The native or deposited concluded with interfacial layer, the density of surface states (N_{ss}), barrier inhomogeneity, image force effect, recombination-forming and tunneling along the barrier and patches results [1, 9, 16, 18]. But, the n value for polymer interlayered structure is lower than the other structure which is the result of passivation effect of (PVP) interlayer. All these results are confirmed to the grown of PVP between Au/n-Si as interfacial polymer layer enhances the quality of the structure. Comparing with MS structures, similar results have also been reported for MPS and MFS structures with Mn-ZnO [30], $BaTiO_3$ [1] and $Bi_4Ti_3O_{12}$ [31] interlayers.

Table 1 Comparison electrical parameters acquired from the I–V data of each structure

Samples	I_0 (A)	n	ϕ_{B0} (eV)	R_s (at 4V) (Ω)	R_{sh} (at -4V) (Ω)	N_{ss} (0.6V) ($eV^{-1}cm^{-2}$)	RR(±4V)
Au/n-Si (MS)	4.55×10^{-8}	3.13	0.74	115.54	3.7×10^6	1.63×10^{13}	1.97×10^4
Au/PVP/n-Si (MPS)	8.49×10^{-10}	2.53	0.84	224.59	1.8×10^8	0.67×10^{13}	1.09×10^6

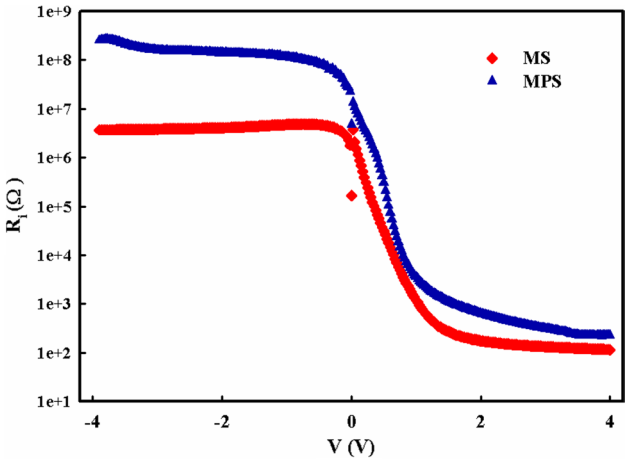

Fig. 2 The structure resistance (R_i) vs V graph of the non-interlayered and polymer interlayered structures

Both R_s and R_{sh} for the diode are also very significant parameters which are more affecting the I–V, C–V and G/ω–V characteristics of the MS structure with and without interfacial layer. Therefore, utilizing from Ohm's law, voltage dependent resistance (R_s) profiles were obtained from I–V data at all biases for the fabricated MS and MPS type structures and given in Fig. 2. The values of R_s and R_{sh} were found to be 115.54 Ω and 3.7×10^6 Ω for the MS and 224.59 Ω and 1.8×108 Ω for the MPS structure from Fig. 2, respectively As shown in these figure, the value of R_i ($=V_i/I_i$) is strong function of applied bias voltage especially at lower and moderate biases, but it becomes almost a constant at enough high forward and reverse biases (± 4 V). Thus, the real value of R_s and R_{sh} are corresponds to the adequate higher and reverse biases, respectively, and their experimental values of R_s and R_{sh} were also tabulated in Table 1, for two structures. Obviously, the R_{sh} value of for polymer interlayered structure is 49 times higher than the non-interlayered structure like RR. This value of R_{sh} converges to the ideal diode state for polymer interlayered structure.

Deviation from linearity occurs at higher biases for both structures stem from R_s and interlayer for forward-biases I–V characteristics. The values of R_s, n, and as a second way, these parameters were also specified from Cheung's functions [25].

$$\frac{dV}{d(lnI)} = \frac{nkT}{q} + IRs. \tag{5}$$

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) = n\phi_b + IRs \tag{6}$$

Figure 3a, b presents the dV/d(lnI) vs I and H(I) vs I plots for the MS and MPS structures. As can been showed in According to Eq. (3), the dV/d(ln I) versus I plots for two diodes have a good straight line or linear region in wide forward biases. Thus, the R_s and n values were obtained from the intercept and slope of these plots as 79.27 Ω and 3.376 for MS, and 272.36 Ω and 6.172 for MPS structure, respectively. By using the value of these ideality factor, the H(I) versus I plots were also drawn for two diodes and these plots indicate a well linearity in the same currents and biases. The R_s and BH were obtained from the intercept and slope of these plots as 75.47 Ω and 0.708 eV for non-interlayered structure and 359.66 Ω and 0.964 eV for the interlayered structure, respectively.

The modified Norde function was used for values of BH and R_S for the non-interlayered and polymer interlayered structures derived by applying the [24], stated as following:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{7}$$

Where I(V) calculated from the forward bias I–V, and γ is dimensionless integer and must be bigger than the ideality factor derived from the slope of ln(I)–V plots for two structures. Figure 4 shows the Norde function for forward applied voltage (V) as the MS and MIS structures

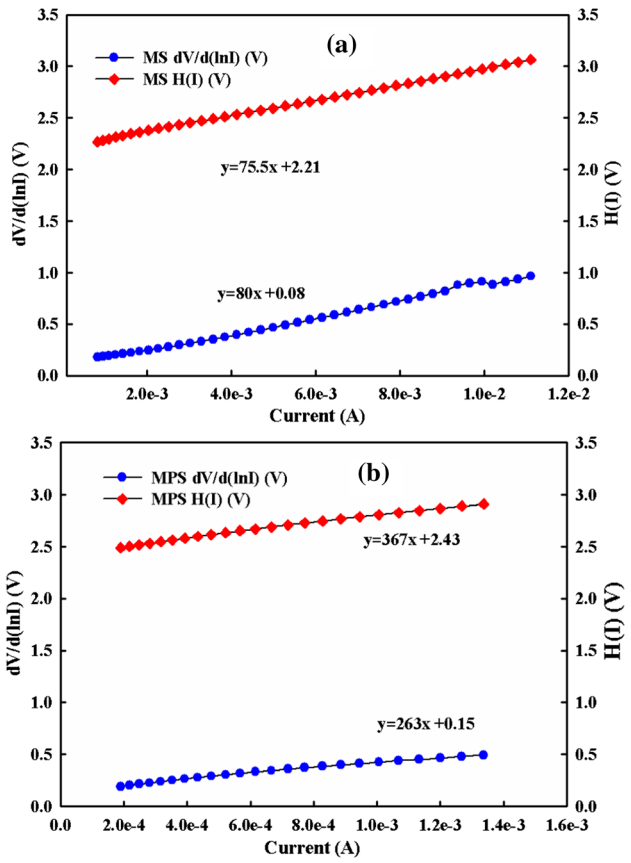

Fig. 3 Plots of dV/d(ln I)-I and H(I)-I for the **a** Au/n-Si (MS) structure and **b** Au/PVP/n-Si (MPS) structure

according to Eq. (7). The BH was obtained from the equation as follows:

$$\Phi_B = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q} \tag{8}$$

The minimum point of F(V) and V_0 is the corresponding voltage for F(V_0). Furthermore, the R_S value can be derived using the following relation:

$$R_s = \frac{kT(\gamma - n)}{qI_0} \tag{9}$$

Where I_0 corresponds to the minimum point F(V_0). Thus the values of BH and R_S were also obtained from the F(V_0) vs V plots as 0.734 eV and 113 Ω for the MS structure and 0.790 eV and 283 Ω for the MPS structure, respectively. The values of R_S obtained lower than using Norde's function comparison with Cheung's method may be due to the different region of the I–V. However, the nonlinear region are applied in Cheung's functions and the complete range of the forward-bias I–V characteristic can be used in the Norde function [24, 25]. But, in general, the values of n, Φ_B and R_s from various methods are generally good agreement one with another (Table 2).

In order to determine conduction system for controlling device behavior in the whole forward bias region, double-logarithmic I–V plots for Au/n-Si (MS) and Au/PVP/n-Si (MPS) structures were given in Fig. 5 at room temperature. As can been as clearly, the Ln(I) vs Ln(V) plots for two type structures have four different linear parts with different slopes which are called as I, II, III, and IV, respectively. They are an evidence to the existence four different current-conduction/transport mechanisms in these structures or conduction mechanism may be different region to region depend on N_{ss} in equilibrium of semiconductor, barrier inhomogeneities at M/S interface, series resistance R_s of the structure and native or deposited interfacial layer [28–31]. As can be seen in Fig. 5, the relation between current and voltage for both diode types show a power-law behavior as

Table 2 Extracted barrier height, ideality factor, shunt resistance, and series resistance for the Au/n-Si (MS) and Au/PVP/n-Si (MPS) junctions

Parameters	MS	MPS
I–V measurements		
Φ_B (eV)	0.741	0.841
n	3.13	2.53
R_s (Ω)	115.84	229.59
R_{sh} (Ω)	3.7×10^6	1.8×10^8
Cheung's method		
(dV/d(lnI)-I)		
R_s (Ω)	79.27	272.36
n	3.376	6.172
H(I)-I		
R_s (Ω)	75.47	359.66
Φ_B (eV)	0.708	0.964
Norde's method		
R_s (Ω)	113	283
Φ_B (eV)	0.734	0.790
C–V characteristic		
R_s (Ω)	380	1102
V_0 (V)	1.421	1.155
N_D (cm^{-3})	2.63×10^{14}	5.70×10^{14}
c_2	0.306	0.661
E_F (eV)	0.289	0.270
Φ_B (eV)	0.748	1.059

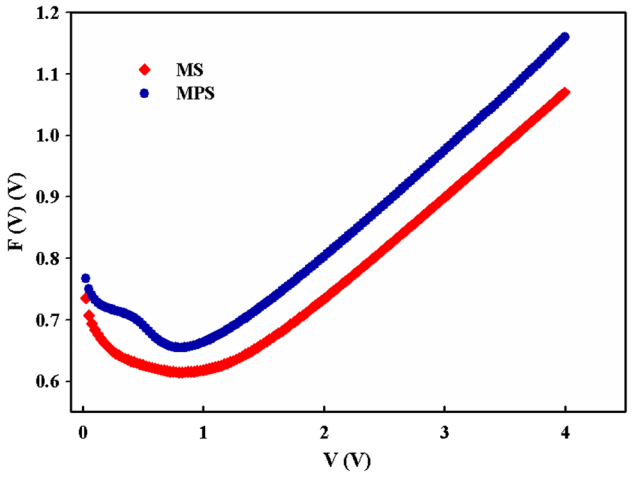

Fig. 4 F(V) vs V graph for the non-interlayered and polymer interlayered structures

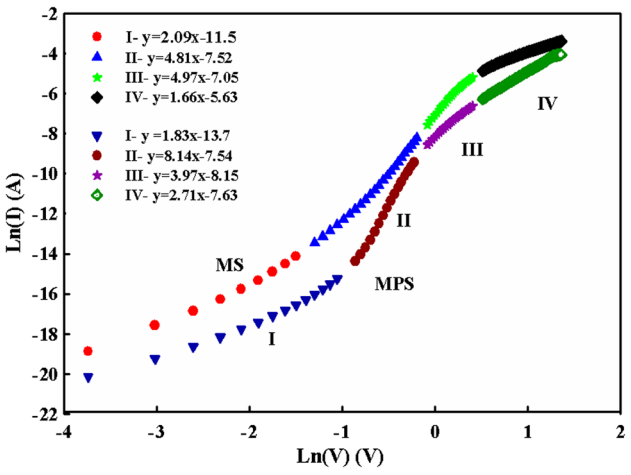

Fig. 5 The forward bias double-logarithmic I_F–V plots of the Au/n-Si (MS) and Au/(PVP)/n-Si (MPS)

$I \sim V^m$ where m can be expressed as the slope of plots for each region.

The slope of these Ln(I) vs Lon (V) plot for the region I and IV, were found as 2.09 and 1.66 for MS and 1.83and 2.71 for MPS structure, respectively. In these regions, the dominant current mechanism are trapped-charge limited current (TCLC) rather than ohmic behavior which indicated that the slope or power-law larger than two. As to TCLC, an increment at injected electrons numbers causes interface traps filling and so increase of the space charges [32] On the other hand, at regions II and III, the dominant current mechanism is space-charge limited current (SCLC). From the electrode to the films using SCLC rised with the increasing applied voltage. Because, the increasing the injected electrons ended up with filling the traps and results the space charge [5, 32].

It is well known that a polymer or semiconductor include between rectifier and ohmic contacts at electronic devices. In these devices interface states or traps (N_{ss}) are also existed where charges can be stored and released. The appropriate forward applied bias voltage applied, as well as they are more effective on the electrical characteristics of these devices [27–29]. The sources of these states/traps is the result any structural defects, donor and receptor atoms, poor molecular connection and impurities. Different types of ways in the literature to uncover N_{ss} such as the forward bias I–V method [27, 28], the receiving spectroscopy method as well as the low/high frequency potency instructions [22]. However, both MS and MPS constructions, as shown in Fig. 1, deviations in the deflection regions, indicating the continuity of the Nss, which is balanced with n-Si and plays an important role in the currents-carrying/transport mechanisms. In current work, the profile of the N_{SS} is energy-dependent manner, our first approach, was obtained based on biases at I–V data by taking into account n and BH depend on voltage. Amounts of n (V) and ($\Phi_e = \Phi_B$ (V)) are depicted by Eqs. (10) and (11), respectively [29].

$$n(V) = (q/kT)\left[V/\ln\left(I/I_0\right)\right] \tag{10}$$

$$\Phi_e = \Phi_{B0} + \alpha V = \Phi_{B0} + \left(1 - \frac{1}{n(V)}\right)\mathrm{V} \tag{11}$$

Here; α ($= d\Phi_e/dV = 1–1/n(V)$) is the voltage coefficient of the BH. According to Card and Rhoderick [29] the ideality factor of a diode which is represented as *n* occur greater than one.

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{SS}(V)\right] \tag{12}$$

In Eq. (12), W_D is the depletion layer width extracted from the reverse biases C^{-2} vs V plot, ε_s and ε_i are the semiconductors' and interlayers' permittivity, and δ is the interlayer thickness, respectively. The ε_s, ε_i and ε_o values are 11.8 ε_o for Si, 4ε_o for (PVP) and ε_o is the vacuum permittivity with the value of 8.85×10^{-12} F/m, respectively. The intermediate layer thickness was specified from the measured C–V characteristics at sufficiently high frequency (100 kHz) at the strong accumulation region using the interlayer capacitance ($C_i = \varepsilon\ \varepsilon_i\ A/\delta$). Thus, the thickness of SiO_2 and PVP was found from this equation as 2.8 nm and 50 nm, respectively. For n-type semiconductors, the energy of interface states which is represented as E_{ss} with respect to the bottom of conduction band edge which is represented as Ec, at the semiconductor surface is given in equation below [27–29].

$$E_e - E_{SS} = q\left[\Phi_e - \left(V - IR_S\right)\right] \tag{13}$$

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_S}{W_D}\right] \tag{14}$$

The N_{ss} vs ($E_c - E_{ss}$) plot for the the Au/n-Si and Au/(PVP)/n-Si structures were shown in Fig. 6. Here, the N_{ss} value rises substantially in the forbidden band's mid-gap of the Si from the conduction band's bottom for these two type SBDs. Clearly, the N_{SS} values for the polymer interlayered structure are remarkably less than the non-interlayered structure in the whole energy range due to the saturation of dangling bond by the PVP interlayer.

3.2 The forward and reverse bias capacitance/conductance–voltage characteristics

To acquire other electrical parameters of each structure such as diffusion potential (V_D), doping concentration of donor atoms (N_D), Fermi energy level (E_F), barrier height (Φ_B(C–V)), and R_s, both the C–V and G/ω–V measurements were performed at 100 kHz which is enough high to determined main electrical parameters to reduce the effects of surface charges, dislocates

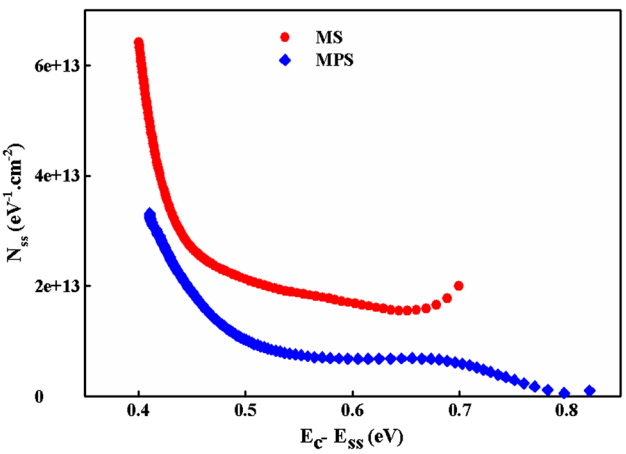

Fig. 6 The energy density distribution profile of the N_{ss} for Au/n-Si (MS) and Au/(PVP)/n-Si (MPS)

and other impurities and given in Figs. 7 and 8, respectively. As presented Figs. 7 and 8, both the C–V and G/ω–V plots which are exhibit three distinct regions as inversion, depletion and accumulation like an interlayered MS type structure as MIS, MFS or MPS, but they have a concave curvature in the accumulation region due to the existence of R_s and interfacial polymer layer. The applied bias voltage will be shared between the depletion layer capacitance, R_s, and interfacial layer. The effect of R_s in depletion and accumulation regions can be ignored low, but in these regions N_{ss} become effective on the C–V and G/ω–V characteristics. It is expected that both C and G/ω values are not dependent on frequency, but this state is substantially dissimilar in the applications due to the N_{ss}, R_s, and interlayer presence [3–10].

The value of Rs is more effective both on the I–V, C–V and G/ω–V data at forward bias region and so it must be taken into account in the calculation of the main electrical parameters of the MS, MIS and MPS type structures especially at high frequencies and enough high forward biases [33]. The resistance (R_i) of these structures are also dependent of bias voltage due to inhomogeneity of interfacial layer and BH at M/S interface, and a particular density distribution of N_{ss} at junction and in the bandgap of semiconductor [22, 23, 28, 29, 33]. Therefore, R_i for both the non-interlayered and interlayered MS structures were acquired from the C–V and G/ω–V data at 100 kHz by using Nicollian-Brews method [22] and compared with the values acquired from Ohm's Law. It is believed that the Nicollian-Brews method for the enough high frequencies ($f \geq 100$ kHz) to eliminate the effects of N_{ss}. In Fig. 9, the real values of R_s was acquired from the acquired C_m and G_m/ω values at strong accumulation region with aid of the following relation [22].

$$R_S = \frac{G_m}{G_m^2 + \left(\omega C_m\right)^2} \tag{15}$$

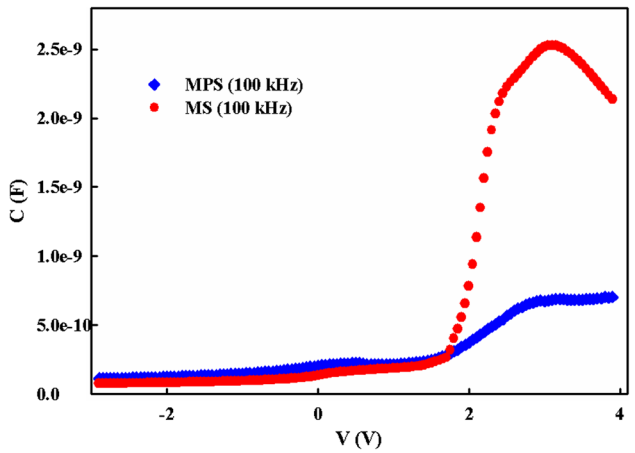

Fig. 7 C–V graph of each structure at reverse and forward biases

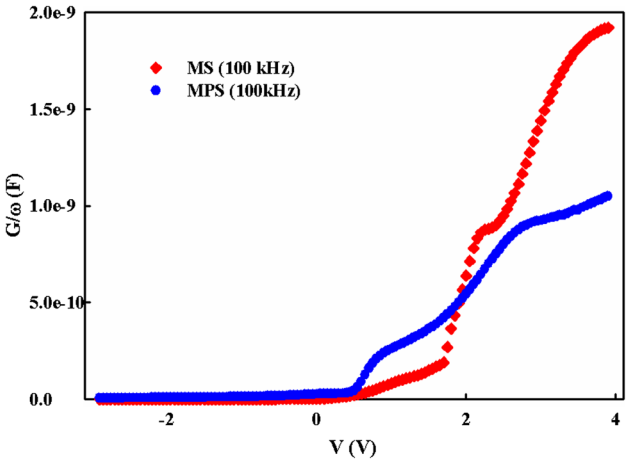

Fig. 8 The G/ω–V graph of each structure at reverse and forward biases

Thus, voltage dependent profile of R_i was extracted from the measured of C and G data for any biases for the two type structures (Fig. 9). The values of R_s for the non-interlayered and interlayered structure were calculated as and 380, 1102 Ω at 4 V respectively. Evidently, the R_s value can be changed from any voltage to other. The observed discrepancy in R_s for two type structures obtained Ohm Law, Norde, Cheung and Nicollian-Brews methods can be interpreted by the measuring method's nature which is corresponding to various range of bias voltage.

Figure 10 shows the reverse bias C^{-2}–V plots for the MS and MPS structure at 100 kHz at room temperature which has a straight line with different slopes over a large reversed bias interval. In the Schotky type structures or Schottky barrier diodes (SBDs), the variation of the depletion layer's capacitance with applied reverse biases (V_R) is given by [28].

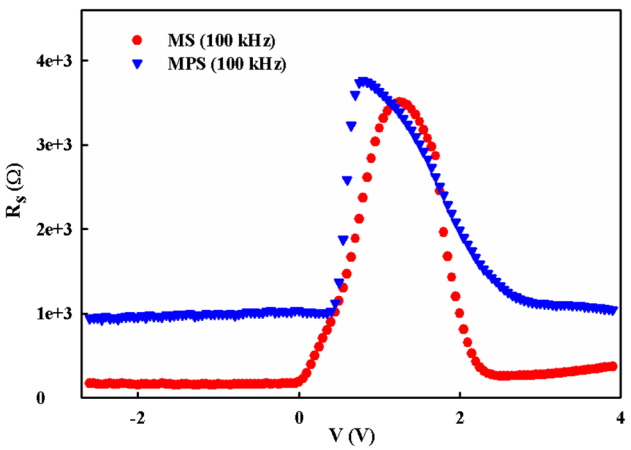

Fig. 9 The structure resistance (R_s)–V graph of the non-interlayered and polymer interlayered structures

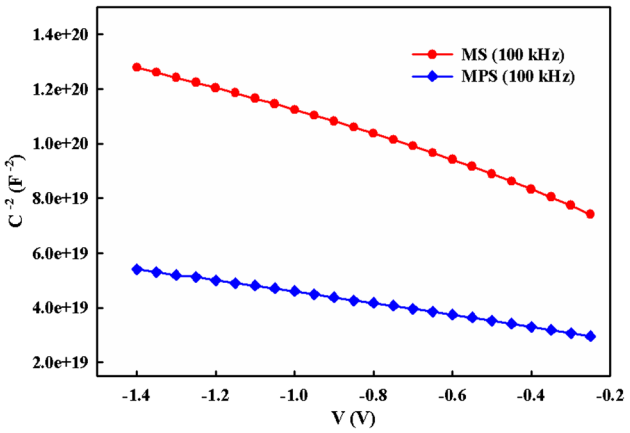

Fig. 10 C^{-2}–V graph of the non-interlayered and interlayered MS structures for 100 kHz

$$C^{-2} = \frac{2(V_R + V_0)}{q\varepsilon_S N_D A^2} \tag{16}$$

Where, V_0 is the intercept of C^{-2}vs V plot at zero biases, and A is the structure's rectifier contact area. The V_0 and N_D values were obtained from the slopes and intercepts of the linear section of C^{-2}–V plots for two type structures and then the E_F value was acquired by the aid of the following relations [28]:

$$E_F = \frac{kT}{q} \ln\left(\frac{N_C}{N_D}\right) \tag{17}$$

With

$$N_C = 4.82 \times 10^{15} T^{3/2} \left(m_e^* / m_0\right)^{3/2} \tag{18}$$

In Eq. (17), N_C is the effective density of states in the Si conductance band (E_c), and is the effective mass of the electron. As can be seen in Fig. 10, the existence of native or deposited an interfacial layer and interface traps between semiconductor and interfacial layer leads to a large intercept of intercept voltage. In this case, the obtained higher value of diffusion potential (V_D) or BH can be modified by using the c_2 (=N_D(exp.)/N_D(theor.)) constant which is the ratio of the obtained experimental value of N_D(exp.) to its theoretical value N_D(theor.) as following form [28].

$$1/n \approx c_2 = \varepsilon_i / (\varepsilon_i + qN_{ss}) \tag{19}$$

Thus, in this study, the value of (C–V) was calculated for the fabricated MS and MPS structure as follow:

$$\Phi_B(C-V) = (c_2 Vo + kT/q) + E_F = V_D + E_F \tag{20}$$

The obtained Vo, N_D, c_2 V_D, E_F, Φ_B(C–V), and Rs values from the C–V and G/ω–V measurements are tabulated Table 2. It is clear that the value of BH in the C–V measurement is larger than the I–V measurements because of the measurement methods which are corresponding different bias voltages and also this is an evident the existence of BH inhomogeneity between metal and semiconductor. The calculated BH from the reverse bias C–V characteristics is influenced from the distribution of electronic charges at depletion region boundary. Thus, such as charges distribution follows the mean value of the BHs. According to Song et al. [34], the discrepancies in the BH determined from the forward bias and reverse bias regions is the results of BH in-homogeneities which is raised from the interfacial layer composition, non-uniformity of the interfacial layer thickness, non-uniformity of the concentration of doping acceptor/donor atoms, and a special distribution of interfacial charges or surface states. Recently, similar results have been reported in the literature [35–37].

4 Conclusions

In this study, we investigated the electrical properties obtained from the forward and reverse bias I–V and C/G–V properties of the (PVP) intermediate layer. For this purpose, both non-interlayered and interlayered MS structures were produced on the identical n-Si wafer and all the electrical properties were compared. I–V features a good rectifier behavior for two types of sample, but the RR ratio of the non-interlayered structure was found to be 55 times less than the polymer interlayered structure. In addition, the MS type structure inverse saturation current (I_0) was 54 times higher than the polymer interlayered structure. The values of R_s, n and Φ_{B0} were obtained from TE and Cheung methods as 272.4Ω, 6.17, and 0.964 eV for MPS and 79.2 Ω, 3.38, and 0.708 eV for MS structure. The density distribution of N_{ss} as energy function ($E_c - E_{ss}$) was found by taking into account the voltage-dependent n and BH values for two different structures by utilizing the I–V forward biased characteristics and they changed from 1.074×10^{12} $eV^{-1}cm^{-2}$ (at $E_c - 0.821$ eV) to 3.55×10^{13} $eV^{-1}cm^{-2}$ (at $E_c - 0.409$ eV) for MPS and 3.85×10^{13} $eV^{-1}cm^{-2}$ (at $E_c - 0.724$ eV) to 5.67×10^{13} $eV^{-1}cm^{-2}$ (at $E_c - 0.405$ eV) for MS structure. To see the effects of the measurement method, some important electrical parameters such as E_F and Φ_{C-V} were obtained from the reverse bais C^{-2}–V characteristics at 100 kHz. These results showed that the BH value obtained from C^{-2}–Vplot was greater than the value found in the forward bias Ln (I) vs V plot for each structure. The difference in BH value acquired from C–V and I–V measurements is caused by many reasons. Some of these, the nature of the measurement methods, the distribution of electronic charge at depletion region boundary, non-uniformity of the interfacial layer thickness, the concentration of doping atoms, the interfacial

layer composition, a special density distribution of N_{ss} or surface states at junction and interlayer in-homogeneities.

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