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Electrical properties of Au–Cu/ZnO/p-Si diode fabricated by atomic layer deposition

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Abstract

The electrical properties of the Au–Cu/ZnO/p-Si diode were investigated with the temperature dependent current–voltage measurements in a wide temperature range from 220 to 360 K with 20 K steps and also frequency dependent capacitance–voltage and conductance–voltage measurements using admittance spectroscopy by changing frequency from 1 to 1000 kHz. The ZnO thin film layer was deposited by atomic layer deposition technique (ALD) to obtain homogenous interface layer and this layer surface was characterized with AFM analyses. Assuming thermionic emission (TE) model, diode parameters such as barrier height and ideality factor were determined for the Au–Cu/ZnO/p-Si diodes and the strong temperature dependence of these values were modeled by TE model with modified by Gaussian distribution of the barrier height. Therefore, the observed non-ideal current behavior was discussed on the basis of barrier inhomogeneity and the presence of native oxide interfacial layer in the diode. The mean barrier height was found as 1.38 eV with 0.18 standard deviation, and the Richardson constant modified by this model was obtained as 28 A/cm^2k^2 close to the theoretical value. Additionally, the distribution profile of the interface states and series resistance value were evaluated by the capacitance and conductance characteristics. It could be seen from the results that both of them strongly depends on the device frequency. As a result of these works, fabricated Au–Cu/ZnO/p-Si diodes may be used for next technological application in wide range temperature in industry.

1 Introduction

In recent years, transparent conductive oxides (TCOs) with various metals and different doping metals have gained attentions among electronic applications mainly in use of photovoltaics, light emitting diodes, and transparent transistors [1–3]. These oxide structures generally include one or two metallic element and therefore fabricated as a binary or ternary compound, respectively. The novel TCO film layers are expected to be in low resistivity values as about 10^{-5} Ω cm [3] with optical band gap higher than 3 eV and low absorption characteristics in the visible region [2–4]. Among the common TCO film layers, ZnO have become a promising alternative in the case of cost effectiveness and environmental friendliness [5]. It is an ionic wide band gap semiconductor in the family II–VI oxides [6]. Having a direct band gap of about 3.4 eV with a high transparency at visible light, large exciton binding energy of 60 meV at room temperature, and high mobility of conducting electrons over 50 cm^2/Vs provides to be one of the materials dominating TCO technology [5–10]. As a result, ZnO layer is one of the most popular metal oxide layer for electronic devices because of its remarkable electrical and optical properties [11–13]. Due to these properties, ZnO have triggered wide attention to use in various diode applications. In the literature works, the main interest was concentrated on metal/ZnO/semiconductor devices and some of researchers investigated temperature-dependent current–voltage plots of metal/ZnO such as Au/ZnO and Pd/ZnO in which the conduction mechanism for these devices with ZnO can be inserted as a metal oxide layer between the metal and semiconductor device [12–14]. In addition, Kocyigit et al. [15], reported temperature-dependent capacitance–voltage plots of Au/ZnO/n-Si devices. In the literature, ZnO is one of the most studied materials for improving metal–oxide–semiconductor (MIS) diode behaviors. Therefore, it has been widely used by depositing different thin film deposition techniques such as sputtering [16], atomic layer deposition (ALD) [15, 17] and sol–gel spin coating [18]. Among them, ALD technique offers distinct advantages since thin ZnO layer can be easily deposited in homogeneity, large area stability, uniformity

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and good thickness control [19]. Additionally, of these advantages, under low temperature synthesis of materials is low cost than fabrication at high temperature [20]. In this work, ZnO layer was deposited using ALD technique due to its mentioned advantages and the electronic properties of Au–Cu/ZnO/p-Si diodes were investigated using current–voltage (I–V), capacitance–voltage (C–V) and conductance–voltage ($G/\omega - V$) characteristics. Transport properties of Au–Cu/ZnO/p-Si diode were analyzed by TE model modified by Gaussian distribution of the barrier height. Additionally, the distribution profile of the interface states and series resistance value were evaluated by the capacitance and conductance plots. The electrical parameters of Au–Cu/ZnO/p-Si diode were extracted as a result of current–voltage (I–V), capacitance–voltage (C–V) and conductance–voltage ($G/\omega - V$) characterization steps.

2 Experimental details

Diode structure was fabricated by depositing ZnO film layer on p-Si substrate with Au top and Al back metal contacts. Before the film deposition step, p-Si wafer substrates were coated with Al metal by thermal evaporation technique and subsequent heat treatment at 450 °C was applied to form an ohmic contact on the back side of the substrate. With high control in atomic composition and also in thickness at the Angstrom level, 5 nm ZnO thin film layer was deposited on (111) oriented p-Si wafer by using by high-vacuum atomic layer deposition (ALD) Savannah S300 system in Bilkent/UNAM facility. It is well known the morphology of thin interfacial layer (ZnO) and its homogeneity are very important for the device performance of Au–Cu/ZnO/p-Si devices [11–14, 21, 22]. Therefore, in order to investigate the morphology of ZnO, the AFM was used for 1 µm × 1 µm wide area scanning and the image is given in Fig. 1a. The AFM topography images of the ZnO films are with rms roughness, σ, of 0.351 nm for ZnO. It is clear that the ZnO thin film has a smooth and uniform surface. It can be said that ALD technique is very effective for smooth ZnO thin film layer. In addition, Au top metal contact was deposited using evaporation on the surface of the ZnO film layer through 2 mm diameter dot-shaped mask. In order to trigger adhesion on the film surface, about 5 nm Cu metal was deposited using electron beam evaporation system prior to the Au evaporation. The energy level and schematic diagram of Au–Cu/ZnO/p-Si diode are presented in Fig. 1b, c, respectively [23–28]. The obtained Schottky diode was characterized by I–V measurements in the temperature range of 220–360 K by using a Keithley 2401 sourcemeter. Additionally, C–V and $G/\omega - V$ measurements were performed by using Hewlett Packard 4192A LF model impedance analyzer in the frequency interval between 1 kHz and 10 MHz at room temperature.

3 Results and discussion

Figure 2 shows the temperature dependent I–V characteristics of the Au–Cu/ZnO/p-Si diode diode in the temperature interval of 220–360 K. It was observed that, the fabricated diode structure is in a typical rectifying behavior and the

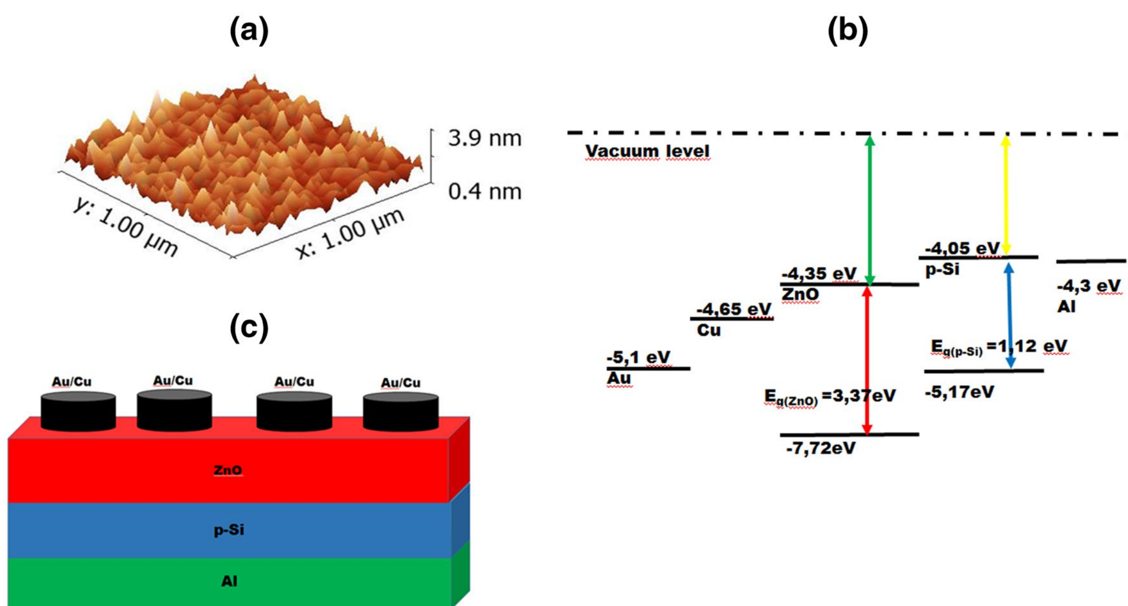

Fig. 1 **a** AFM image of the ZnO thin film, **b** the energy level of Au–Cu/ZnO/p-Si diode, **c** the schematic diagram of Au–Cu/ZnO/p-Si diode

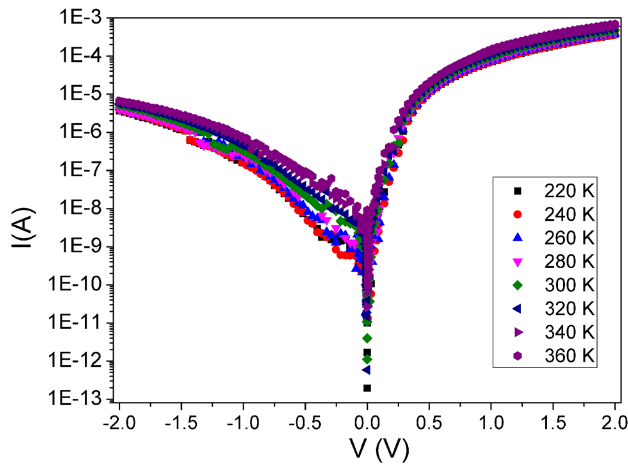

Fig. 2 Semi-logarithmic forward and reverse bias I–V characteristics of Au–Cu/ZnO/p-Si diode

Table 1 Calculated diode parameters using TE theory for Au–Cu/ZnO/p-Si diode

Temperature (T in K)	Barrier height (Φ_{B0} in eV)	Ideality factor (n)
360	0.89	1.83
340	0.86	1.95
320	0.82	2.01
300	0.76	2.10
280	0.73	2.18
260	0.68	2.26
240	0.65	2.32
220	0.56	2.49

linear current characteristics at low bias region were modeled by the standard thermionic emission (TE) model as [29, 30];

$$I = I_0\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \quad (1)$$

where I_0 is the reverse saturation current at zero-bias derived from the straight line intercept of the semi-logarithmic plot given in Fig. 2 with the following relation,

$$I_0 = AA^*T^2 \exp\left(\frac{-q\Phi_{B0}}{kT}\right) \quad (2)$$

where A is the effective diode area, A^* is the effective Richardson constant and Φ_{B0} is the zero-bias barrier height. In Eq. 1, the other parameters, q, k, T and n are the electronic charge, the Boltzmann constant, the applied temperature and ideality factor. According to the TE model given in Eq. 1, the assumption on the current conduction mechanism is based on the dimensionless parameter, n and it can be determined from the slope of the linear region of the forward bias region given in Fig. 2 as,

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln(I)}\right) \quad (3)$$

In this proposed model, in addition to the voltage drop due to the series resistance (R_s), the presence of an interface layer could be effective in the current flow through the diode [5, 31–34]. According to the TE model, diode parameters as Φ_{B0} and n were calculated from the Eqs. 2, 3, respectively and the experimental values were tabulated in Table 1. These values were found in temperature dependent characteristics in which Φ_{B0} increases whereas n decreases with increase in T. Although the ideal diode is expected to have n in unity for the pure TE mechanism, the values obtained between 1 and 2 can also be accepted as the indication of TE in the diode structure [29]. On the other hand together with the strong temperature dependence in Φ_{B0} and n, this deviation in n can be due to the presence of an interfacial thin oxide layer at Au–Cu and ZnO interface, a wide distribution of low-Schottky barrier height and effect of R_s [5].

Using these values, the homogeneity of the obtained barrier was investigated from the plot of Φ_{B0} versus n (Fig. 3) and the observed linear relation was analyzed by linear fitting process. As a result of the linear fit equation, the homogeneous barrier height for this diode was determined as 1.33 eV [34, 35].

Moreover, the observed variations in the Φ_{B0} and n, was resulted as non-linear behavior of the Richardson plot derived from Eq. 2 and this deviation together with non-ideal characteristics of these values can be evaluated as a non-ideal I–V behavior in the diode on the basis of a model including barrier in homogeneties [5, 34]. According to model proposed a

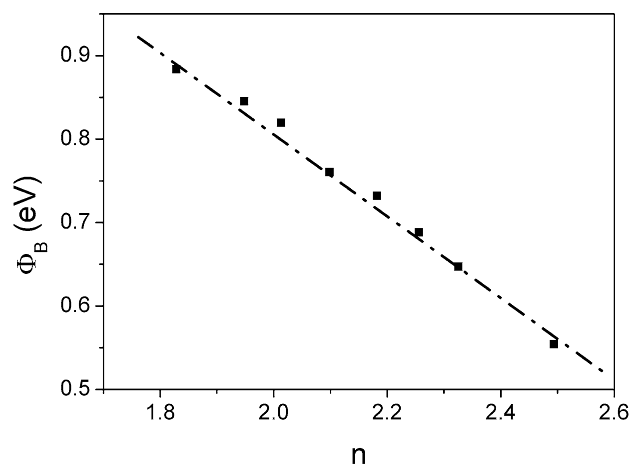

Fig. 3 Φ_{B0} vs. n plot for Au–Cu/ZnO/p-Si diode

Gaussian distribution (GD) in the barrier, the I–V relation can be modified as,

$$I = AA^*T^2 \exp\left[\left(-\frac{qV}{kT}\right)\left(\bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT}\right)\right] \exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \quad (4)$$

with modified reverse saturation current expression as,

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{ap}}{kT}\right) \quad (5)$$

where Φ_{ap} and n_{ap} are the apparent barrier height and apparent ideality factor, respectively. In this model, barrier inhomogeneity in the diode is expressed by a Gaussian function with a mean barrier height $\bar{\Phi}_{B0}$ and standard deviation, σ_0. Therefore, based on the inhomogeneities in the barrier height formation in the diode, Φ_{ap} can be expressed as;

$$\Phi_{ap} = \bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT} \quad (6)$$

In this case, the Gaussian parameters, $\bar{\Phi}_{B0}$ and σ_0 were calculated from the plot Φ_{B0} versus $q/2kT$ using Eq. 6. As shown in Fig. 4, a straight line was observed in the relation of these experimental data, and by applying the linear fitting, $\bar{\Phi}_{B0}$ and σ_0 were found as 1.38 and 0.18 in the intercept on the ordinate axis and slope, respectively. Since deviation from the mean value is in the percentage of about 13%, it can be the indication of the validity of GD model with the existence of the interface inhomogeneity [34, 36]. In addition, according to the GD model, these parameters are assumed to be bias dependent and these voltage coefficients can be found from the relation between $(n^{-1} - 1)$ and $q/2kT$ as [32, 36–39],

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \quad (7)$$

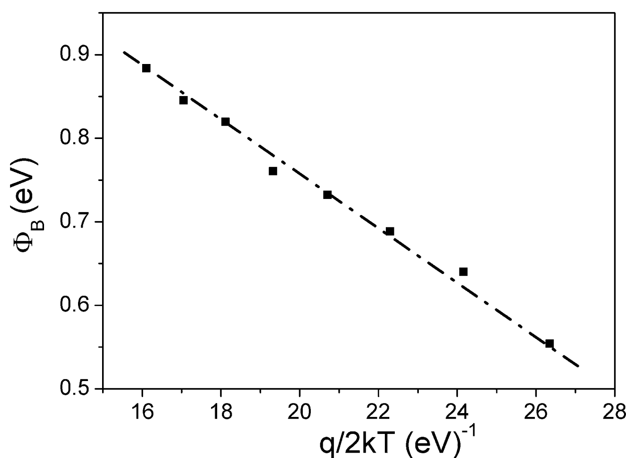

Fig. 4 Φ_{B0} vs $q/2$kT plot for Au–Cu/ZnO/p-Si diode

Thus, from the slope and intercept of the fitting process in the plot given in Fig. 5, ρ_2 and ρ_3 were extracted as about 0.013 and −0.2625 as a linear bias dependence of $\bar{\Phi}_{B0}$ and σ_0, respectively. These parameters are used as the identification of the voltage deformation of the barrier height distribution. In fact, Eq. 7 predicts the temperature effect on n and it is used as a measure for the homogenization of the barrier distribution.

In Fig. 6, the modified Richardson plot was investigated using the following modified relation,

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\bar{\Phi}_{B0}}{kT} \quad (8)$$

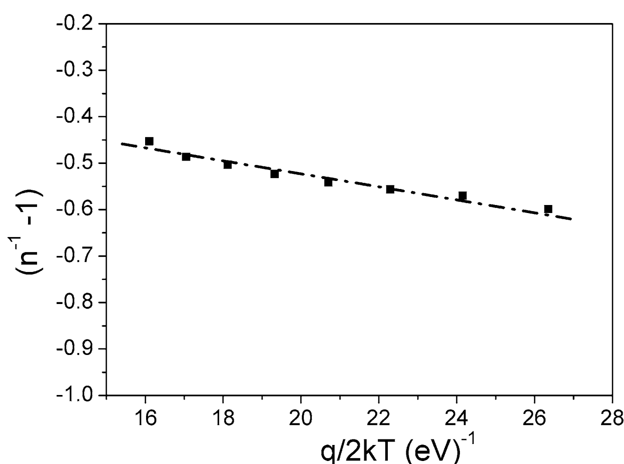

Fig. 5 $(n^{-1} - 1)$ vs q/2kT plot for Au–Cu/ZnO/p-Si diode

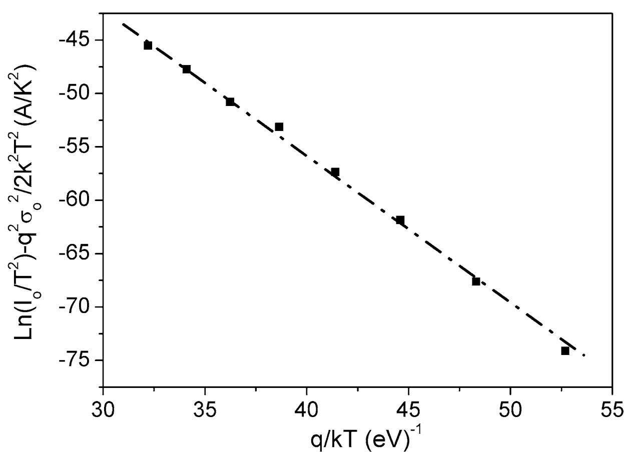

Fig. 6 Modified Richardson $\ln(I_0/T^2) - \left(q^2\sigma_0^2\right)/(2k^2T^2)$ vs q/kT plot for Au–Cu/ZnO/p-Si diode

and the intercept of the observed linear relation was used to determine Richardson constant [39, 40]. The experimental value was calculated as 28 A/cm^{2}k^2 for a given diode area and it is found in a good agreement with the theoretical value as expected to be 32 A/cm^{2}k^2 for ZnO semiconducting layer [6].

In a detailed interpretation of the electrical characteristics of the diode structure, the capacitance–voltage (C–V) and conductance–voltage ($G/\omega - V$) profiles were analyzed as a function of applied frequency as shown in Fig. 7.

Figure 7 presents the decreasing trend in the capacitance and conductance values with increase in frequency and the frequency dependence is low at reverse bias region whereas the high variation was obtained with increasing bias voltage. In the case of low frequency values, the additive capacitance values are expected from the effects of the interface states, however at sufficiently high frequency values, they do not contribute to the capacitance [15, 41–43]. Therefore, distribution of the density of interface states (D_{it}) were investigated by using high-frequency ($C_{HF} - C_{LF}$) [40, 41] and Hill-Coleman methods [43]. Under high frequency values, the interface state capacitance (C_{it}) can be described as,

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_i}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_i}\right]^{-1} \tag{9}$$

where C_{HF} and C_{LF} are the measured highest and lowest capacitance values, and C_i is the capacitance of the

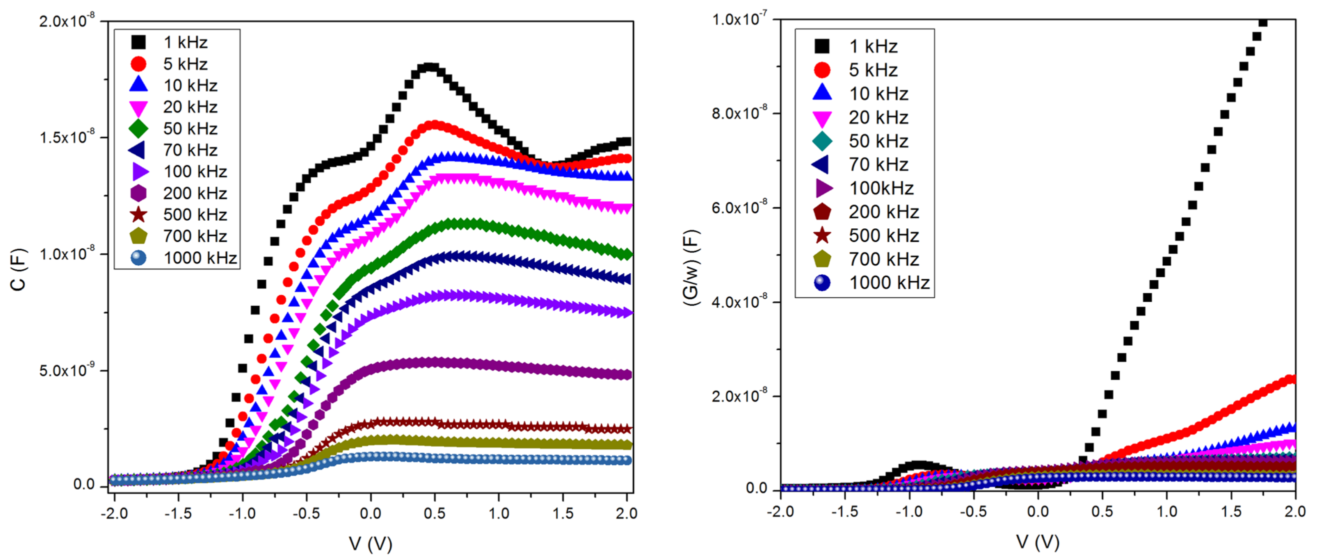

Fig. 7 Capacitance (C) and conductance (G/ω) versus bias voltage plots for Au–Cu/ZnO/p-Si diode at room temperature

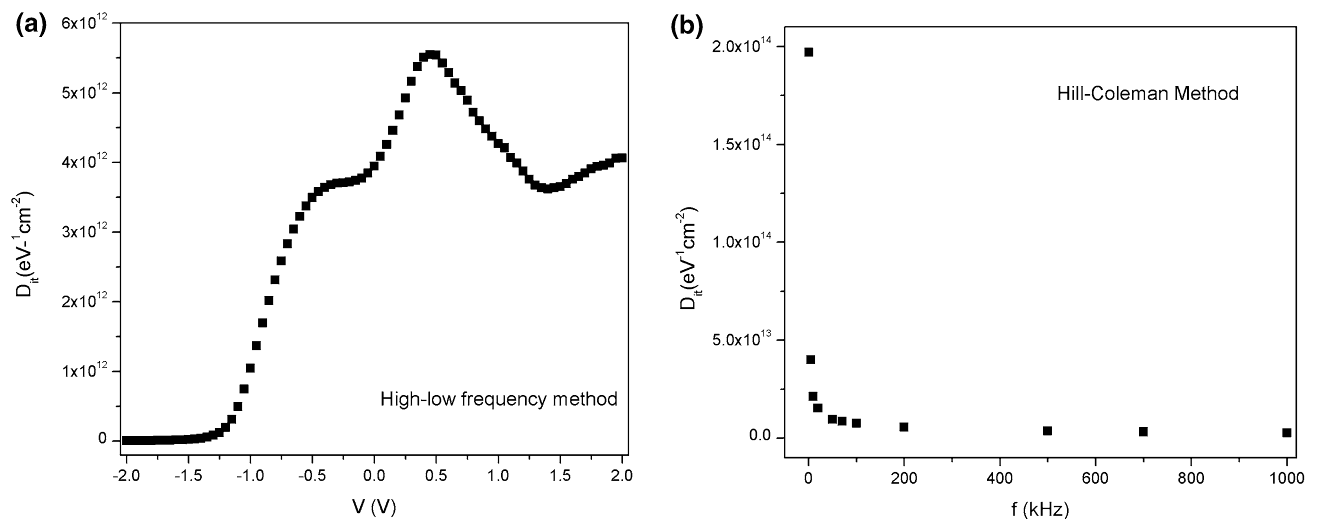

Fig. 8 Density of interface states, D_{it} characteristics in Au–Cu/ZnO/p-Si diode in terms of **a** ($C_{HF} - C_{LF}$) and **b** Hill-Coleman methods

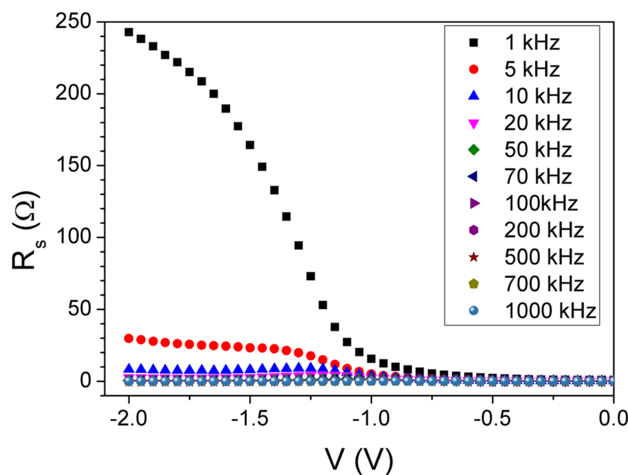

Fig. 9 Frequency dependent R_s values under reserve bias

interfacial layer [40, 41]. According to the $C_{HF} - C_{LF}$ model, the voltage dependent D_{it} profile was given in Fig. 8a and it was observed that there is a peak around 0.6 V. This peak could be related with the contribution of the interface states to the capacitance characteristics of the diode [44]. In addition, Hill-Coleman method was used to investigate the frequency dependent profile expressed as,

$$C_{it} = \frac{(G_m/\omega)_{\max}}{\left[(G_m/\omega)_{\max}/C_i\right]^2 + \left(1 - C_m/C_i\right)^2} \tag{10}$$

where C_m and G_m are the measured capacitance and conductance values, respectively [45]. As presented in Fig. 8b, D_{it} values were found in decreasing behavior with the increasing frequency, and this trend observed also observed at higher frequencies. In addition, the calculated D_{it} values using two different methods show approximately the same order in the magnitude.

From the results in C–V and $G/\omega - V$ measurements, the R_s profile was evaluated in the strong accumulation region at high frequency values as [29],

$$R_s = \frac{G_m}{(G_m)^2 + (\omega C_m)^2} \tag{11}$$

and the calculated values were shown in Fig. 9 for various frequencies. In this application of the admittance-based method, R_s values were found in decreasing characteristics with increasing the applied frequency that could be due to the distribution of D_{it} in the diode structure [41].

4 Conclusion

The electrical properties of the Au–Cu/ZnO Schottly barrier diode fabricated on the p-Si substrate were analyzed in terms of the forward I–V characteristics in the temperature range of 220–360 K. As a result of the experimental results, the values of Φ_{B0} and n were extracted according to the initial assumption on TE model. Depending on the temperature response of these values, pre-dominant conduction mechanism was explained by a Gaussian function to model the inhomogeneous barrier height formation in the diode. On the basis of TE with GD of barrier, the Gaussian parameters $\bar{\Phi}_{B0}$ and σ_0 were obtained as 1.38 and 0.18 respectively. Since in the analysis of diode parameters, Richardson constant was used as in the same value from the literature and the dominant transport mechanism was modeled by different mechanism than thermionic emission model, under the effect of Gaussian approximation this constant was modified and it was found as about 28 A/cm^2k^2 in a good agreement with the literature works. C–V and $G/\omega - V$ measurements were carried out to investigate the possible interface state effects, and the voltage and frequency dependent D_{it} profiles were expressed by using $C_{HF} - C_{LF}$ and Hill-Coleman methods. As a result of these analyses, decreasing behavior of R_s values with increasing frequency was discussed.

References

1. D.S. Ginley, C. Bright, MRS Bull. **25**, 15–18 (2000)
2. K.L. Chopra, S. Major, D.K. Pandya, Thin Solid Films **102**, 1–46 (1983)
3. A. Stadler, Materials **5**, 661–683 (2012)
4. T. Minami, Semicond. Sci. Technol. **20**, S35–S44 (2005)
5. S. Aydogan, K. Cinar, H. Asil, C. Coskun, A. Turut, J. Alloy. Compd. **476**, 913–918 (2009)
6. J. Dhananjay, Nagaraju, S.B. Krupanidhi, Physica B **391**, 344–349 (2007)
7. L. Rajan, C. Periasamy, V. Sahula, Perspect. Sci. **8**, 66–68 (2016)
8. M. Purica, E. Budianu, E. Rusu, Thin Solid Films **383**, 284–286 (2001)
9. S. Alkis, B. Tekcan, A. Nayfeh, A.K. Okyay, J. Physiother. Occup. Ther. **15**, 105001 (2013)
10. A. Alaya, K. Djessas, L. El Mir, K. Khirouni, J. Electron. Mater. **45**, 4859–4864 (2016)
11. F. Yakuphanoglu, S. Ilican, M. Caglar, Superlattices Microstruct. **47**, 732–743 (2010)
12. B.A. Gozeh, A. Karabulut, A. Yildiz, F. Yakuphanoglu, J. Alloy. Compd. **732**, 16–24 (2018)
13. N.H. Al-Hardan, A. Jalar, M.A. Abdul Hamid, L.K. Keng, N.M. Ahmed, R. Shamsudin, Sens. Actuators A Phys. **207**, 61–66 (2014)
14. A. Kocyigit, I. Orak, Z. Caldıran, A. Turut, J. Mater. Sci. **28**, 17177–17184 (2017)
15. A. Kocyigit, I. Orak, S. Aydoğan, Z. Caldıran, A. Turut, J. Mater. Sci. **28**, 5880–5886 (2017)

16. S.K. Singh, P. Hazra, S. Tripathi, P. Chakrabarti, Superlattices Microstruct. **91**, 62–69 (2016)
17. İ Orak, Solid State Commun. **247**, 17–22 (2016)
18. F. Yakuphanoglu, Y. Caglar, M. Caglar, S. Ilican, Mater. Sci. Semicond. Process. **13**, 137–140 (2010)
19. A. Turut, A. Karabulut, K. Ejderha, N. Bıyık, Mater. Sci. Semicond. Process. **39**, 400–407 (2015)
20. A. Karabulut, I. Orak, A. Turut, Solid State Electron. **144**, 39–48 (2018)
21. I. Orak, A. Kocyigit, A. Turut, J. Alloy. Compd. **732**, 873–879 (2017)
22. H.H. Gullu, M. Parlak, Mod. Phys. Lett. B **31**, 1750043 (2017)
23. R.L. Anderson, Solid State Ceram. **5**, 341–351 (1962)
24. J.-I. Chyi, D. Mui, J. Chen, H. Morkoc, Solid State Ceram. **34**, 747–750 (1991)
25. J.M. Nel, F.D. Auret, L. Wu, M.J. Legodi, W.E. Meyer, M. Hayes, Sen. Actuators B **100**, 270–276 (2004)
26. M.L. Grilli, S. Aydogan, M. Yilmaz, Superlattices Microstruct. **100**, 924–933 (2016)
27. B. Parida, S. Kim, M. Oh, S. Jung, M. Baek, J.H. Ryou, H. Kim, Mater. Sci. Semicond. Proc. **71**, 29–34 (2017)
28. K. Lui, M. Sakurai, M. Aono, Sensors **10**, 8604–8634 (2010)
29. S.M. Sze, K.N. Kwok, *Physics of Semiconductor Devices* (Wiley, USA, 2010)
30. E.H. Rhoderick, R.H. Williams, *Metal-semiconductor Contacts* (Clarendon, Oxford, 1988)
31. S. Altindal, S. Karadeniz, N. Tugluoglu, A. Tataroglu, Solid-State Electron. **47**, 1847–1854 (2003)
32. H.H. Gullu, O. Bayrakli, D.E. Yildiz, M. Parlak, J. Mater. Sci. Mater. Electron. **28**, 17806–17815 (2017)
33. H.H. Gullu, M. Parlak, J. Mater. Sci. **29**, 11258–11264 (2018)
34. F.Z. Pur, A. Tataroglu, Phys. Scr. **86**, 035802 (2012)
35. R.T. Tung, Appl. Phys. Lett. **58**, 2821–2823 (1991)
36. D.E. Yıldız, S. Altindal, H. Kanbur, J. Appl. Phys. **103**, 124502 (2008)
37. M. Ozer, D.E. Yildiz, S. Altindal, M.M. Bulbul, Solid State Electron. **51**, 941–949 (2007)
38. H. Ozerli, I. Karteri, S. Karatas, S. Altindal, Mater. Res. Bull. **53**, 211–217 (2014)
39. S. Karatas, M. Cakar, A. Turut, Mater. Sci. Process. **28**, 135–143 (2014)
40. W. Mtangi, F.D. Auret, C. Nyamhere, P.J. van Rensburg, M. Diale, A. Chawanda, Physica B **404**, 1092–1096 (2009)
41. A. Tataroglu, S. Altindal, Microelectron. Eng. **85**, 2256–2260 (2008)
42. R. Castagne, A. Vapaille, Surf. Sci. **28**, 175–193 (1971)
43. W.A. Hill, C.C. Coleman, Solid State Electron. **23**, 987–993 (1980)
44. M. Terlemezoglu, O. Bayrakli, H.H. Gullu, T. Colakoglu, D.E. Yildiz, M. Parlak, J. Mater. Sci. **29**, 5264–5274 (2018)
45. J.H. Werner, H.H. Guttler, J. Appl. Phys. **69**, 1552 (1991)