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Forward and reverse bias current–voltage (I–V) characteristics in the metal–ferroelectric–semiconductor (Au/$SrTiO_3$/n-Si) structures at room temperature

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Abstract
The main electrical parameters of fabricated Au/$SrTiO_3$/n-Si (MFS) structures have been investigated by using various methods. The values of ideality factor (n) and zero-bias barrier height (Φ_{B0}) are calculated from the forward bias current–voltage (I_F–V_F) data as 0.60, and 0.48 eV from thermionic theory (TE) and Cheung functions, respectively. The value of R_s is also obtained from the Norde function and Cheung functions as 87.83 and 137.57 Ω, respectively. The discrepancy between these results can be attributed to the calculated method and the measured voltage range. Besides, the energy density distribution profile of interface state (N_{ss}) was obtained from the (I_F–V_F) data by taking into account voltage dependent barrier height (BH), n and without R_s. On the other hand, the possible current conduction mechanism (CCM) are determined by utilizing the In(I_F) versus In(V_F) and In(I_R) versus $V_R^{1/2}$ plots. The double logarithmic I_F–V_F plot shows three linear regions which are corresponding to low, moderate and high bias voltages with different slopes (m) as 2.40, 1.96 and 1.27 respectively. While the first region space charge limited current (SCLC) is dominated, the other two regions ohmic behavior is dominated. The field-lowering coefficient (β) was also obtained from the slope of In(I_R)–$V^{1/2}$ plot as 4.40×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$. This value of β is close to theoretical value of Poole–Frenkel emission (PFE) rather than Schottky emission (SE) mechanism.

1 Introduction

Strontium-titanate-oxide (STO) has $SrTiO_3$ chemical formula and some important properties such as a high charge storage capacity, wide bandgap (3.25–3.95 eV), high dielectric constant ($\varepsilon = 310$) excellent optical transparency in the visible region and chemical stability [1, 2]. Therefore, it has been used in microelectronic materials and semiconductor devices such as tunable high temperature superconducting microwave filters, metal–insulator/oxide semiconductor (MIS and MOS), metal-polymer-semiconductor (MPS), MOS field-effect transistors (MOSFETs), ultra-low-temperature scanning microscopes, oxygen sensors, magnetic field insensitive thermometer etc [1–6]. STO film can be also fabricated by various methods such as radio frequency (RF) magnetron sputtering, metal–organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), and sol–gel and it crystallizes in the ABO_3 cubic perovskite structure at room temperature. However, for temperature less than 105 K, it returns to the tetragonal structure [4]. Therefore, in this study, STO was used as interfacial layer between metal and semiconductor to improve the quality or performance of Au/n-Si (MS) structure.

The forward and reverse bias I–V measurements can be supplied more information on the main electrical parameters and possible the CCMs. The main electrical parameters such as the n, reverse saturation current (I_0), Φ_{B0} and energy–density distribution of N_{ss} can be calculated by using the thermionic emission (TE) theory. But, both the existence of R_s, high-dielectric interfacial layer and N_{ss} are more effective on the CCMs. Because, the applied voltage across the diode/structure will be shared by them. Therefore, value of R_s was obtained from both the Norde and Cheung's functions. On the other hand, the reverse bias I_R–V_R plot can be supplied on CTMS [7–12]. For instance, at forward bias region, the space charge limited current (SCLC), trap charge limited current (TCLC) or ohmic behavior can be dominated in the CCMs. When the electrons injections are high and electrons

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escape from the traps, the SCLC mechanism can occur. But, the filling of traps and increase of the space charge because of the number of injected electrons increase can be occurred at the TCLC mechanism [6, 13]. On the other hand, at the reverse bias regions, the Schottky (SE) or Poole–Frenkel (PF) emission may be dominated in the CCMs. According to the SE, current transport occurs across the contact interface instead of the bulk material, but based on the Poole–Frenkel emission, the current transport occurs from the metal into conductive dislocations via trap states [6, 14].

The grown of high-dielectric interfacial layer between metal and semiconductor interface is more importance to the performance and reliability of the MS structures. Therefore, in recently, high-dielectric materials such as TiO_2, $SrTiO_3$ (STO), $Bi_4Ti_3O_{12}$ (BTO) and graphene-doped PVA take the place of the traditional SiO_2 and SnO_2. It is believed that the traditional SiO_2 formed on a semiconductor by the traditional methods cannot passivate the active dangling bonds at the semiconductor surface. On the other hand, this high-dielectric material can be reduced the active dangling bonds and so leads to a decrease of the leakage current, surface states, series resistance and increased of BH. However, the use of a high dielectric interfacial layer does not only prevent inter-diffusion at M/S interface but also alleviates the electric field reduction issue in these structures [15–18]. Therefore, in this study, $SrTiO_3$ was used an interfacial ferroelectric layer between Au and n-Si.

The main aim of this study is characterization of the electrical properties of Au/n-Si structure with high-dielectric $SrTiO_3$ interfacial ferro-electric layer by utilizing both reverse and forward bias current–voltage (I–V) measurements in the wide range of voltage (±5 V) at room temperature. Main electrical parameters of this MFS type structure such as n, Φ_{B0}, R_s were obtained by using various methods (TE, Norde and Cheung's). The energy dependent profile of N_{ss} was calculated for from the forward bias I_F–V_F data by taking into account voltage dependent BH, n, and R_s. The possible CCMs were also determined from both the reverse and forward bias region.

2 Experimental details

Au/$SrTiO_3$/n-Si structure was prepared on n-Si wafer which has (111) surface orientation, 280 μm thick, 5.08 cm diameter and 4.45 Ω cm resistivity. Firstly, the n-Si wafer cleaning and etching processes is traditionally done by using different chemical solvent in ultrasonic bath and then it was rinsed using deionized water with 18 Ω cm resistivity and finally dried with dry nitrogen gas (N_2). After the cleaning process, the wafer was heated optically and loaded into a radio frequency (RF) magnetron sputtering system. The $SrTiO_3$ (STO) thin film was deposited by RF magnetron sputtering method on n-Si wafer. Then, the film was heated at 400 °C in air for 30 min to remove residual organic. High purity (99.999%) gold (Au) with a thickness of ~ 2000 Å was deposited on the whole back side of the n-Si wafer at 10^{-7} Torr by using the high-vacuum metal evaporation system through a shadow Cu mask. In order to get low resistivity ohmic back contact, STO/n-Si wafer was annealed at 700 °C for 60 min in flowing nitrogen ambient at rate of 2 L/min. Finally, the wafer was placed in the same evaporation system and then the high-pure Au rectifier contact with 1 mm diameter and approximately 2000 Å thick formed on the front of n-Si wafer at a rate of 4 Å/s through a Cu shadow mask. Thus, the fabrication processes of Au/$SrTiO_3$/n-Si (MFS) type structures were completed. For the electrical measurements, the fabricated samples were placed on the copper holder and the contacts were made by silver paste and the electrical contacts were also made to the upper electrodes using small thin silver coated wires with silver paste. The current–voltage (I–V) measurements of the structure were carried out with utilizing Keithley 2400 source meter in the VPF-475 cryostat to avoid an external noise and light at room temperature. The sample temperature was monitored by using a copper–constantan thermocouple and a lakeshore 321 auto-tuning temperature controller with sensitivity better than ± 0.1 K.

The schematic diagram of the fabricated Au/$SrTiO_3$/n-Si (MFS) type structures and the measurement forward and reverse bias I–V measurements were given in Fig. 1.

3 Results and discussion

The conduction mechanism of a diode is defined by utilizing the thermionic emission (TE) theory. According to this theory, the forward bias I–V relation can be expressed as [6];

$$I = I_0\left[\exp\left(\frac{q\left(V - IR_s\right)}{nkT}\right) - 1\right] \tag{1}$$

where I_0 is the reverse saturation current, V is applied bias voltage, q is the electric charge (1.6×10^{-19} coulombs), k is the Boltzmann constant (1.38×10^{-23} J/K), n is the ideality factor, T is the absolute temperature (K), R_s is the series resistance of the sample and the IR_s term is voltage drop on R_s. The I_0 is given by following equation for any temperature;

$$I_0 = AA^*T^2\exp\left(-\frac{q\phi_{B0}}{kT}\right) \tag{2}$$

where A is the rectifier contact area (7.85×10^{-3} cm^2), A* is the effective Richardson constant (112 for n-Si), Φ_{B0} is the zero bias barrier height. Firstly, the value of I_0 can be

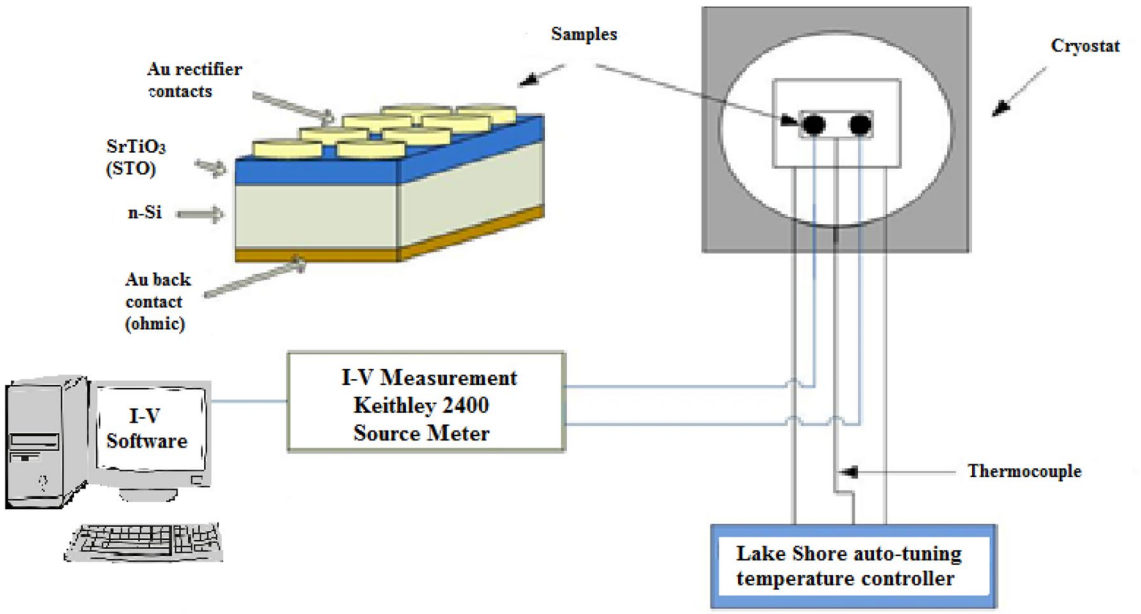

Fig. 1 The schematic diagram of the fabricated Au/$SrTiO_3$/n-Si (MFS) type structures and the I–V measurement system

obtained from the intercept of the linear part of the forward bias current–voltage characteristic and then the Φ_{B0} is defined by following equation:

$$\phi_{B0} = \frac{kT}{q} In\left(\frac{AA^*T^2}{I_0}\right) \tag{3}$$

The ideality factor (n) of the diode is obtained by using the experimental forward bias current–voltage data. It was calculated from the slope of the linear part of the forward bias current–voltage characteristic and may be written as

$$n = \frac{q}{kT}\left(\frac{dV}{d(In\ I)}\right) \tag{4}$$

The reverse and forward bias semi-logarithmic I–V plot of the Au/$SrTiO_3$/n-Si (MFS) structure is illustrated in Fig. 2. As shown in Fig. 2, the forward bias current plot in the range of 0.1 V < V < 0.3 V shows a distinct linear behavior and then because of the effect R_s and interlayer the semi-logarithmic I–V plot is deviated from the linearity. Since the voltage applied on the sample it will be shared by depletion layer, interfacial layer and R_s. But the effect of R_s can be eliminated low in the linear part of LnI–V plot [19, 20]. The non-saturation behavior in the reverse current can be commonly explained in the terms of the image force lowering of the BH between metal and semiconductor and inhomogeneity of barrier height. If we used this linear part, we can calculate the values of both Φ_{B0} and n. The values of Φ_{B0} and n are found as 0.60 eV and 2.45 by using the TE at room temperature, respectively. Similar result have been reported

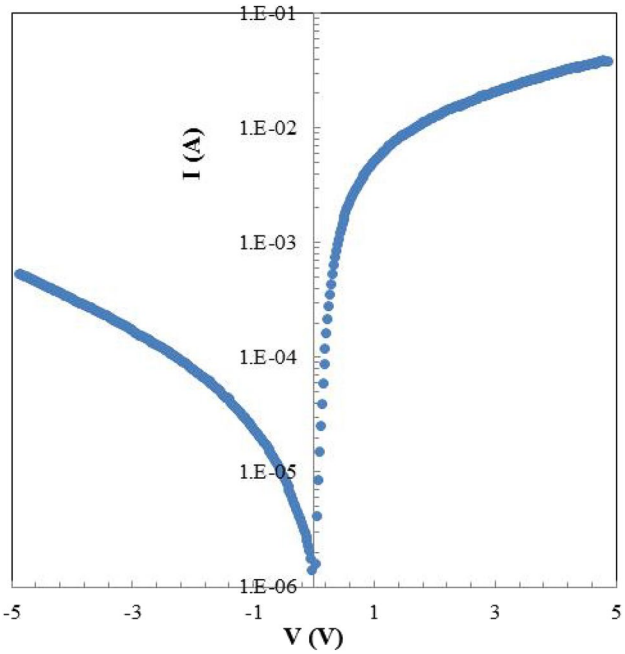

Fig. 2 The semi-logarithmic forward and reverse I–V characteristic of the Au/$SrTiO_3$/n-Si (MFS) structure at room temperature

in the literature for MIS [19–23], MPS [24] and MFS [18] structures.

As can be seen in Fig. 2, the value of R_s is more effective on the forward bias I–V characteristics and leads to deviated from the linearity of I–V plot at enough high forward bias voltage. In general, R_s can originate from five different sources; (a) the back ohmic contact to the semiconductor,

(b) the contact made by the probe wire to the gate or rectifier contact, (c) the bulk resistance of the semiconductor, (d) a particulate matter at back contact/pedestal interface and (e) non-uniform doped atoms in the semiconductor [23, 25]. It can be reduced either by having a low BH at M/S interface or by having an enhanced tunneling through the barrier by using heavy doped semiconductors ($\geq 10^{17}$ cm^{-3}) or by the use of a good cleaning and fabrication process. In order to the estimation of the R_s from the forward bias I–V data one of the most commonly used methods are the modified Norde functions by Bohlin [26] and Cheung [27] functions. According to Bohlin, an alternative easy method to determine the barrier height (Φ_B) and R_s can be expressed as [26]:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\left[\ln\left(\frac{I(V)}{AA^*T^2}\right)\right] \tag{5}$$

where γ is a dimensionless integer and it should be selected greater than n. According to this method, the values of Φ_B and are given by Eqs. 6 and 7, respectively.

$$\Phi_B = F(V_o) + \frac{V_o}{\gamma} - \frac{kT}{q} \tag{6}$$

where $F(V_o)$ is the minimum value of the F(V)–V plot. Thus the value of R_s can be extracted from the Norde function as:

$$R_s = \frac{kT(\gamma - n)}{qI_{min}} \tag{7}$$

The F(V) versus V(V) plot of Au/$SrTiO_3$/n-Si (MFS) structure at room temperature is given in Fig. 3. This plot gives a minimum point and both Φ_B and R_s are calculated by utilizing this minimum point. The values of Φ_B and R_s were found 0.61 eV and 87.83 Ω at room temperature, respectively.

Also, the values of R_s, n and Φ_B can be obtained from another alternative method which is known as Cheung functions. Cheung's functions were defined as [27];

$$\frac{dV}{d(In\ I)} = IR_s + \left(\frac{nkT}{q}\right) \tag{8}$$

and

$$H(I) = V - \frac{nkT}{a} In\left(\frac{I}{AA^*T^2}\right) = IR_s + n\phi_{B0} \tag{9}$$

Both the dV/dIn (I) versus I and H(I) versus I plots are illustrated in Fig. 4. It is clear that these two plots have a good linear behavior in the wide range of forward bias current. The value of R_s is found from the slope of the both dV/dIn (I) versus I and H(I) versus I plots. The obtained R_s values from these slopes are found as 137.57 and 121.04 Ω, respectively. It is shown that, the calculated values of R_s are in close agreement with each other. On the other hand, the value of n was found as 2.95 from the intercept of dV/dIn (I) versus I plot. After that, the value of Φ_B was obtained as 0.48 eV from the intercept of H(I) versus I plot. This discrepancy in n and Φ_B is the result of voltage dependent [6, 7].

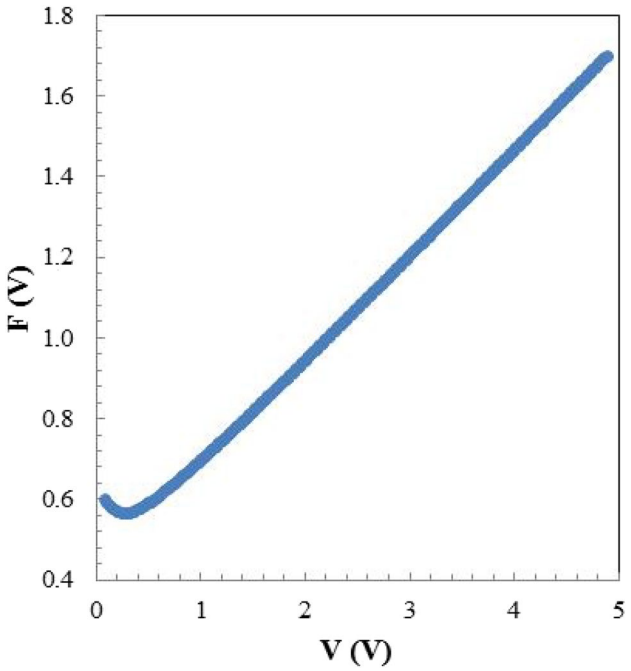

Fig. 3 F(V) versus V (V) plot of the Au/$SrTiO_3$/n-Si (MFS) structure at room temperature

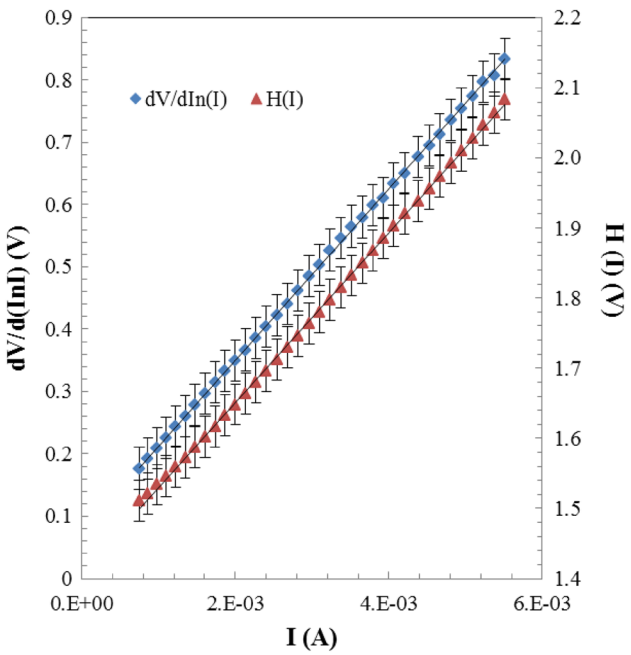

Fig. 4 dV/d(InI) and H(I) versus I plots of Au/$SrTiO_3$/n-Si (MFS) structure at room temperature

The existence of N_{ss} located between interfacial layer and semiconductor are also more effective on the forward bias I–V characteristics. Unless specifically manufactured the MS, MIS, MPS and MFS structures, many N_{ss}, bulk traps and dislocations can be occurred which lead to electronic states with energies located in the forbidden band gap of the semiconductor between metal and semiconductor. When the interfacial layer thickness is higher than 30 Å, these states/traps are equilibrium with semiconductor rather than metal. These states can be altered the performance of these devices and they usually originated from defects such as dangling bounds at the insulator/substrate interface with energy states in the semiconductor band gap (E_g) and are dependent on the chemical composition of the interface [6, 7, 22, 27]. Therefore, the density of N_{ss} for the Au/$SrTiO_3$/n-Si (MFS) structure was also calculated by using following equations (Eqs. 10–13) by taking into account voltage dependent effective BH (Φe), n (V) and R_s and presented in Fig. 5 [7, 22, 27]:

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\delta}{\varepsilon_i}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right] \tag{10}$$

where, δ is the thickness of interfacial insulator layer (5×10^{-7} cm), W_D is the depletion layer width, ε_i is permittivity of the interfacial insulator layer, ε_s is permittivity of the semiconductor and ε_0 is the permittivity of the free space.

$$n(V) = \frac{qV_d}{kTLn\left(I/I_0\right)} \tag{11}$$

Moreover, the energy dependent value of the N_{ss} with respect to the top of the conduction band (E_c) at the surface of semiconductor is given as:

$$E_c - E_{ss} = q\left(\Phi_e - V_d\right) \tag{12}$$

$$\Phi_e - \Phi_{B0} = \left(1 - \frac{1}{n(V)}\right)V_d \tag{13}$$

In Eqs. 1–13, V_d is the voltage across on the structure ($= V - IR_s$). When these structures have an interfacial layer and R_s, the applied bias voltage will be shared by them. The calculated mean value of N_{ss} is approximately 10^{13} eV^{-1} cm^{-2} and this value may be noted suitable for a semiconductor device. However, these values with R_s is almost one order lower than the without R_s. All of these results show that both the value of R_s and interfacial layer thickness must be taken into account in the calculations.

In order to determine separately the dominant current transport mechanisms in both the forward and reverse bias regions, In (I_F) versus In (V) and In (I_R) versus $V^{1/2}$ plots were drawn. The first of these is the In (I_F) versus In (V) plot and is shown in Fig. 6. This plot has three district linear regions which have different slopes. The region 1 ($-3.25 < V < -1.35$), region 2 ($-1.21 < V < -0.28$) and region 3 ($-0.15 < V < 1.61$) obey I–V^m change. The m is the slope of each region and was obtained 2.40, 1.96 and 1.27 respectively. At first region which is known as low bias region, the dominant conduction mechanism is space charge limited current (SCLC) because of the value of m is higher than two. On the other hand at second region which is known as moderate bias region and third region which is known as high bias region, the dominant conduction mechanism

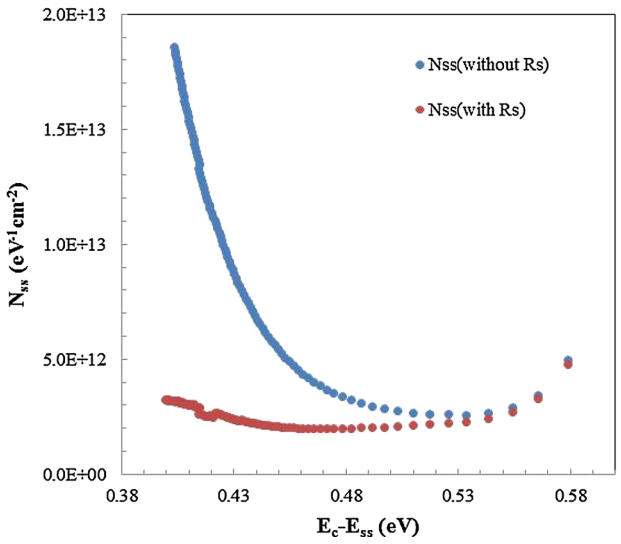

Fig. 5 N_{ss} versus E_c–E_{ss} plots with and without of R_s for the Au/$SrTiO_3$/n-Si (MFS) structure at room temperature

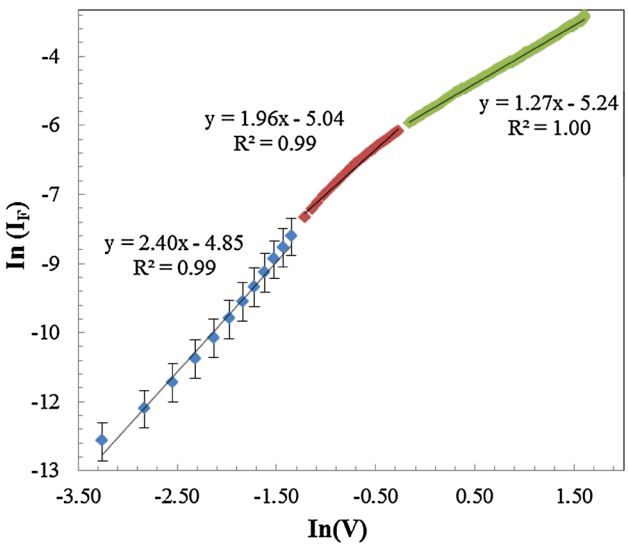

Fig. 6 The In(I_F) versus In(V) plot of the Au/$SrTiO_3$/n-Si (MFS) structure at room temperature

is ohmic behavior because of the value of m is close to the unity [28–32]. The obtained experimental main electrical parameters of the Au/$SrTiO_3$/n-Si (MFS) structure show that the possible current conduction mechanism in the forward bias region may be different from region to region depend on a special distribution of N_{ss}, barrier and interfacial layer inhomogeneity between metal and semiconductor.

The reverse bias I–V characteristics is general different from the forward bias I–V characteristics. In the reverse bias region, the current mechanisms are usually can be explained by using Poole–Frenkel emission (PFE) and Schottky emission (SE) theories. If the PFE mechanism is dominant, the reverse current can be expressed as [14, 29–35]:

$$I_R = I_0 \exp\left(\frac{\beta_{PF} V^{1/2}}{kTd^{1/2}}\right) \tag{14}$$

If the SE mechanism is dominant, the reverse current can be expressed as;

$$I_R = AA^*T^2 \exp\left(\frac{-\Phi_b}{kT}\right) \exp\left(\frac{\beta_{SC} V^{1/2}}{kTd^{1/2}}\right) \tag{15}$$

where β_{PF} and β_{SC} are the field-lowering coefficients of PFE and SE, respectively. The theoretical values of these coefficients are given in following equation.

$$2\beta_{SC} = \beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_0\varepsilon_r}\right)^{1/2} \tag{16}$$

where ε_r is the relative permittivity of interfacial layer. As shown in Eq. 16, the value of β_{PF} is always twice the value of β_{SC}. The theoretical value of both β_{PF} and β_{SC} are found as 4.30×10^{-6} and 2.1×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$, respectively. The $In(I_R)$ versus $V^{1/2}$ plot of Au/$SrTiO_3$/n-Si structure is shown in Fig. 7. As seen in Fig. 7, the plot has a district linear variation. The field-lowering coefficient is found by using of the slope of this linear region. The value of field-lowering coefficient is calculated as 4.40×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$. The obtained value of field-lowering coefficient is close to theoretical value of PFE coefficient. This result shows that the dominant reverse bias conduction mechanism is PFE mechanism. So, the carrier transport is formed from the metal into conductive dislocations via trap states.

4 Conclusions

In this study, both the reverse and forward bias current–voltage (I–V) characteristics in the Au/$SrTiO_3$/n-Si (MFS) structure have been analyzed in the wide range of voltage (± 5 V) at room temperature by using various methods. The value of Φ_{B0} is found as 0.60, 0.61 and 0.48 eV by using the TE, Norde function and Cheung functions, respectively. The value of n is found as 2.45 and 2.95 by using the TE and Cheung functions, respectively. The value of R_s was found as 87.83 Ω (from Norde function), 135.87 Ω [from dV/dIn (I) vs. I plot] and 121.04 Ω [from H(I) vs. I plot]. The energy density distribution of N_{ss} for the MFS structure was obtained from the forward-bias I–V data by takin into account voltage dependent Φ_e, n and Rs. The calculated value of the N_{ss} is ~ 10^{13} eV^{-1} cm^{-2} without of R_s but they found as ~ 10^{12} eV^{-1} cm^{-2}. In addition, the possible dominant current transport mechanisms of both forward and reverse bias regions were determined by using the In (I_F) versus In (V) and In (I_R) versus $V^{1/2}$ plots. The dominant conduction mechanisms of the forward bias regions are SCLC at low bias region and ohmic behavior at high bias region. The obtained results show that the possible current conduction mechanism in the forward bias region may be different from region to region depend on a special distribution of N_{ss}, barrier and interfacial layer inhomogeneity between metal and semiconductor. The value of field-lowering coefficient is calculated as 4.40×10^{-6} eV^{-1} $m^{1/2}$ $V^{1/2}$from the reverse bias I–V characteristics and it is close to theoretical value of PFE coefficient. This result shows that the dominant reverse bias conduction mechanism is PFE mechanism. So, the carrier transport is formed from the metal into conductive dislocations via trap states.

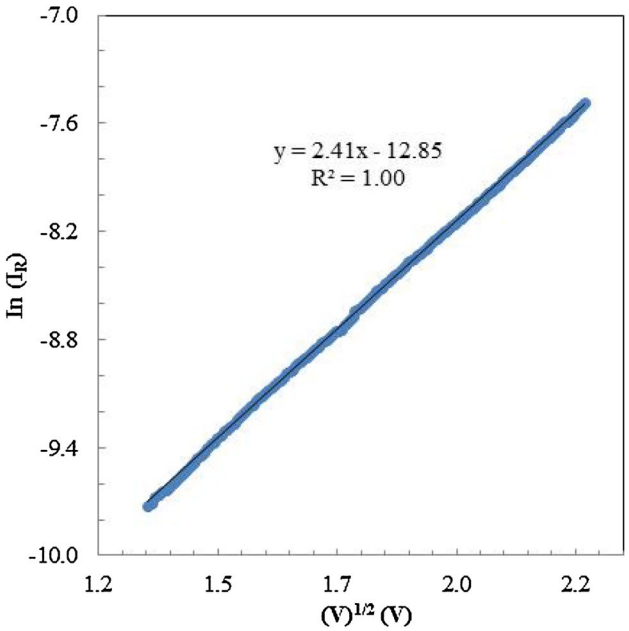

Fig. 7 Ln (I_R) versus $V_R^{1/2}$ plot of the Au/$SrTiO_3$/n-Si (MFS) structure at room temperature

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References

1. K. van Benthem, C. Elsässer, R.H. French, 'Bulk electronic structure of $SrTiO_3$: experiment and theory'. J. Appl. Phys. **90**, 6156 (2001)
2. R.K. Gupta, K. Ghosh, P.K. Kahol, 'Fabrication and electrical characterization of Au/p-Si/STO/Au contact'. Curr. Appl. Phys. **9**, 933–936 (2009)
3. M.K. Hudait, M. Clavel, Y. Zhu, P.S. Goley, S. Kundu, D. Maurya, S. Priya, 'Integration of $SrTiO_3$ on crystallographically oriented epitaxial Germanium for Low-Power device applications'. ACS Appl. Mater. Interfaces **7**, 5471–5479 (2015)
4. G. Panomsuwan, O. Takai, N. Saito, 'Enhanced memory window of Au/$BaTiO_3$/$SrTiO_3$/Si (001) MFIS structure with high *c*-axis orientation for non-volatile memory applications. Appl Phys A **108**, 337–342 (2012)
5. İ Taşcıoğlu, Ö Tüzün Özmen, H.M. Şağban, E. Yağlıoğlu, Ş. Altındal, 'Frequency dependent electrical and dielectric properties of Au/P3HT:PCBM:F4-TCNQ/n-Si Schottky Barrier Diode'. J. Electron. Mater. **46**, 2379–2386 (2017)
6. S.M. Sze, *Physics of Semiconductor Devices*, 2nd edn. (Wiley, New York, 1981), pp. 362–380
7. E.H. Rhoderick, R. H. Williams, *Metal Semiconductor Contacts*, 2nd edn. (Clarendon Press, Oxford, 1988), pp. 257–267
8. S.R. Forrest, Ultrathin organic films grown by organic molecular beam deposition and related techniques. Chem. Rev. **97**, 1793–1896 (1997)
9. R.T. Tung, Formation of an electric dipole at metal-semiconductor interfaces. Phys. Rev. B **64**, 205310 (2001)
10. S.G. Wang, Y. Zhang, Y.M. Zhang, Y.M. Zhang, Characterization of ion-implanted 4H-SiC Schottky barrier diodes. Chin. Phys. B **19**, 017203 (2010)
11. A. Tataroglu, Comparative study of the electrical properties of Au/n-Si (MS) and Au/Si_3N_4/n-Si (MIS) Schottky diodes. Chin. Phys. B **22**, 068402 (2013)
12. S. Chand, On the intersecting behaviour of current–voltage characteristics of inhomogeneous Schottky diodes at low temperatures. Semicond. Sci. Technol. **19**, 82 (2004)
13. A.C. Varghese, C.S. Menon, Electrical properties of hybrid phthalocyanines thin films using gold and lead electrodes. Eur. Phys. J. B **47**, 485 (2005)
14. V. Janardhanam, H.K. Lee, K.H. Shim, H.B. Hong, S.H. Lee, K.S. Ahn, C.J. Choi, Temperature dependency and carrier transport mechanisms of Ti/p-type InP Schottky rectifiers. J. Alloys Compd. **504**, 146 (2010)
15. S. Hlali, A. Farji, N. Hizem, L. Militaru, A. Kalboussi, A. Souifi, High temperature and voltage dependent electrical and dielectric properties of TiN/Al_2O_3/p-Si MIS structure. J. Alloys Compd. **713**, 194–203 (2017)
16. H. Trabelsi, M. Bejar, E. Dhahri, M. Sajieddine, K. Khirouni, P.R. Prezas, B.M.G. Melo, M.A. Valente, M.P.F. Graça, Effect of oxygen vacancies on $SrTiO_3$ electrical properties. J. Alloys Compd. **723**, 894–903 (2017)
17. G.D. Wilk, R.M. Wallace, J.M. Anthony, High-k gate dielectrics: current status and materials properties considerations. J. Appl. Phys. **89**, 5243–5275 (2001)
18. H.G. Çetinkaya, M. Yıldırım, P. Durmuş, Ş Altındal, Correlation between barrier height and ideality factor in identically prepared diodes of Al/$Bi_4Ti_3O_{12}$/p-Si (MFS) structure with barrier inhomogeneity. J. Alloys Compd. **721**, 750–756 (2017)
19. A. Tataroğlu, Ş Altındal, The analysis of the series resistance and interface states of MIS Schottky diodes at high temperatures using I–V characteristics. J. Alloys Compd. **484**, 405 (2009)
20. H. Tanrıkulu, A. Tataroğlu, E.E. Tanrıkulu, A.B. Uluşan, Electrical characterization of MIS diode prepared by magnetron sputtering. IJPAP **56**, 142–148 (2018)
21. Ö Vural, N. Yıldırım, Ş Altındal, A. Türüt, Current–voltage characteristics of Al/Rhodamine-101/n-GaAs and Cu/Rhodamine-101/n-GaAs rectifier contacts. Synt. Metal. **157**, 679–683 (2007)
22. Ş Altındal, İ Yücedağ, A. Tataroğlu, Analysis of surface states and series resistance in Au/n-Si Schottky diodes with insulator layer using current-voltage and admittance—voltage characteristics. Vacuum **84**, 363–368 (2010)
23. A. Tataroğlu, Ş Altındal, Characterization of current–voltage (I–V) and capacitance–voltage– frequency (C–V–f) features of Al/SiO_2/p-Si (MIS) Schottky diodes. Microelectron. Eng. **83**, 582–588 (2006)
24. A. Büyükbaş Uluşan, A. Tataroğlu, Y. Azizian-Kalandaragh, Ş Altındal, On the conduction mechanisms of Au/(Cu_2O–CuO–PVA)/n-Si (MPS) Schottky barrier diodes (SBDs) using current–voltage–temperature (I–V–T) characteristics. J. Mater. Sci. **29**, 159–170 (2018)
25. E.H. Nicollian, J.R. Brews, *MOS Physics and Technology*, 2nd edn. (Wiley, New York, 1982), pp. 71–150
26. K.E. Bohlin, Generalized Norde plot including determination of the ideality factor. J. Appl. Phys. **60**, 1223 (1986)
27. S.K. Cheung, N.W. Cheung, Extraction of Schottky diode parameters from forward current-voltage characteristics. Appl. Phys. Lett. **49**, 85 (1986)
28. S.B.K. Aydin, D.E. Yıldız, H.K. Çavuş, R. Şahingöz, ALD TiO_2 thin film as dielectric for Al/p-Si Schottky diode. Bull. Mater. Sci. **37**, 1563–1568 (2014)
29. A. Tataroglu, A.A. Hendi, R.H. Alorainy, F. Yakuphanoglu A new aluminum iron oxide Schottky photodiode designed via sol–gel coating method. Chin. Phys. B **23**, 057504 (2014)
30. S. Alialy, D.E. Yıldız, Ş Altındal, Study on the reverse bias carrier transport mechanism in Au/TiO_2/n-4H-SiC structure. J. Nano. Opto. **11**, 626–630 (2016)
31. V. Rajagopal Reddy, V. Manjunath, V. Janardhanam, Y.-H. Kıl, C.-J. Cho, Electrical properties and current transport mechanisms of the Au/n-GaN Schottky structure with solution-processed high-k $BaTiO_3$ interlayer. J. Electron. Mater. **43**, 3499 (2014)
32. K. Sreenu, C. Venkata Prasad, V. Rajagopal, Reddy, Barrier parameters and current transport characteristics of Ti/p-InP schottky junction modified using orange G (OG) Organic Interlayer. J. Electron. Mater. **46**, 5746 (2017)
33. A.C. Varghese, C.S. Menon, Electrical properties of hybrid phthalocyanines thin films using gold and lead electrodes. Eur. Phys. J. **47**, 485–489 (2005)
34. A. Ashok Kumar, V. Rajagopal Reddy, V. Janardhanam, H.D. Yang, H.J. Yun, C.J. Choi, Electrical properties of Pt/n-type Ge Schottky contact with PEDOT:PSS interlayer. J. Alloys Compd. **549**, 18–21 (2013)
35. V. Janardhanam, Y.K. Park, K.S. Ahn, C.J. Choi, Carrier transport mechanism of Se/n-type Si Schottky diodes. J. Alloys Compd. **534**, 37–41 (2012)