Journal of Materials Science: Materials in Electronics (2018) 29:15761–15769
https://doi.org/10.1007/s10854-018-9240-8

Gate modeling of metal–insulator–semiconductor devices based on ultra-thin atomic-layer deposited TiO_2

Hector Uribe-Vargas[1] · Joel Molina-Reyes[1] · Alejandra Romero-Morán[1] · Eduardo Ortega[2] · Arturo Ponce[1,2]

Received: 21 November 2017 / Accepted: 3 May 2018 / Published online: 7 May 2018

Abstract
Metal–insulator–semiconductor devices having different oxide thicknesses (10, 6, 4 and 2 nm) were fabricated using atomic-layer deposited ultra-thin amorphous TiO_2 as gate dielectric. From Ig–Vg measurements it was determined that the main conduction mechanism is Schottky emission for all thicknesses and even after passivation of the semiconductor–insulator interface using SiO_x. Furthermore, the Schottky barrier height (Φ_B) increases when the oxide thickness decreases; this was further corroborated using semi empirical models and SILVACO simulations having excellent agreement. From this analysis, important physical parameters like barrier height (Φ_B), effective mass (m*) and optical dielectric constant ($\boldsymbol{\varepsilon}_r$) were extracted, and could be used to effectively understand the performance and reliability of these devices. From the extraction of physical parameters associated to the conduction mechanism, a correlation between materials' properties with device performance could be obtained (higher barrier height (Φ_B) would result in a decrease in leakage current). Also, the high reproducibility enables enhanced performance and therefore, better reliability predictions for electron devices based on these oxides.

1 Introduction

Titanium dioxide (TiO_2) has been widely studied due to its low cost, light weight, and long-term stability [1–3]. The crystalline based TiO_2 such as anatase and rutile have been widely studied due to its electronic structure [4–6], meanwhile, amorphous TiO_2 could also play a crucial role as an active photocatalyst, a protection layer or to increase the effective dielectric constant in MOSFET based devices [7–9]. Thus, it is important to accurately understand the conduction mechanism of amorphous thin films TiO_2 in order to obtain a higher level of performance and being able to predict the reliability of such devices. In this work, we have studied the current carrier transport properties of ultra-thin TiO_2 deposited by thermal atomic-layer deposition (ALD). For this, metal–insulator–semiconductor (MIS) devices were fabricated and their morphological and electrical characteristics were measured. Devices with four different thicknesses (10, 6, 4, and 2 nm) and a set of each passivated resulted in eight different samples. This passivation promotes the development of an interfacial layer between silicon and TiO_2. Also, as the oxide thickness decreases, the barrier height increases, thus resulting in lower gate leakage current. The main conduction mechanism was found to be Schottky emission, and from the extraction of the physical parameters associated to this conduction mechanism, correlation of materials' properties with device performance could be made. For instance, oxides with increased barrier heights Φ_B (same thickness) would result in a decrease in the leakage current. Also, given that the current–voltage (Ig–Vg) and capacitance voltage (C–V) characteristics for these MIS devices are highly dependent on the quality of the deposition of TiO_2 and its interface with silicon, the presence of defects like oxygen vacancies or interface states, or even an inappropriate nucleation, will also have a major impact on the performance of these simple devices. Therefore, a simple mechanism explaining conduction models correlated to barrier heights and its alignments with silicon help us to understand and possibly modulate the electrical behavior of these devices. Finally, the high reproducibility, conformality, outstanding control (to atomic level) on the thickness and

✉ Hector Uribe-Vargas
hecuribe@inaoep.mx

Joel Molina-Reyes
jmolina@inaoep.mx

[1] Electronics Department, National Institute of Astrophysics, Optics and Electronics, Luis Enrique Erro No. 1, Santa Maria Tonantzintla, 72840 Puebla, Mexico

[2] Department of Physics and Astronomy, University of Texas at San Antonio, One UTSA Circle, San Antonio, TX 78249, USA

stoichiometry, interface properties with the semiconductor substrate, and the low deposition temperature ($T \leq 250$ °C) for these metal oxides, puts ALD as a powerful deposition technique which enables enhanced performance and therefore, better reliability predictions for electron devices based on these oxides.

2 Experimental details

300 µm thick, n-type, 2–5 Ω cm resistivity, with a (100) surface plane silicon wafers were used as semiconductor substrate. Initial cleaning (RCA cleaning, HF-last) of these wafers was followed by thermal ALD of TiO_2 (10, 6, 4, and 2 nm) at 250 °C using tetrakis(dimethylamino)titanium and water as precursors. Right after deposition of TiO_2, electron-beam evaporation of the metal gate (aluminium = 400 nm at 10 Å/s) was done in ultra-high vacuum conditions while keeping a transitioning time (from ALD to evaporation) less than 2 min in order to minimize any exposure of TiO_2 to the clean room's atmosphere. Standard photolithography for wet-etching of aluminium was used in order to properly define the metal gate patterns. Figure 1a, b show the process flow and the eight fabricated MIS structures (four of them with a SiO_x passivation).

After fabrication, all structures were characterized using a semiconductor-device analyzer (SDA 4200 from Keithley), and at least 15 devices were measured for each condition in order to ensure reproducibility. Current–voltage (Ig–Vg), capacitance–voltage (C–V), and current–voltage–temperature (Ig–Vg–T) measurements were made at room temperature, in dark conditions, and with electromagnetic isolation.

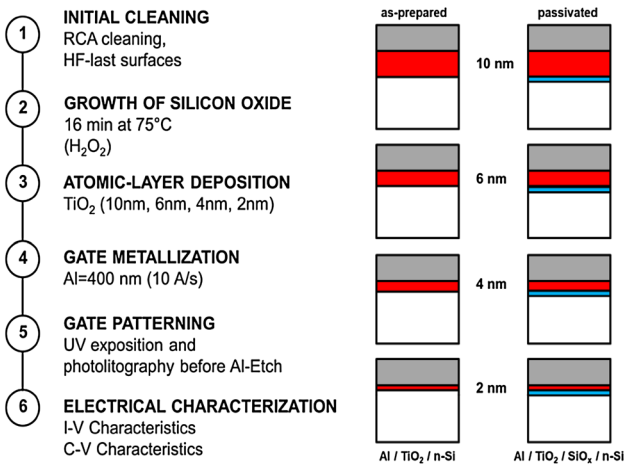

Fig. 1 **a** Process flow for fabrication of MIS structures using TiO_2 as gate oxide, **b** Schematic of the resulting MIS structures having eight samples with 10, 6, 4 and 2 nm of physical thickness for TiO_2 and also, a passivation treatment. It is expected that passivated samples result in less interfacial states

3 Material characterization

3.1 FTIR measurements

Chemical analysis by FTIR (Bruker Vector-22) at room temperature was performed for the films formed on silicon wafers just after the deposit by ALD for both the as-prepared and passivated MIS devices to analyze the thin film structure. The formation of TiO_2 on the surface of silicon wafers of the as-prepared devices was confirmed by the characteristic peaks observed below 1000 cm^{-1} [10], however, no specific bands of rutile or anatase phase were observed. The existence of intense bands in 610 and 1100 cm^{-1} associated with vibrational modes of the Si–O bonds [11], indicate silicon dioxide thermal growing on the silicon wafer surface during material deposition, so it is suggested that surface presence of TiO_2 is not uniform, a phenomenon that could be associated with the lack of nucleation observed in very thin deposits by ALD (Fig. 2a).

For the passivated devices the typical absorbance bands associated with the presence of TiO_2 were not observed, instead, a large decrease in the absorbance band associated with the presence of silicon dioxide around 1200 cm^{-1} is observed as seen in Fig. 2b. The decrease of this signal could be explained due to the presence of titania that screens-out the silicon dioxide underneath. However, it is also important to mention that the absence of any absorbance vibrational mode for TiO_2 could mean an incomplete nucleation of this film during the ALD process. It is known that in order to properly nucleate ultra-thin TiO_2 films on silicon, delicate conditions must be met regarding the chemical nature of the silicon surface [12, 13]. In particular, there must be an adequate density of proper chemical species on silicon, so that the possibility of an unsaturated surface chemistry (leading to undesired interfacial reactions), could be minimized and thus, promote proper nucleation given the self-limited reactions during the sequential introduction of the titanium and oxygen precursors. Also, a complete nucleation of thermal ALD-based TiO_2 is enhanced for relatively thicker films on silicon, where even the anatase phase could be obtained [14–16]. Nevertheless, this problem could somewhat be alleviated by introducing super-saturated cycles for each precursor being sequentially introduced during the ALD process of even thinner TiO_2 [14].

3.2 X-ray diffraction

The crystalline phases of the resulting TiO_2 films obtained after X-ray diffraction (XRD) measurements (Philips

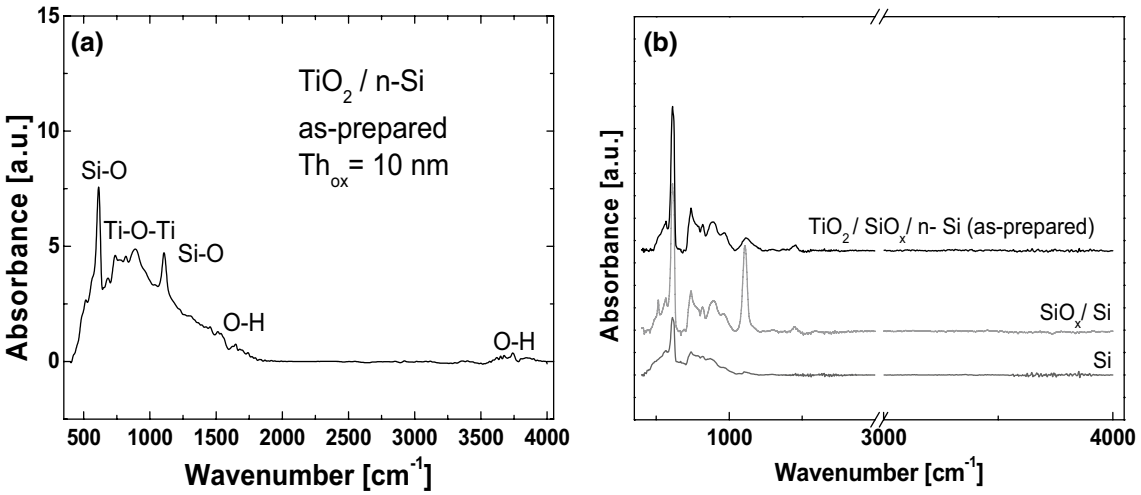

Fig. 2 **a** FTIR measurements of the as-prepared MIS devices. **b** FTIR spectra for ALD titanium dioxide thin films (10 nm TiO_2) before and after passivation with SiO_x

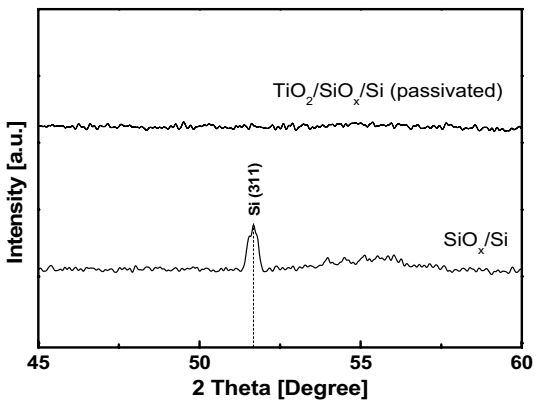

Fig. 3 XRD patterns for the ultra-thin chemical oxide used as passivation layer on silicon (SiO_x layer) and the titanium dioxide thin film (10 nm of TiO_2 deposited on SiO_x/Si) in the passivated condition

X'Pert MPD), with a scanning step of 0.02°, using Cu–Kα radiation with λ = 1.5406 Å as an X-ray source are shown in Fig. 3. There, we show the XRD patterns for SiO_x/Si and the TiO_2/SiO_x/Si structures obtained. For only the chemical oxide on silicon (SiO_x/Si structure), a diffraction peak at 52° was observed and associated with the (311) plane of silicon. This peak disappears when an ultra-thin film of titania is deposited as shown in the passivated XRD pattern, where no signal was observed suggesting the presence of amorphous material. This shows that the TiO_2 layers (10 nm in thickness for the XRD data) could be largely present in an amorphous phase or, for the thinner films, present an incomplete nucleation due to the unsaturated reactions during the first ALD cycles.

3.3 HR-TEM measurements

High resolution TEM (HRTEM) was used to observe the structure from a cross-sectioned area of the MIS device (TiO_2 = 2 nm in physical thickness). A polycrystalline thick top aluminium layer can be observed in the cross-section. Figure 4a, c shows that the aluminium top layer is formed by columnar grains running perpendicular to the TiO_2/silicon structure (grain boundaries at 90°) for both samples. The HR TEM images show the gate oxide for both as-prepared and passivated devices, (Fig. 4a, c). Even though the EDS analysis shows no titanium presence, it is evident that a partially crystallized gate oxide with the desired thickness is present on the silicon substrate. Although a detailed compositional characterization for this gate oxide is needed (like Angle-resolved X-ray photoelectron spectroscopy (AR-XPS), which is able to resolve chemical composition and other details with spatial resolution in the nanoscale), we observe a combined crystallized and amorphous phase for the resulting gate oxide, and also, the presence of the ultra-thin chemical oxide (SiO_x) in the passivated samples. From the fast Fourier transform (FFT) images displayed in Fig. 4b1, b2, aligned to the <011> zone axis, it is possible to determine the Si-substrate (200) planes parallel to the growth direction of the gate oxide. Experimental distances from the FFT are in close agreement with expected values of the diffraction spots of Si. Indexing this FFT, an interplanar distance of 0.3169, 0.2779 and 0.1958 nm for its (111), (200) and (220) planes can be measured. As the imaged aluminium grain is away of any zone axis, only 0.235 nm stripes can be measured, which points to the values for (111) Al planes.

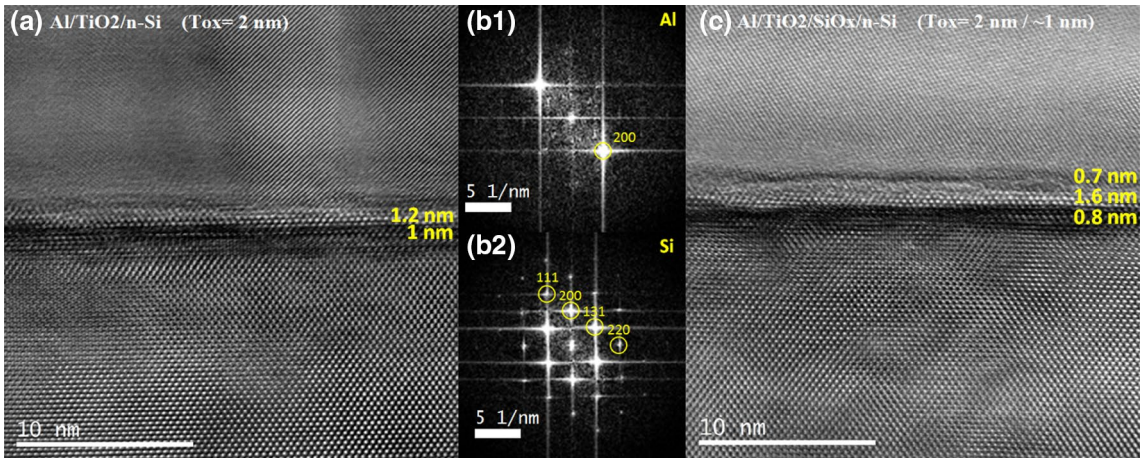

Fig. 4 **a** HR-TEM image of the as-prepared MIS devices with $TiO_2 = 2$ nm in expected physical thickness. FFT images showing the crystalline planes associated to **b1** aluminium and **b2** silicon substrate. **c** HR-TEM image of passivated MIS devices. In this case, a $TiO_2 = 2$ nm in physical thickness is deposited on top of an ultra-thin chemical oxide (SiO_x ~1 nm in thickness)

4 Theory of conduction mechanisms

When a moderate E (in the form of an applied gate voltage Vg) is applied and sustained across a MIS device, it generates a gate current that flows throughout the oxide. The studying of this tunneling current helps to identify conduction mechanisms that in turn, are strongly related to important physical parameters in the gate oxide (TiO_2 in this case) thus giving us information about its general physical properties [17–20].

Temperature dependent Ig–Vg measurements must also be performed in the MIS devices in order to accurately determine the right CM present. In our samples, it is found that the main conduction mechanism is Schottky emission, obtained from Ig–Vg–T measurements and that was confirmed with the corresponding theoretical models by using analytical expressions and computer-aided design (CAD) tools after simulations in SILVACO. Due to the temperature dependence, Poole–Frenkel emission was also explored, nevertheless, it was determined that this CM was not present for these samples.

4.1 Schottky emission

This current conduction mechanism is due to an electron emission from the semiconductor in accumulation to the dielectric, this is one of the most observed CM in dielectric films, especially at relatively high temperatures. The expression is given by [21]

$$J = A^* T^2 \exp\left[-\frac{q\left(\Phi_B - \sqrt{qE/(4\pi\varepsilon_r\varepsilon_o)}\right)}{k_B T}\right], \quad A = \frac{120\, m^*}{m_0} \tag{1}$$

where A* is the effective Richardson constant, T is the absolute temperature, q is the electronic charge $q\Phi_B$ is the Schottky barrier height, E is the electric field across the dielectric, m_0 is the electron mass, m* is the effective mass, k_B is the Boltzmann constant, ε_o is the permittivity in vacuum and ε_r is the optical dielectric constant, this value should be close to the square of the refractive index ($\varepsilon_r = n^2$).

4.2 Poole–Frenkel emission

This current conduction mechanism considers an electron in a trapping center within the oxide; where the Coulomb potential energy of the electron can be reduced by an applied electric field across the dielectric film. Then, the reduction in potential energy may increase the probability of an electron being thermally excited out of the trap into the conduction band of the dielectric. This makes this conduction mechanism highly dependent on temperature. The expression for PF emission is given by [21]:

$$J = q\mu N_C E \exp\left[-\frac{q\left(\Phi_T - \sqrt{qE/(\pi\varepsilon_i\varepsilon_o)}\right)}{k_B T}\right] \tag{2}$$

where $q\Phi_T$ is the trap energy level found in the energy gap of the oxide (taken from the minimum of its conduction band and below), and ε_i is the optical dielectric constant, the other variables are defined as before. For this conduction model, we notice a strong dependence of gate leakage current with temperature.

5 Results and discussion

Figure 5a shows the Ig–Vg experimental data for the as-prepared MIS devices having $TiO_2 = 2$, 4, 6 and 10 nm as gate dielectric oxide, as seen, no clear relation between current and thickness exist for gate injection, due to the amorphous structure of the TiO_2, nevertheless, after normalizing to thickness and area, a lowering of the leakage current under substrate injection is observed, as seen in Fig. 5c. On the other hand, Fig. 5b shows that, after passivation with SiO_x, the current under substrate injection decreases slightly compared to the as-prepared samples, due to less interfacial states and the formation of an interfacial layer between silicon and TiO_2, as to the widening of the effective bandgap of the TiO_2 layer.

Gate current density versus electric field (J–E) characteristics are shown in Fig. 5c, d after normalizing the former Ig–Vg data to device area and gate oxide thickness respectively. As seen, when the oxide thickness decreases, the gate current density also decreases, this effect is caused by a widening of the effective bandgap of the TiO_2 [22–24], thus resulting in a larger barrier height and its more evident in the passivated devices due to the interfacial layer, which effectively decreases the barrier height associated to each device. Also, from Fig. 5b, d, it is observed that passivation of the bare silicon results in a reduction of the contact resistance, via a fermi level depinning [25, 26], except for the 6 nm device, which could be explained by a failed passivation or a poor nucleation of the TiO_2, allowing us to make a correlation between material properties and electrical characteristics [27–29].

C–V measurements were performed in all devices, and, even though the dielectric constant could be not be extracted due to a high leakage current of all devices, flat band voltage could be obtained, as seen in Fig. 6. The flat band voltages for the as-prepared MIS devices are: 10 nm = 0.15 V, 6 nm = 0.26 V, 4 nm = 0.08 V and

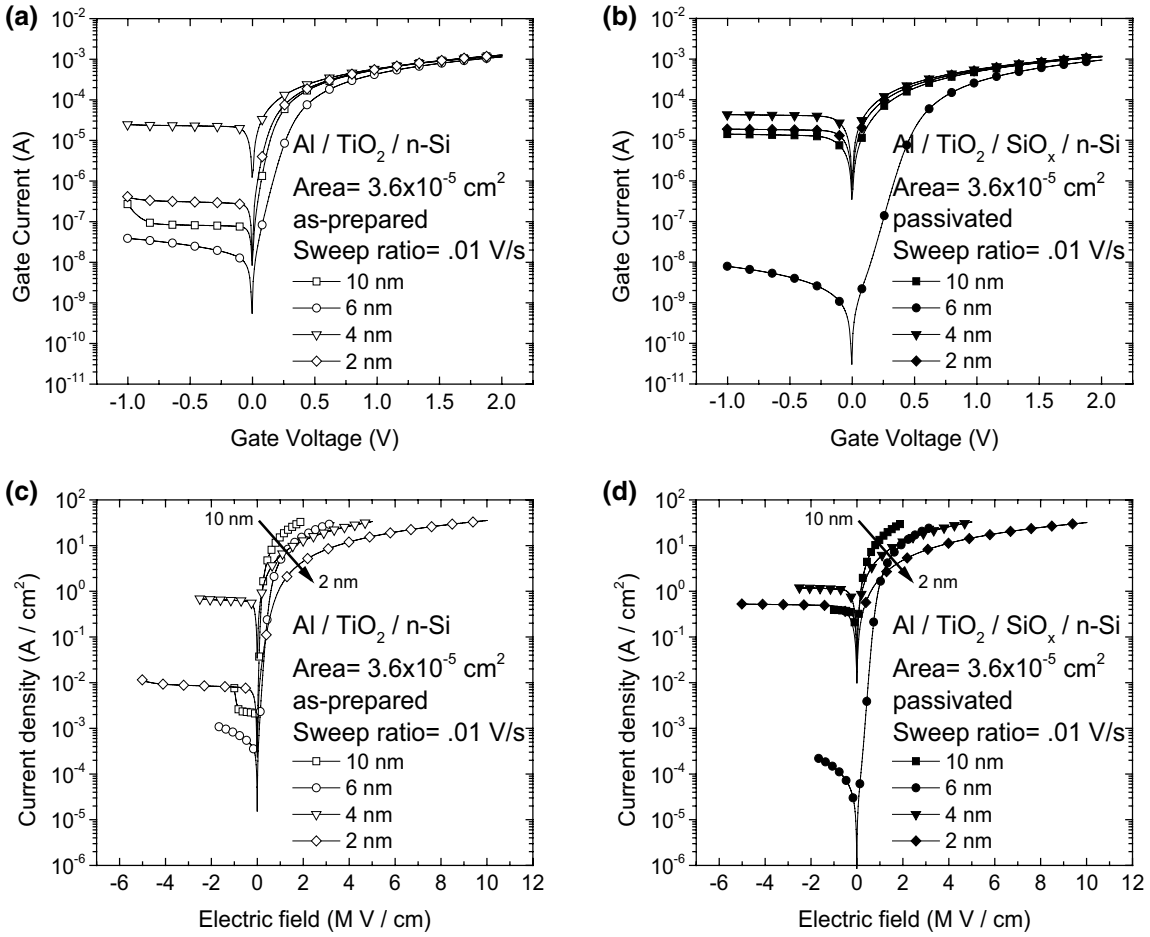

Fig. 5 **a** Ig–Vg characteristics for the as-prepared MIS devices using ultra-thin TiO_2 as gate oxide with $th_{ox} = 10$, 6, 4 and 2 nm. **b** Ig–Vg characteristics for the passivated MIS devices using ultra-thin TiO_2 as gate oxide with $th_{ox} = 10$, 6, 4 and 2 nm. **c, d** J–E characteristics of MIS devices, after normalizing the former Ig–Vg data to device area and oxide thickness respectively. At least 10–15 MIS devices for each condition (oxide thickness, passivated) were measured in order to ensure reproducibility

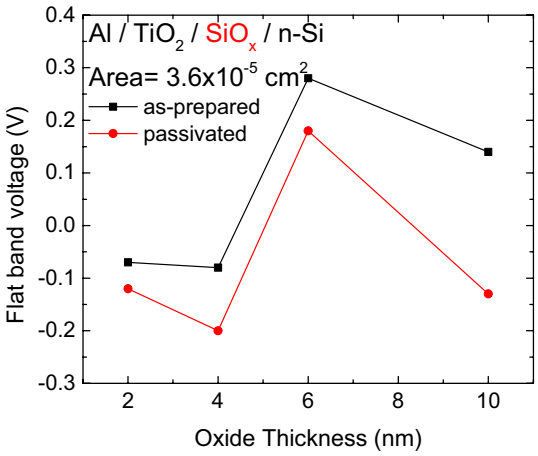

Fig. 6 Flat band voltage of MIS devices. The passivation of the interface using SiO_x results in change to the left of the flat band voltage, thus the SiO_x is inducing a positive charge in the interface

2 nm = 0.06 V, which is expected due to the band alignment between the silicon and the aluminium. Meanwhile, the flat band voltages for the passivated devices are: 10 nm = −0.13 V, 6 nm = 0.18 V, 4 nm = −0.20 V and 2 nm = −0.12 V. This reduction in the value of Vfb for the passivated Al/TiO_2/SiO_x/n-Si structures is associated to the dipole formation near the TiO_2/SiO_x interface. Because TiO_2 presents a high concentration of oxygen vacancies, the difference in the oxygen density for TiO_2 and the SiO_x could promote dipole formation in this interface when charged oxygen vacancies migrate from the region of higher oxygen density towards the region of lower oxygen density [30–33] thus reducing the flat band voltage. The passivation with SiO_x is also reducing the dangling bonds in the interface between insulator and semiconductor.

Ig–Vg–T (from 300 to 355 K) measurements were performed in order to accurately obtain the conduction mechanisms that could best fit the experimental data. Poole–Frenkel emission was evaluated and found out to be impossible due to a nonexistent energy trap level obtained. Afterwards, Schottky emission was fitted as seen in Fig. 7a, b and resulted to be the main conduction mechanism for these devices; as seen, there exist a point in which MIS devices are not affected by temperature, which is also consistent with Schottky emission [34, 35]. Furthermore, after this temperature independent point, the tendency of the leakage current shifts, resulting in a lower leakage current for higher temperatures, which can be explained by generation of electron–holes pairs created by temperature, resulting in recombination centers, thus lowering the overall leakage current. From this conduction mechanism the Schottky barrier height was obtained for the as-prepared MIS devices (Fig. 7a, b) and found to be 0.253 eV for the 10 nm, 0.265 eV for the 6 nm, 0.284 eV for the 4 nm, and 0.297 eV for the 2 nm, which is consistent with the lowering of the current density as the oxide thickness decreases. For the passivated devices, the Schottky barrier height was 0.255 eV for the 10 nm, 0.272 eV for 6 nm, 0.291 eV for 4 nm and 0.312 eV for the 2 nm. This is also consistent with the increased barrier height due to an interfacial SiO_x layer for the passivated devices under substrate injection.

After extracting physical parameters from experimental data, the semi-empirical conduction models (Eqs. 1, 2) and the models for gate leakage current provided in standard CAD tools, can be simulated and compared to our

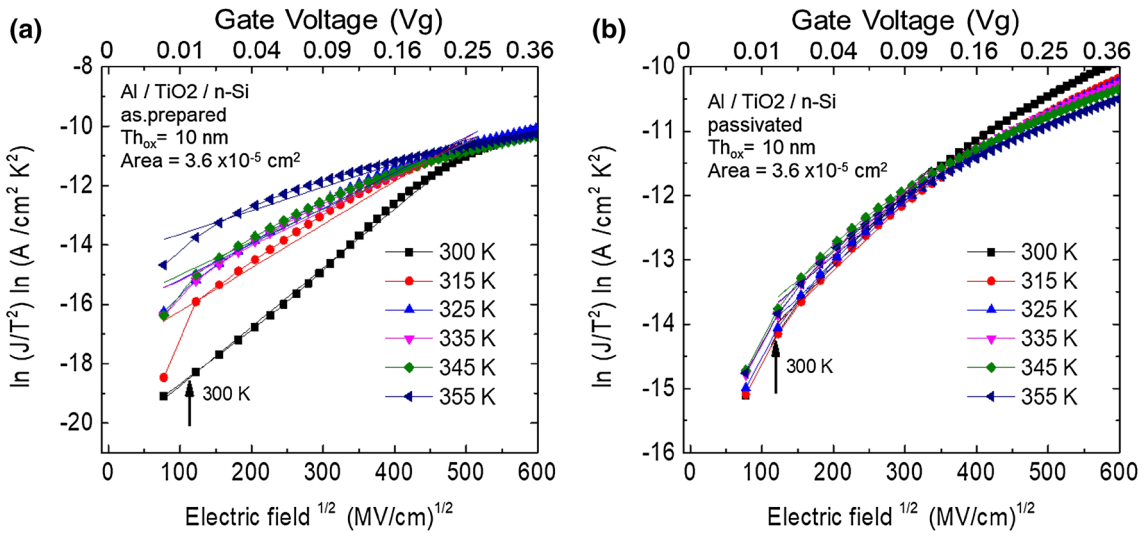

Fig. 7 Fitting of experimental Ig–Vg-T data of MIS devices (TiO_2 = 10 nm in thickness) to the Schottky emission model for the **a** as-prepared and **b** passivated. In both cases, Φ_B and Ɛr are extracted

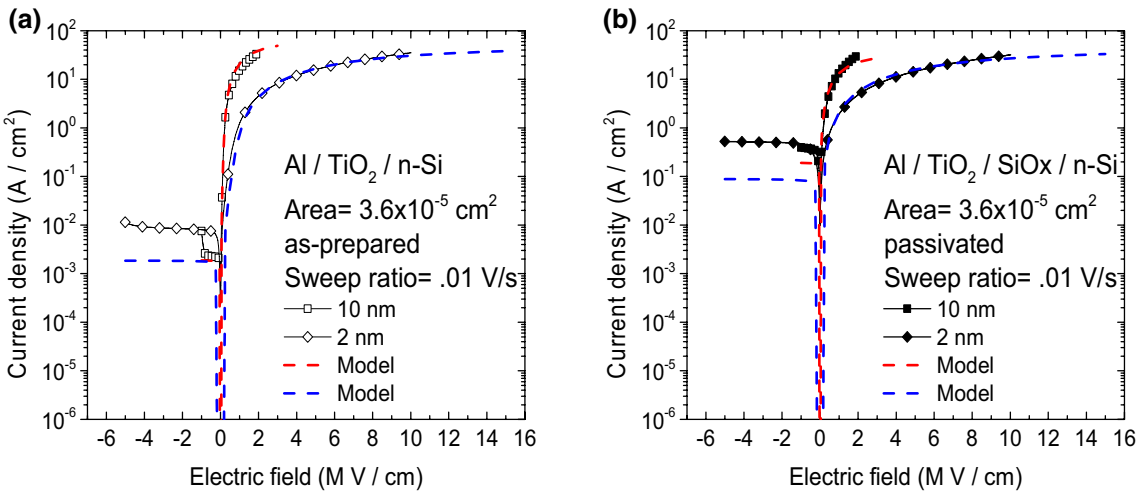

Fig. 8 Comparison between experimental Ig–Vg data, semi-empirical models (using MATLAB for the models already described in Eq. 1) and CAD simulations (using standard conduction models from SILVACO) for TiO_2-based MIS devices with **a** as prepared TiO_2 devices **b** passivated samples. For all conditions, an excellent fitting of the simulated and experimental data is observed

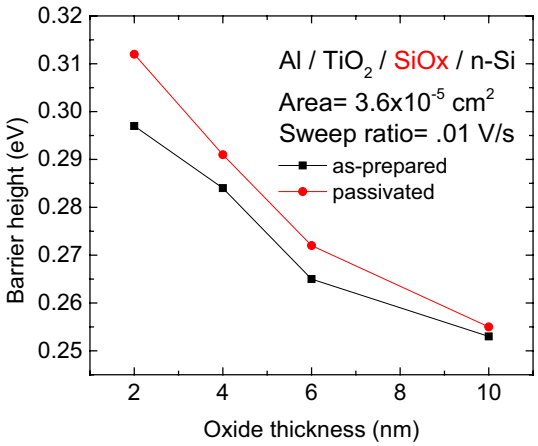

Fig. 9 Oxide thickness for the fabricated MIS devices. An almost linear relation between barrier height and oxide thickness is observed

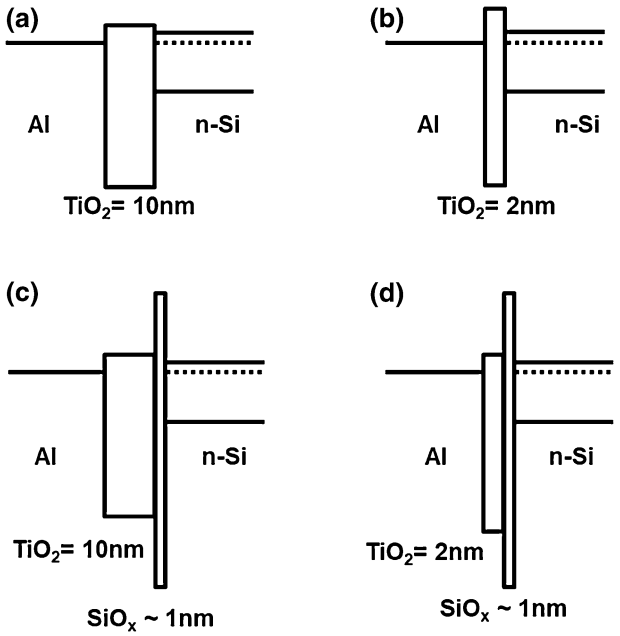

Fig. 10 Ideal energy band diagrams (thermal equilibrium) for MIS devices in the **a** 10 nm as-prepared, **b** 2 nm as prepared, **c** 10 nm passivated condition and **d** 2 nm passivated condition. A widening of the bandgap is observed as the oxide thickness decreases

experimental Ig–Vg data in order to validate the formerly fitted conduction mechanism. Using MATLAB and SILVACO, Schottky emission was further validated and fitted with excellent agreement with experimental data as seen in Fig. 8a, b. Also, it is seen that if the experimental measurements continue, the model will still be fitted for higher electric fields.

Figure 9 shows the change in the Schottky barrier height for different thicknesses and as seen, the relation is almost linear, which could be adjusted in case of even thinner dielectrics and/or when a passivation with SiO_x is performed, which is very important since the barrier height could be tuned according to application.

Figure 10a–d show the ideal energy band diagrams for as-prepared and passivated Al/TiO_2/n-Si samples respectively (thermal equilibrium). After passivation, an interfacial lower k-IL between TiO_2 and silicon is obtained, which reduces the dangling bonds and lowers the effective gate leakage current. Also, when the oxide thickness is reduced, a widening of the TiO_2 bandgap occurs, thus having a larger Schottky barrier height resulting in less leakage current.

Table 1 shows the parameters extracted from experimental data, as from MATLAB and SILVACO simulations.

Table 1 Summary of the parameters extracted from experimental data, semi empirical models and simulations

Parameter	TiO_2 10 nm	TiO_2/SiO_x 10 nm	TiO_2 6 nm	TiO_2/SiO_x 6 nm	TiO_2 4 nm	TiO_2/SiO_x 4 nm	TiO_2 2 nm	TiO_2/SiO_x 2 nm
Schottky barrier, Φ_B (eV)	0.253	0.255	0.265	0.272	0.284	0.291	0.297	0.312
Optical dielectric constant, ε_r	5.1	4.9	4.8	4.6	4.7	4.6	4.6	4.5
Effective mass (m_0/m)	0.37	0.37	0.37	0.37	0.37	0.37	0.37	0.37

These parameters have excellent agreement with previously reported values for amorphous TiO_2 [35–38].

6 Summary and conclusions

Schottky emission was found to be the main CM for the fabricated MIS devices using amorphous TiO_2 as gate dielectric with different thicknesses (10, 6, 4, and 2 nm); furthermore, this CM remains the same even after passivation of the interface between insulator and semiconductor using SiO_x. From this analysis important physical parameters such as the effective mass (m*), barrier height (Φ_B) and the optical dielectric constant ($\boldsymbol{\varepsilon_r}$) were extracted and compared to semi empirical models, having excellent agreement with reported amorphous TiO_2 values. When the samples were passivated, a shift to the left in the flat band voltage is observed and is consistent with a positive charge in SiO_x, this passivation reduces the interface charges of the fabricated MIS devices and reduces the gate current density when substrate injection is applied. The accurate identification of CM for the gate leakage current in MIS devices allows for better reliability predictions before failure of these devices.

Acknowledgements This work was fully supported by the Mexican Council for Science and Technology (CONACYT-Mexico).

References

1. X. Chen, S.S. Mao, Chem. Rev. **107**, 2891–2959 (2007)
2. M. Landmann, E. Rauls, W.G. Schmidt, J. Phys. **24**, 195503 (2012)
3. C. Di Valentin, G. Pacchioni, A. Selloni, Phys. Rev. B **70**, 085116 (2004)
4. D.O. Scanlon, C.W. Dunnill, J. Buckeridge, S.A. Shevlin, A.J. Logsdail, S.M. Woodley, C.R.A. Catlow,.M.J. Powell, R.G. Palgrave, I.P. Parkin, G.W. Watson, T.W. Keal, P. Sherwood, A. Walsh, A.A. Sokol, Nat. Mater. **12**, 798–801 (2013)
5. R. Hengerer, B. Bolliger, M. Erbudak, M. Grätzel, Surf. Sci. **460**, 1–3 (2000)
6. M. Buchalska, M. Kobielusz, A. Matuszek, M. Pacia, S. Wojtyła, W. Macyk, ACS Catal. **5**(12), 7424–7431 (2015)
7. E.B. Kandemir, B. Gonul, G.T. Barkema, K.M. Yu, W. Walukiewicz, L.W. Wang, Comput. Mater. Sci. **82**, 100–106 (2014)
8. H.Z. Zhang, B. Chen, J.F. Banfield, G.A. Waychunas, Phys. Rev. B **78**, 214106 (2008)
9. H.H. Pham, L.-W. Wang, Phys. Chem. Chem. Phys. **17**, 541 (2015)
10. A.N. Murashkevich, A.S. Lavistkaya, T.I. Barannikova, I.M. Zharskii, J. Appl. Spectrosc. **75**(5), 730 (2008)
11. W.L. Scopel, Braz. J. Phys. **32** (2002)
12. A.C. Bronneberg, C. Höhn, R. van de Krol, J. Phys. Chem. C **121**, 5531–5538 (2017)
13. R. Methaapanon, S.F. Bent, J. Phys. Chem. C **114**, 10498–10504 (2010)
14. M. Reiners, K. Xu, N. Aslam, A. Devi, R. Waser, S. Hoffmann-Eifert, Mater. Des. **120**, 99–108 (2017)
15. G.T. Lim, D.-H. Kim, Thin Solid Films **498**, 254–258 (2006)
16. B. Abendroth, T. Moebus, S. Rentrop, R. Strohmeyer, M. Vinnichenko, T. Weling, H. Stöcker, D. Meyer, Thin Solid Films **545**, 176–182 (2013)
17. G. He, Z. Sun, *High-k Gate Dielectrics for CMOS Technology* (Wiley, Weinheim, 2012)
18. J.C. Ranuárez, M.J. Deen, C.H. Chen, Microelectron. Reliab. **46**, 1939–1956 (2006)
19. B.L. Yang, P.T. Lai, H. Wong, Microelectron. Reliab. **44**, 709–718 (2004)
20. F.C. Chiu, Adv. Mater. Sci. Eng. **2014** (2014)
21. S. Ganichev, E. Ziemann, W. Prettl, I. Yassievich, A. Istratov, E. Weber, Phys. Rev. B **61**, 10361 (2000)
22. S. Zhuiykov, M. Karbalaei, A. Zhenyin, C. Xue, H. Xu, L. Hyde, Mater. Des. **120**, 99–108 (2017)
23. D. Wei, T. Hossain, N.Y. Garces, N. Nepal, H.M. Meyer III, M.J. Kirkham, C.R. Eddy Jr., J.H. Edgar, ECS J. Solid State Sci. Technol. **2**(5), 110–114 (2013)
24. S. Duenas, H. Castan, H. García, E. San Andres, M. Toledano-Luque, I. Martil, G. Gonzalez-Díaz, K. Kukli, T. Uustare, J. Aarik, Semicond. Sci. Technol. **20**, 1044–1051 (2005)
25. W. Park, Y. Kim, S.K. Lee, U. Jung, J.H. Yang, C. Cho, Y.J. Kim, S.K. Lim, I.S. Hwang, H.-B.-R. Lee, B.H. Lee, Electron Devices Meeting (IEDM), IEEE International, (2014)
26. A. Agrawal, J. Lin, M. Barth, R. White, B. Zheng, S. Chopra, S. Gupta, K. Wang, J. Gelatos, S.E. Mohney, S. Datta, Appl. Phys. Lett. **104**, 112101 (2014)
27. S. Akin, S. Sönmezoğlu, Metall. Mater. Trans. A **46**, 4150–4159 (2015)
28. S. Akın, F. Özel, M. Kuş, S. Sönmezoğlu, Phil. Mag. **94**(23), 2678–2691 (2014)
29. S. Sönmezoğlu, Curr. Nanosci. **9**, 39–45 (2013)
30. K. Kita, A. Toriumi, Appl. Phys. Lett. **94**, 132902 (2009)
31. K. Iwamoto, Y. Kamimuta, A. Ogawa, Y. Watanabe, S. Migita, W. Mizubayashi, Y. Morita, M. Takahashi, H. Ota, T. Nabatame, A. Toriumi, Appl. Phys. Lett. **92**, 132907 (2008)
32. X. Wang, K. Han, W. Wang, S. Chen, X. Ma, D. Chen, J. Zhang, J. Du, Y. Xiong, A. Huang, Appl. Phys. Lett. **96**, 152907 (2010)
33. L.Q. Zhu, K. Kita, T. Nishimura, K. Nagashio, S.K. Wang, A. Toriumi, Jpn. J. Appl. Phys. **50**, 031502 (2011)
34. S.B. K Aydin, D.I. Yildiz, H.I. Kanbur, R. Shaningoz, Bull. Mater. Sci. **37**(7), 1563–1568 (2014)

35. Z. Yuan, A. Nainani, Y. Sun, J.-Y. Jason Lin, P. Pianetta, K.C. Saraswat, Appl. Phys. Lett. **98**, 172106 (2011)
36. M.K. Bera, C.K. Maiti, Mater. Sci. Semicond. Process. **9**, 909–917 (2006)
37. A. Wypych, I. Bobowska, M. Tracz, A. Opasinska, S. Kadlubowski, A. Krzywania-Kaliszewska, J. Grobelny, P. Wojciechowski, J. Nanomater., **124814** (2014)
38. V.M. Kalygina, I.S. Egorova, I.A. Prudaev, O.P. Tolbanov, V.V. Atuchin, Chin. J. Physiol. **55**, 59–63 (2017)