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Electrical and impedance properties of MPS structure based on (Cu_2O–CuO–PVA) interfacial layer

A. Buyukbas-Uluşan[1] · S. Altındal Yerişkin[2] · A. Tataroğlu[1] · M. Balbaşı[2] · Y. Azizian Kalandaragh[3,4]

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Abstract
In this study, the electrical characteristics of the prepared Au/(Cu_2O–CuO–PVA)/n-Si (MPS) structures have been investigated in detail by using the frequency dependent C–V and G/ω–V measurements by taking into account the interfacial polymer layer, surface states (N_{ss}), polarization and series resistance (R_s). The electric parameters such as the diffusion potential (V_D), the concentration of donor atoms (N_D), and barrier height (BH) values were obtained from C^{-2}–V plots for each frequency and they were found as 0.33 eV, $7.60\times10^{13}cm^{-3}$, 0.65 eV at 10 kHz and 0.70 eV, $6.99\times10^{13}cm^{-3}$, 1.02 eV at 3 MHz. The energy dependent profiles of N_{ss} and their relaxation time (τ) were found by using admittance method and they ranged from 1.09×10^{11} to 1.60×10^{11} eV^{-1} cm^{-2} and 7.75×10^{-6} to 9.93×10^{-5} s, respectively. These low values of N_{ss} are indicated that the (Cu_2O–CuO)-doped PVA interfacial layer considerably enhances the performance of the Au/n-Si (MS) structure and so it can be successfully utilized instead of the traditional insulator/dielectric layer due to its passivized the surface states. The R_s versus V plot was obtained from the C–V and G/ω–V data using Nicollian and Brews method and it shows a distinctive peak, while the magnitude of the peak decreases with increasing frequency, its position shift towards lower or negative bias voltage with decreasing frequency due to the reordering and restructuring of surface states and their relaxation time under applied bias voltage. The impedance measurements were also performed in the wide range of frequency (100 Hz–1 MHz) at room temperature. The equivalent circuit model parameters such as parallel resistor (R_p), capacitor (C_p) and a series resistance (R_s) were calculated from Cole–Cole plots. The values of R_s, R_p and C_p decrease with increases dc voltage. The decrease of R_p is because of the increasing in the number of injected charge carriers into the device.

1 Introduction

In recent years, due to the technological importance of the organic/polymeric materials play an important role in electronic and optoelectronic device applications such as Schottky type diode, solar cells, light-emitting diodes, transistors, sensors and capacitors [1–6]. In order to improve the performance and reliability of metal-semiconductor (MS) type Schottky barrier diodes (SBDs), a thin polymer layer with and without metal doped are inserted between metal and semiconductor instead of traditional insulator materials such as SiO_2 and SnO_2. Although SiO_2 is a good gate dielectric thanks to its compatibility with Si wafer, it may be unsatisfying to restrain unacceptably large leakage current and high N_{ss}. It is believed that the use of high-dielectric interfacial layer and both its thickness and homogeneity play an important role in reviewing the performance, reliability and stability of these devices. Therefore, to perform a high quality SBDs with a thin interlayer, low ideality factor, low surface states (N_{ss}), high or moderate BH and its homogeneity are critical parameters. In other words, this drawback can be overcome through usage of the other interlayers instead of insulator layer.

The impedance-voltage (Z^*–V) measurements which are including capacitance/conductance–voltage (C/G–V) characteristics of these devices are independent of frequency, but the situation is quite different in applications due to the polarization processes, N_{ss}, series resistance (R_s) of the device, native or deposited interfacial layer, the level

✉ A. Buyukbas-Uluşan
aysel.buyukbas@gmail.com

1 Physics Department, Faculty of Sciences, Gazi University, Ankara, Turkey

2 Department of Chemical Engineering, Faculty of Engineering, Gazi University, Ankara, Turkey

3 Physics Department, Faculty of Sciences, University of Mohaghegh Ardabili, Ardabil, Iran

4 Engineering Sciences Department, Sabalan University of Advanced Technologies, Namin, Iran

of doping concentration atoms, the nature of barrier height (BH) at M/S interface. Therefore, the investigation of the forward and reverse C–V and G/ω–V characteristics of these electronic devices measured only at one frequency and voltage cannot supply enough information both on the electric and dielectric properties of these devices. For these reasons, the C–V and G/ω–V measurements of these devices in the wide range of frequency and voltage are more important study to get both the fabrication of high-performance and obtain knowledge on the conduction mechanism in these devices. Usually, metal-polymer-semiconductor (MPS) structure shows similar behavior of metal-insulator-semiconductor (MIS) type Schottky diodes. Especially, polyvinyl alcohol (PVA) has an important place among organics/polymers and it has low cost, low weight, flexible and easy fabrication processes such as electrostatic spraying, electrochemical deposition, sol–gel, dip coating, and spin coating [1–4]. PVA is also water soluble and it has a semi-crystalline polymer exhibit more important applications due to the role of OH group and hydrogen bonds [4]. On the other hand, PVA has normally poor electrical conductivity and may be conductive upon doping with some dopants such as Zn, Ni, Co, graphene, (Cu_2O–CuO) due to the high physical interaction between polymer chains [5, 6].

There are many workers in the literature on the characterization of N_{ss} and R_s [7, 8]. Among them admittance method or impedance (Y = 1/Z) method has been described and analyzed by Nicollian and Goetzberger [9] which can supply more reliable and accurate results. The existence of N_{ss} and R_s in MIS/MOS and MPS type structures can be affected the C–V and G/ω–V characteristics. Because, at low and moderate frequency the charges at surface states/traps can easy follow the ac signal and yield an excess capacitance and conductance to real values of them. Surface states have an energy distribution within the band-gap and even extend into the conduction and valence band of the semiconductor. Conductance method can not only extract the values of N_{ss} in both the depletion and weak inversion region, and relaxation time (τ) of them. This conductance method is based on measuring a set of C_m and G_m of the MIS or MPS type structure both as a function of frequency and bias voltage and subsequently calculating the parallel conductance (G_p/ω) by solving the small signal equivalent circuit. Parallel conductance represents the loss mechanism occurring when the surface states/traps capture and emit carriers, and is used to extract the density of N_{ss}.

In our previous study [10], the conduction mechanisms of the fabricated Au/(Cu_2O–CuO–PVA)/n-Si (MPS) structures have been investigated by using the current–voltage (I–V) characteristics in the wide range of temperature (100–380 K) and voltage (±5 V). The forward bias I–V–T characteristics of the Au/(Cu_2O–CuO–PVA)/n-Si (MPS) structures were successfully described by the double-GD of BHs with mean BHs. Therefore, in the present study, we aimed that an achieve good understand effects of N_{ss}, R_s, (Cu_2O–CuO–PVA) polymer layer and polarization. For this purpose, the forward and reverse bias C–V and G/ω–V measurements were carried out in the wide range of frequency (10 kHz–3 MHz) and voltage (±4V) at room temperature.

2 Experimental details

The Au/(CuO–Cu_2O–PVA)/n-Si (MPS) type SBDs were fabricated on P-doped (n-Si) single crystalline Si wafer with (100) orientation, with approximately 300 µm thick and 0.2 Ohm cm resistivity. More information on the cleaning processes, structural analysis and schematic diagram of structures system can be seen in our previous study [10]. The admittance measurements in this study were carried out by using a HP 4192A LF Impedance analyzer at room temperature. The forward and reverse bias C–V and G/ω–V measurements were carried out in the wide range of frequency (10 kHz–3 MHz) and voltage (±4 V) by 50 mV steps. In addition, the impedance measurements were performed using a Solartron SI1260 Impedance/Gain-Phase Analyzer and Solartron 1296 Dielectric Interface at room temperature.

3 Result and discussion

3.1 Frequency dependent electrical properties

The C–V and G/ω–V characteristics of the Au/(Cu_2O–CuO–PVA)/n-Si (MPS) structure for various frequency at room temperature were given in Figs. 1 and 2, respectively. In order to see the effects of interfacial layer, surface states and R_s of the structure, these measurements

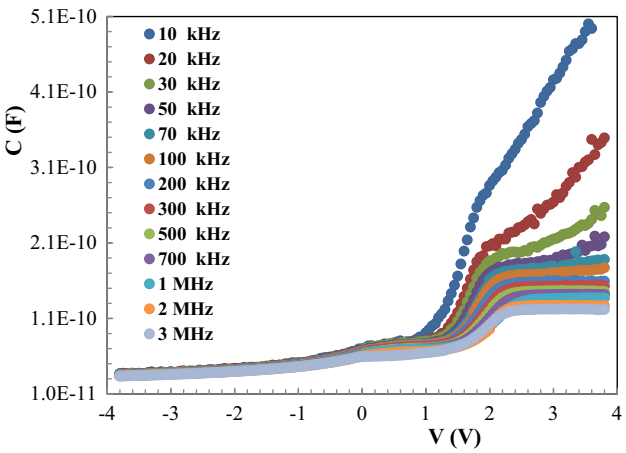

Fig. 1 C–V plot of the Au/(Cu_2O–CuO–PVA)/n-Si (MPS) structure for various frequencies

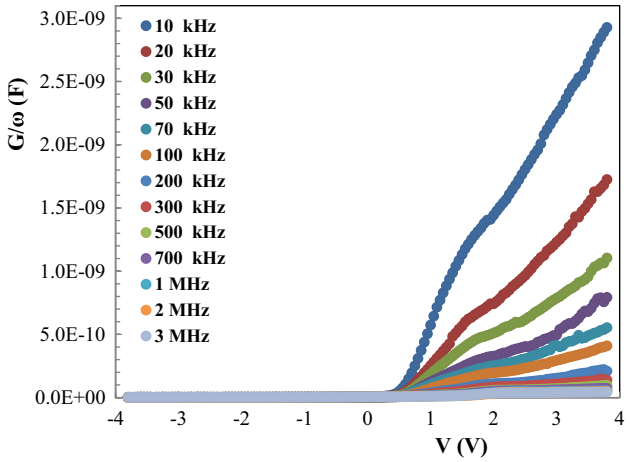

Fig. 2 G/ω–V plot of the Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structure for various frequencies

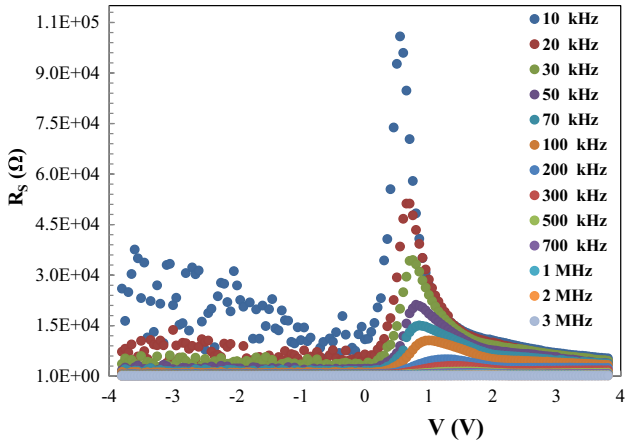

Fig. 3 R_s–V plot of the Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structure for various frequencies

were performed in the frequency range of 10 kHz–3 MHz at ±4V. As can be clearly seen in Figs. 1 and 2, both the C–V and G/ω–V curves have inversion, depletion and accumulation regions like a metal–oxide–semiconductor (MOS) capacitor and they show some discrepancies especially in the depletion and accumulation regions which are routed from the surface states the existence of N_{ss}, R_s, polarization and interfacial polymer layer. However, an interfacial polymer or insulator layer between metal and semiconductor can be easy polarized under an external electric field that displaces the charges from their equilibrium position. The life time of charges at surface states and both the interfacial layer and the formation of BH at M/S interface are also more effective on the impedance measurements. As shown in Figs. 1 and 2, both the values of C and G/ω increase with increase voltage and decrease with increased frequency both in depletion and accumulation regions. Such behavior of them in depletion region especially at low frequencies can be attributed to the existence of N_{ss} and surface polarization, but at accumulation regions especially due to the effects of R_s and interfacial polymer layer, respectively. On the other hand, the decreases with increasing frequency of them especially in the depletion region is the result of the interface states cannot follow the a.c. signal at higher frequency and so that they cannot yield any contribution or excess values of the measurements of them [11–14].

existence of R_s can also cause a serious error in the extraction of the electrical parameters. While the N_{ss} are more effective at low frequency, but R_s is effective at high frequency. To avoid from this error and the sensitivity limitation, R_s can be minimized by (a) the fabrication process of the sample (b) performing these measurements at low frequency and (c) measuring R_s and applying a correction/adjustment. According to the Nicollian and Brews [7] method, the real value of R_s can be calculated from the measurements of the C_{ma} and G_{ma} values at strong accumulation region at enough high frequencies (f≥500 kHz). However, the voltage dependence profile of R_s can be also extracted from the measured any C_m and G_m for each frequency and voltage. Therefore, the R_s versus V plot was obtained by using the fallowing equation formalized by Nicollian and Brews [7].

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \left(\omega C_{ma}\right)^2}. \tag{1}$$

Thus, R_s versus V plot for each frequency was given in Fig. 3. It is clear that the value of R_s at strong accumulation region at high frequencies become almost constant or independent from voltage and so this value is corresponding to the real value of R_s, but it becomes increases with decreasing frequency at low frequencies due to the effects of R_s and surface polarization. On the other hand the R_s versus V plot has one distinctive peak especially at low frequencies. While the magnitude of the peak decreases with increasing frequency, its position shift towards lower or negative bias voltage with decreasing frequency. Such behavior of it with frequency is the result of reordering and restructuring of surface states under electric field [13–15].

In order to extract some main parameters of the Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structure such as diffusion potential (V_D), doping concentration atoms (N_D) and barrier height [$\Phi_{B(C-V)}$], the reverse bias C^{-2} versus V plot was drawn for the whole measured frequency range and is given in Fig. 4. In MIS/MOS and MPS structures, the depletion layer capacitance per unit area can be expressed as [8]:

$$C^{-2} = 2\left(V_o + V_R\right)/\left(q\varepsilon_s\varepsilon_o A^2 N_D\right), \tag{2}$$

$$\tan\theta = d\left(C^{-2}\right)/dV_R = 2/\left(q\varepsilon_s\varepsilon_o A^2 N_D\right). \tag{3}$$

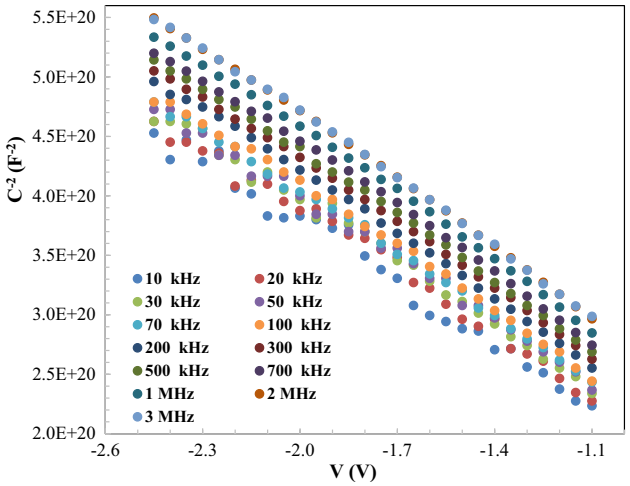

Fig. 4 C^{-2}–V plot of the Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structure for various frequencies

Table 1 The values of various parameters for Au/(Cu_2O–CuO–PVA)/n-Si (MPS) structure obtained from C^{-2}–V plots

f (kHz)	V_o (V)	V_D (eV)	N_D ($\times 10^{13}$) (cm^{-3})	$\Phi_{B(C-V)}$ (eV)
10	0.30	0.33	7.60	0.65
20	0.34	0.37	7.57	0.69
30	0.38	0.41	7.53	0.73
50	0.40	0.43	7.49	0.75
70	0.43	0.46	7.44	0.78
100	0.46	0.49	7.41	0.81
200	0.50	0.53	7.31	0.85
300	0.53	0.56	7.26	0.88
500	0.57	0.60	7.22	0.92
700	0.61	0.64	7.16	0.96
1000	0.63	0.66	7.11	0.98
2000	0.65	0.68	7.04	1.00
3000	0.67	0.70	6.99	1.02

In Eq. 2, ε_s is the dielectric constant of the semiconductor (11.9 for Si), A is the area of rectifier contact and other quantities are well known in the literature. The values of V_D ($= V_o + kT/q$) and N_D are usually calculated the intercept and slope of the linear part C^{-2} versus V plot, respectively. In this way, the value of $\Phi_{B\,(C-V)}$ is calculated by the following equations [8].

$$\Phi_{B(C-V)} = V_D + \frac{kT}{q} Ln\left(\frac{N_C}{N_D}\right) - \Delta\Phi_B = V_D + E_F - \Delta\Phi_B, \tag{4}$$

With

$$\Delta\Phi_b = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_o}\right]^{1/2} \text{and } E_m = \left[\frac{2qN_DV_O}{\varepsilon_s\varepsilon_o}\right]^{1/2}. \tag{5}$$

Here, E_m is the maximum electric field, N_c is the density of states at the conduction-band and E_F is the energy different between the bulk Fermi level and valance band edge and $\Delta\Phi_B$ is the image force barrier lowering. The calculated experimental values of V_D, N_D and $\Phi_{B(C-V)}$ for various frequencies at room temperature are tabulated in Table 1. As can be seen from Table 1, the values of V_D, N_D and $\Phi_{B(C-V)}$ are found as 0.33 eV, $7.60\times10^{13}cm^{-3}$, 0.65 eV at 10 kHz and 0.70 eV, $6.99\times10^{13}cm^{-3}$, 1.02 eV at 3 MHz. It is clear that all of these electric parameters are a strong function of frequency. As shown in Fig. 5, while the value of $\Phi_{B(C-V)}$ increases almost as exponentially, N_D decreases. Such behavior of $\Phi_{B(C-V)}$ and N_D with frequency is the effects of N_{ss} and polarization [16–18].

The obtained experimental high values of N_D and R_s at low frequencies can be attributed to the existence of surface states and dislocation located between interfacial layer and semiconductor. While the contribution of C and G by surface states is very important especially at low frequencies, the value of R_s becomes very effective at high frequency at accumulation region (Fig. 6). As shown in Fig. 6, the value of R_s decreases with the increasing applied bias voltage for each frequency. As the frequency is increased further, the value of R_s remains almost constant such that this value at strong accumulation region corresponds to the real value of R_s. Therefore, both the existence of the interfacial layer native or deposited, N_{ss} and R_s must be taken into account in the calculations [14–19].

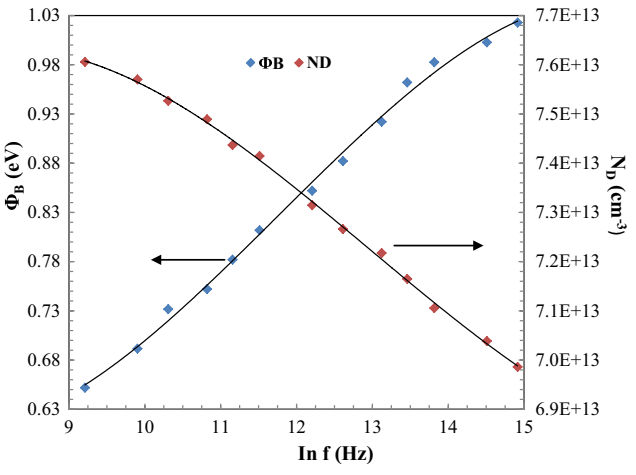

Fig. 5 Φ_B-Inf and N_D-Inf plot of the Au/(Cu_2O–CuO–PVA)/n-Si (MPS) structure

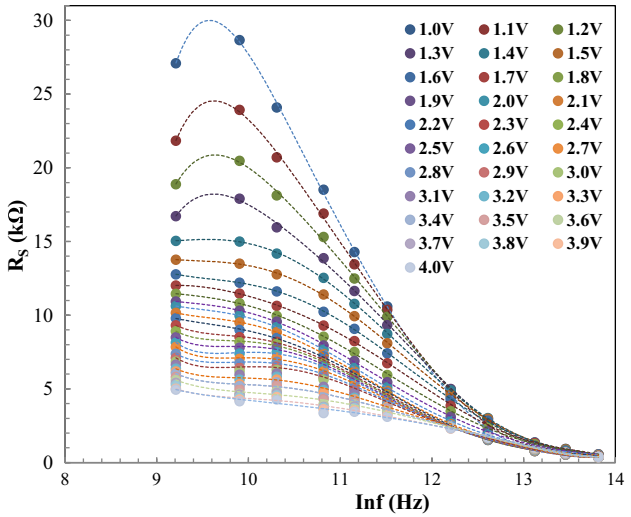

Fig. 6 R_s-Inf plot of the Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structure for various voltage

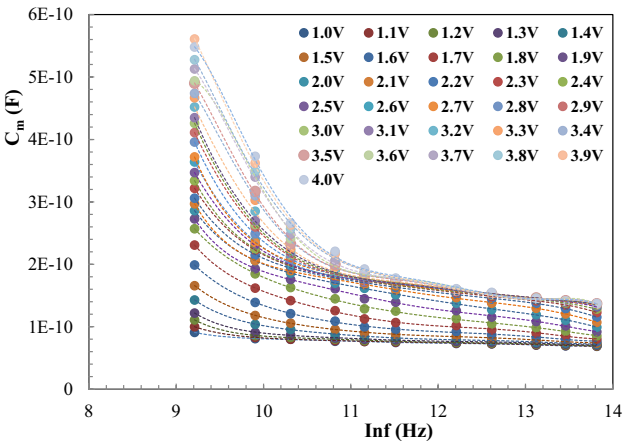

Fig. 7 C_m-Inf plot of the Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structure for various voltage

3.2 The extraction of energy dependent profile of surface states

There are many studies have suggested different ways of the characterization of surfaces states/traps (N_{ss}) [7–9]. Among them the one of the most useful methods to determine of them is the conductance method. This method is defined by Nicollian and Brews and they have observed that the values of C and G/ω decreased with increasing frequency, especially at low and moderate frequencies. According to this method, the value of parallel conductance can be expressed as [8]:

$$G_p/\omega = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2\left(C_{ox} - C_m\right)^2} = \frac{qN_{SS}}{2\omega\tau}\ln\left(1+\omega^2\tau^2\right). \quad (6)$$

In Eq. 6, τ is the life time or relaxation time of the surface states and C_{ox} is the interfacial layer capacitance. The G_p/ω versus Inf plots were calculated from the use of C_m and G_m values in the wide range of applied bias voltage (1–4 V) at room temperature. Firstly, both the C_m and G_m/ω versus Inf plots were drawn and given in Figs. 7 and 8, respectively. As shown Figs. 7 and 8, both C_m and G_m/ω values increase with increasing voltage but decrease with increasing frequencies as almost exponentially and then they remain almost constant at high frequencies [20–25].

It is clear that, the changes in the C and G is considerably high in the depletion region when compared accumulation region. In other words, while N_{ss} are effective especially in the depletion region at low and moderate frequencies, R_s becomes effective only at accumulation region at high frequencies. The higher values of C and G/ω at low frequency are due to the excess capacitance and conductance (C_{ex} and G_{ex}/ω) steam from the N_{ss} which are equilibrium with the semiconductor (di ≥ 30 Å) and they can easy follow the ac signal. Similar results have been reported by Tecimer et al. and Şafak et al. [19, 26, 27]. Figure 9 shows the curves of parallel conductance (G_p/ω) versus Inf of the Au/(Cu_2O–CuO–PVA)/n-Si (MPS) structure at various forward bias voltages. As can be seen in Fig. 9, for each forward bias voltage the G_p/ω versus Inf plot gives a peak and this peak value shifts towards to the accumulation or high forward bias increase with increasing applied bias voltage. Such peak behavior of G_p/ω can be attributed to the existence of N_{ss} and their restructure and reordering under applied bias voltage [9, 25, 26]. The magnitude of peak is dependent on the capture rate, i.e. on the N_{ss} level occupancy and life time of them. At the peak value of G_p/ω, ωτ is corresponding to 1.98

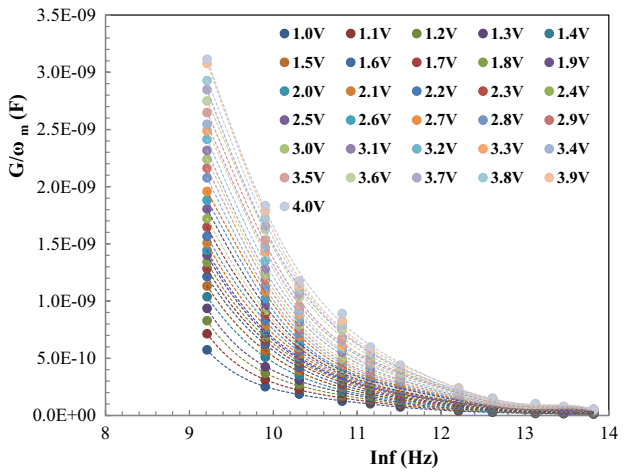

Fig. 8 G_m/ω-Inf plot of the Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structure for various voltage

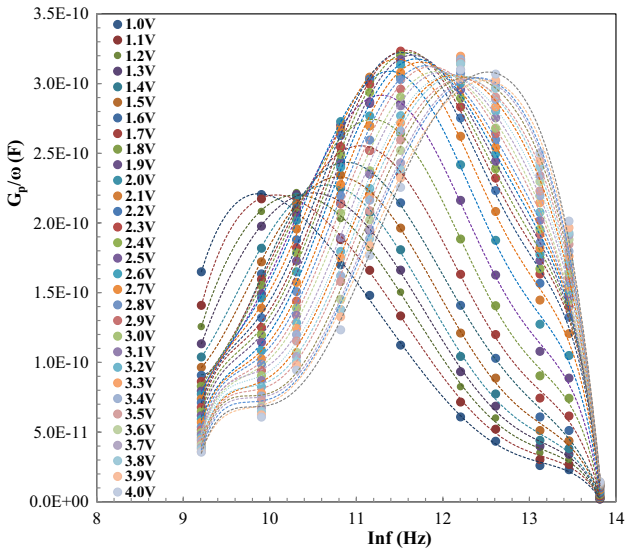

Fig. 9 G_p/ω-Inf plot of the Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structure for various voltage

and substituting this value in Eq. (6), one obtains $N_{SS} = \frac{(G_p/\omega)\max}{0.402qA}$ and life time $\tau = 1.98/\omega_p$, where ω_p is the frequency at the $(G_p/\omega)_{max}$.

The energy distribution of N_{ss} and their relaxation time (τ) are indicated in Fig. 10. As can be seen from Fig. 10, the values of N_{ss} and their relaxation time (τ) ranged from 1.09×10^{11} to 1.60×10^{11} eV^{-1} cm^{-2} and 7.75×10^{-6} to 9.93×10^{-5} s, respectively. Such dispersion in the C–V and G/ω–V characteristics as function of frequency and voltage have been also reported in the literature [28–31] due to the existence of N_{ss}, R_s, and interfacial layer. It is clear that, the obtained values of N_{ss} which are order 10^{11} eV^{-1} cm^{-2} are more suitable for an electronics device. These values of N_{ss} are indicated that

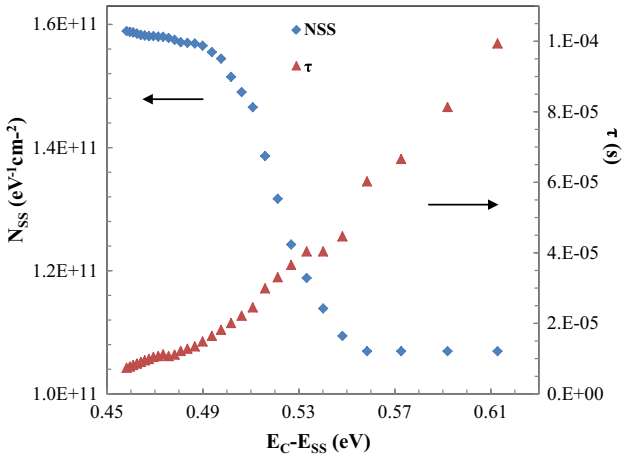

Fig. 10 Energy distribution of N_{ss} and their τ calculated from the experimental G_p/ω versus Inf characteristics

the (Cu_2O–CuO)-doped PVA interfacial layer considerably enhances the performance of the Au/n-Si (MS) structure. Therefore, (Cu_2O–CuO)-doped PVA polymer interfacial layer can be successfully used instead of the traditional insulator/dielectric layer due to its passivized the surface states.

3.3 Impedance properties

The impedance spectroscopy (IS) is a technique used to understand the alternating current (ac) behavior of dielectric materials and electronic devices. This technique enables us to measure the response of the material to a small amplitude excitation over a wide range of frequency. A device with dielectric material can be represented by a parallel RC circuit. The impedance (Z) of RC circuit is expressed by,

$$Z = \frac{1}{Y} = \frac{1}{(1/R) + i\omega C} \tag{7}$$

where Y, R and C are the admittance, resistance and capacitance of device, respectively. The RC circuit can be modeled by an equivalent circuit, as shown in Fig. 11. The equivalent circuit can be considered as a single parallel resistor R_p and capacitor C_p network with a series resistance R_s.

Generally, the complex impedance of the equivalent circuit can be given by the following equation [32–38],

$$Z^* = ReZ + iImZ = Z' + iZ'' = R_s + \frac{R_p}{1 + i\omega R_p C_p} \tag{8}$$

where Z' and Z'' are the real part and imaginary parts of the complex impedance, and $\omega(=2\pi f)$ is the angular frequency of the ac excitation. Z' and Z'' are given by,

$$ReZ = Z' = \left[R_s + \frac{R_p}{1 + \left(\omega R_p C_p\right)^2}\right], \tag{9}$$

$$-ImZ = Z'' = \left[\frac{\omega R_p^2 C_p}{1 + \left(\omega R_p C_p\right)^2}\right]. \tag{10}$$

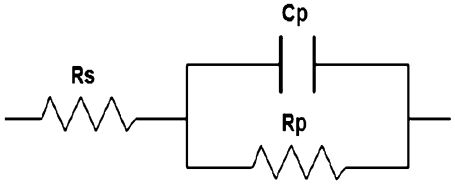

Fig. 11 Proposed equivalent circuit model consist in terms of a single parallel resistance R_p and capacitance C_p network with a series resistance R_s

By removing the angular frequency from the equations, the semicircle is associated with the real and imaginary parts of the complex impedance. In other words, the semicircle of the Cole–Cole plot can be defined by the following equation,

$$\left[ReZ - \left(R_s + \frac{R_p}{2}\right)\right]^2 + (-ImZ)^2 = \left(\frac{R_p}{2}\right)^2. \quad (11)$$

This equation defines a circle centered at (R_s+R_p/2,0) with radius R_p/2.

The impedance measurements were carried over wide frequency range of 100 Hz–1 MHz. Figure 12a and b show the variation of real part (ReZ or Z′) and imaginary part (ImZ or Z″) of the complex impedance with frequency at various dc bias voltages. It is observed that the ReZ and ImZ value decrease with increasing applied dc bias. As seen in Fig. 12a, the magnitude of ReZ remains constant up to a certain frequency, then decreases rapidly with increasing frequency. As seen in Fig. 12b, the ImZ plots give a peak for all bias voltages. The ImZ increases with increasing frequency and reaches a maximum peak value, then decreases with increasing frequency. Also, the position of the Z″ peak shifts to higher frequencies with increasing dc bias voltage. This observed peak confirms the single relaxation process in the system. At this case, the dielectric relaxation time τ (= 1/ω_{max}) can be determined from the position of the peak. When the bias voltage is increased and consequently the parallel resistance R_p decreases, the relaxation time decreases with increasing dc voltage. This decrease of relaxation time is attributed to the injection of charge carriers into the device [37, 38].

Figure 13 shows the Cole–Cole plots at various bias voltages. As seen in Fig. 13, these plots indicate a single semicircle for all dc bias voltages. Moreover, it is observed that the size and radius of these semicircles decrease with increasing applied dc bias. A single semicircle suggests the equivalent electrical circuit, shown in Fig. 11. In other words, the device can be modeled by an equivalent circuit which consists of the parallel resistance (R_p) and the capacitance (C_p) network in series with a series resistance (R_s) [38–40].

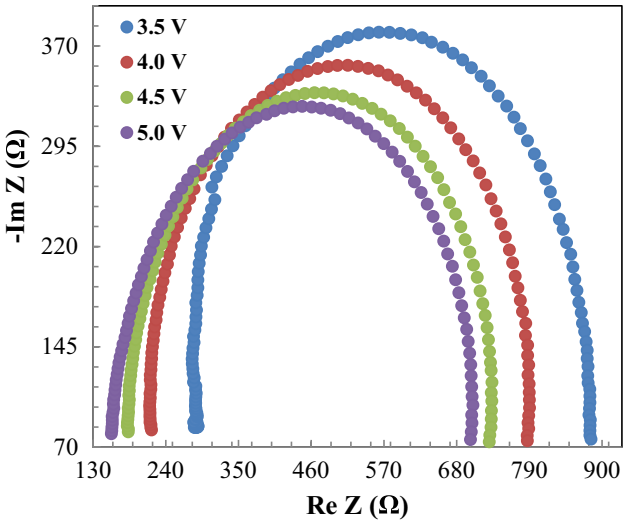

Fig. 13 Cole–Cole plots at various dc bias voltages

The minimum ReZ value represents R_s, and the maximum ReZ value corresponds to the summation of R_s and R_p to the capacitance C_p [9]. The R_s is caused by the electrode contact. The fitting parameters of impedance data of the device by provided the equivalent electrical circuit at various bias voltages are given in Table 2. As seen in Table 2, R_s, R_p and C_p value decrease as the dc bias voltage increases. The decrease of R_p is because of the increasing in the number of injected charge carriers into the device [37–41].

As a result both the value of N_{ss} and R_s are more effective on the C–V and G–V characteristics. On the other hand, while the value of N_{ss} has an effect in the depletion and inversion regions at low frequencies, R_s has an effect on the

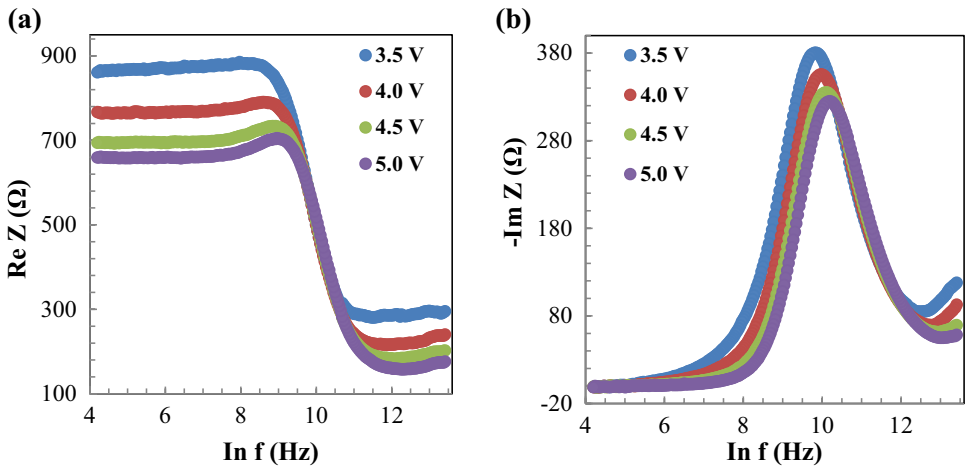

Fig. 12 The variation of **a** real (ReZ) and **b** imaginary (ImZ) part of the complex impedance with frequency at various dc bias voltages

Table 2 The fitting parameters (R_s, R_p and C_p) of impedance data for the device at various bias voltages

Voltage (V)	R_s (Ω)	R_p (Ω)	$C_p \times 10^{-9}$ (F)
3.5	270.3	628.1	8.63
4.0	208.9	582.2	7.79
4.5	175.9	549.7	7.17
5.0	151.5	523.5	6.66

accumulation region at high frequencies. Usually, during the fabrication of semiconductor devices such as metal–semiconductor (MS) structures with and without an interfacial insulator or polymer layer (MIS or MPS), many defects/dislocations can be occurred and which lead to electronic states with energies located in the forbidden band gap of the semiconductor between interfacial layer and semiconductor interface. These states are known as surface states or traps (N_{ss} or D_{it}) and alter the performance of these devices. Usually they can be originated from defects such as dangling bounds between interfacial layer and semiconductor with energy states in the semiconductor band gap (E_g) and dependent on the chemical composition of the interface [23–31, 42–45]. These electronic states can be stored and released charges when an appropriate dc and external ac signal is applied on the sample. These states can be arise from four different sources: (1) interface trapped charges which are located at interfacial layer/semiconductor ; (2) fixed oxide charges which are located at or near the interface ; (3) oxide trapped charges which can be created by high energetic radiation and (4) mobile ionic charges such as sodium ions [9, 10]. The changes in the values of C and G/ω with applied biases are especially dependent on the ability of these states to follow the ac signal and their relaxation time (τ). The value of R_s has an effect both on the electric and dielectric properties of electronic devices as well as surface states. Usually it can originate from various sources such as the back ohmic and front rectifier contacts, the probe wire to the gate or rectifier contact, the bulk resistance of the semiconductor, a dirty film or particulate matter at back contact interface and extremely non-uniform doped atoms in the semiconductor [7, 9]. The value of R_s can be reduced either by having a low BH between metal and semiconductor and using heavy doped semiconductors ($\geq 10^{17}$ cm^{-3}) or by the use of a good cleaning and fabrication process.

4 Conclusion

In this study, Au/(Cu_2O–CuO)–PVA/n-Si (MPS) structures were fabricated and their electrical characteristics and energy dependent profiles of N_{ss} and τ have been characterized using frequency dependent C–V and G/ω–V measurements. Both the values of C and G/ω show a large dispersion in the depletion region due to a special distribution of N_{ss} and their life time. On the other hand these dispersions at accumulation region due to the existence of R_s and interfacial (Cu_2O–CuO)–PVA polymer layer. While the polarization and surface states are effective at low frequencies, R_s is effective only at enough high frequency ($f \geq 500$ kHz). Some main electrical parameters such as V_D, N_D and $\Phi_{B(C-V)}$ were found from the reverse bias C^{-2} versus V plot as 0.33 eV, 7.60×10^{13} cm^{-3}, 0.65 eV at 10 kHz and 0.70 eV, 6.99×10^{13} cm^{-3}, 1.02 eV at 3 MHz. While the value of $\Phi_{B(C-V)}$ increases almost as exponentially, N_D decreases. Such behavior of $\Phi_{B(C-V)}$ and N_D with frequency is the effects of N_{ss} and polarization. In addition, the R_s versus V plot was obtained from the C–V and G/ω–V data using Nicollian and Brews method and it has one distinctive peak at low frequencies. While the magnitude of the peak decreases with increasing frequency, its position shift towards lower or negative bias voltage with decreasing frequency due to the reordering and restructuring of surface states and their relaxation time under applied bias voltage. The energy dependent profile of N_{ss} and their relaxation time (τ) were found by using admittance method and they ranged from 1.09×10^{11} to 1.60×10^{11} eV^{-1} cm^{-2} and 7.75×10^{-6} s to 9.93×10^{-5} s, respectively. The obtained values of N_{ss} which are order 10^{11} eV^{-1} cm^{-2} are more suitable for an electronics device. These low values of N_{ss} are indicated that the (Cu_2O–CuO)–doped PVA interfacial layer considerably enhances the performance of the Au/n-Si (MS) structure. Therefore, (Cu_2O–CuO)-doped PVA polymer interfacial layer can be successfully used instead of the traditional insulator/dielectric layer due to its passivized the surface states. The impedance measurements were also performed in the wide range of frequency (100 Hz–1 MHz) at room temperature. The equivalent circuit model parameters such as parallel resistor (R_p), capacitor (C_p) and a series resistance (R_s) were calculated from Cole–Cole plots. Experimental results show that the R_s, R_p and C_p value decrease as the dc bias voltage increases. The decrease of R_p is because of the increasing in the number of injected charge carriers into the device.

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