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Effect of nitrogen passivation/pre nitration on interface properties of atomic layer deposited HfO_2

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Abstract

Properties and quality of thin films depend on the methods used to deposit it. ALD is a surface dependent process and is one of the best deposition techniques because of the control we have on the deposition. In ALD, quality of initial few layers depends on substrate surface. A well prepared substrate surface reduces problem of nucleation. In this work, we have reported nitrogen passivation/pre nitration of silicon wafer as a surface preparation technique for atomic layer deposition. The results obtained have shown that the nitrogen passivation/pre nitration have profound effect on electrical characteristics. Nitrogen passivation has been done at two different temperatures, 350 and 500 °C. Crystal structures and phase information of deposited HfO_2 thin films were studied in passivated and non passivated cases using GI-X-ray diffraction, elemental composition was investigated by EDX. Capacitance–voltage (C–V), current–voltage (I–V) and conductance–voltage (G–V) measurements were performed. The density of the interface state charges (D_{it}) was computed from C–V and G–V characteristics. Leakage current has been reduced almost two fold by utilizing this technique indicating change in properties of deposited oxide and its interface with the substrate. Decrease in interface trap charges has also been observed. Density of interface traps has been decreased from 2.87×10^{-12} to 1.57×10^{-12} cm^{-2} eV^{-1}. Crystallographic phase of the deposited films are also found different in two different temperatures, 350 and 500 °C of passivation. Crystallographic phase of the deposited films were determined from analysis of measured XRD spectra and are found different in two cases.

1 Introduction

In order to meet the requirement of low power, high density and high speed electronic devices, down scaling of MOS transistor (basic building block of memories and other devices) are being constantly tried [1]. This small geometry using similar material has resulted in a new set of problems such as increased leakage current, sub-threshold conduction, drain induced barrier lowering (DIBL), various short channel effects, dopant penetration and serious reliability problems [2]. Silicon dioxide has driven the semiconductor industry for several decades, but with scaling of MOS transistors, thickness of SiO_2 gate dielectric is decreased in order to increase the drain current, reduce threshold voltage and increase device performance [1]. Reduced thickness of the gate dielectric results in increased leakage current and so power dissipation. Increased power dissipation has severe effects on reliability of devices [2]. Replacing SiO_2 gate oxide with suitable high dielectric constant substances permits increased gate oxide thickness and very small leakage current for the same gate capacitance [3, 4]. High K dielectric substances are solution to overcome the scaling limit of SiO_2. There are several candidate high-K materials such as Al_2O_3, Ta_2O_5, TiO_3, La_2O_3, $LaAlO_3$, HfO_2, ZrO_2 and their silicates & aluminates. The choice of the alternate gate oxide has been narrowed to group IV B oxides, particularly HfO_2 and ZrO_2 due to their excellent electrical resistance, fabrication compatibility and thermal stability on Silicon and other substrates. Both of these oxides have high dielectric constant (> 25), good thermal stability, and high conduction band offset (~ 1.5 eV). The gate oxides need to be chemically and thermally stable and compatible with the substrate material. Hf and Zr based oxides have low crystallization temperature [3, 4]. In standard CMOS fabrication processes, gate stacks undergo rapid thermal annealing (RTA) and some other fabrication steps of more than 500–600 °C that may result in easy crystallization during these steps. Grain boundaries in crystalline thin films may result in increased gate leakage, can offer path for diffusion of dopants that can lead to

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dielectric breakdown [5]. Increase in crystallization temperature has been tried through incorporation of elements such as N, Al and Si. Other than this (low crystallization temperature), high interface state density is also an issue with these oxides [3, 4]. Pyrolytic-gas passivation (PGP) has been used as one of the methods to passivate silicon dangling bonds [6, 7]. Some other methods also have been tried by the researchers to passivated dangling bonds [8, 9]. Passivation of dangling bonds is also important for devices working in radiation environment as reported by some researchers [10–13]. In this study, passivation with nitrogen (N_2), has been extensively explored. This might complement PGP. This paper reports the fabrication processes that would improve the electrical behavior of HfO_2.

Nitrogen was introduced into the silicon/oxide interface to improve electrical properties of the deposited oxide films. A number of varying effects were reported [14]. Better boron diffusion resistance and better hot carrier reliability were observed [15, 16]. However, other electrical properties, such as channel mobility and interface trap density have deteriorated by nitridation [17, 18]. Nitrogen incorporation mainly occurs at Si/SiO_2 interface and on the surface. This was attributed to the nitridation of silicon dangling bonds and nitridation of Si–Si bonds [17]. Nitrogen incorporation increases crystallization temperature and dielectric constant of hafnium dioxide [19]. It also reduces boron penetration in the oxide [15, 16]. It has been reported that nitrogen incorporation in hafnium dioxide can reduce the leakage current, although hafnium nitride is in fact a conductor [16, 19, 20]. Reduction in the leakage current is attributed to the suppression of centers of oxygen vacancy (Vo). The centers of oxygen vacancy are supposed to be the major conduction path in hafnium dioxide. Incorporation of nitrogen atoms next to the oxygen vacancy may push the vacancy level out of the gap, as shown by theoretical calculations [21, 22]. Some authors have reported effect of nitrogen annealing on electrical characteristics [23, 24]. It is important to find the interrelation among the growth/process conditions for the HfO_2 films, their crystal structure, and electronic properties. In this study, the effect of incorporation of nitrogen during thermal annealing has been presented in detail. Nitrogen gas passivation during film fabrication has shown considerable improvement in leakage current, dielectric constant, crystallization temperature and stress induced behavior which may be of considerable technological interest for other dielectric applications such as in MIM capacitors.

2 Experimental details

P-type <100> silicon wafers with resistivity of 0.1–0.5 Ω-cm were used for the fabrication of the MOS capacitor. Standard RCA process was used for cleaning the single side polished (SSP) Si wafers. The thin layer of native SiO_2 that forms after the RCA cleaning was removed by dipping wafers in hydrofluoric acid (HF) and de-ionized (DI) water in the ratio of 1:10 at a temperature of 20 °C for 15 s. After rinsing in de-ionized water, the wafers were dried immediately in dry N_2. Since ALD is a surface dependent process, properly processed surface offers less nucleation in initial few cycles of atomic layer deposition. Therefore, few silicon wafers were subjected to pre-nitration at 350 and 500 °C before loading them in the load lock chamber of ALD system for deposition of HfO_2. HfO_2 films were deposited on cleaned wafer by atomic layer deposition. The number of reaction cycles was chosen in order to achieve HfO_2 thickness of 7 nm. A thin film of 300 nm aluminum (Al), was used as top electrode. The Al film was deposited by DC magnetron sputtering on top of the HfO_2 layer. Al thin film was patterned by photolithography followed by wet etching to obtain capacitors of different areas varying from 40×50 to $120\times130\ \mu m^2$ and different shapes. AZ ECI 3027 has been used as positive photoresist in photolithography. Generally, adhesion of photoresist onto inorganic material surface is poor and results in loss of fine structures after the PR development. HfO_2 is an inorganic material with relatively poor adhesion to AZ ECI 3027. Therefore, oxygen plasma has been used for 52 s as adhesion promoter for photo resist instead of popular adhesion promoter HMDS (Hexa-methyl di-siloxane). AlSi thin film of 300 nm was deposited as backside electrode after chemical mechanical polishing of backside of Si wafer. Finally MOS capacitors were annealed in forming- gas at 450 °C for 30 min. The electrical characteristics of the MOS capacitors were measured using Agilent B1500A Semiconductor Device Parameter Analyzer and Keithley SCS-4200. To measure step coverage and precise electrode size, surface profilometry and SEM characterization have been carried out respectively. Glancing angle X-ray diffraction (GA-XRD) pattern has been measured to determine the crystal structure and phase information of the deposited hafnium dioxide. Elemental composition of the deposited HfO_2 has been done by EDX analysis and has been carried out using JEOL SEM operated on 16 kV of accelerating voltage. More details about fabrication can be found in [25].

3 Results and discussion

3.1 Crystallographic analysis

HfO_2 can exist in four crystal phases: monoclinic (m-HfO_2), cubic (c-HfO_2), orthorhombic (o-HfO_2) and tetragonal (t-HfO_2) with different electronic properties [26]. Therefore it is important to find out crystal phase information of deposited HfO_2. Crystal structure and

phase information of the deposited HfO_2 thin film samples have been determined using GI-XRD. Stress was laid on the comparative measurements of XRD spectrum and electrical characteristics of the experimental HfO_2/Si-substrate structures with and without nitrogen passivation. Passivation lead to more complicated structures and these were explored using X-ray analysis of ultrathin films. Figure 1 shows the XRD spectrum of atomic layer deposited HfO_2 thin films, deposited on silicon. Figure 1a is for the case without any passivation, Fig. 1b for the case with pre annealing/nitrogen passivation at 500 °C. The XRD pattern of non passivated HfO_2 contains peaks at different Bragg's angles. These peaks are allocated to crystallographic plane that implies presence of nano-crystallites. XRD spectrum also shows other peaks indicating the presence of monoclinic crystallites. It is a sign of presence of anisotropy in the thin film structure. Crystallographic plane (-111), seen at 31.64°, has the lowest strain energy [22] among the crystallographic planes. Another major crystallographic plane is seen at 28.36°. Crystallographic orientations along the (-111) and (111) planes have different size of crystallites. Figure 1b shows XRD spectra of HfO_2 with pre annealing/passivation at 500 °C. Deposited film is orthorhombic in nature. Three major crystallographic planes are seen at 30.36°, 34.28° and 35.46°. Peak seen at 30.36°, corresponds to crystallographic plane (211), peak at 34.28° corresponds to (020) plane and peak at 35.46° corresponds to (002) plane. Without any passivation/pre annealing in nitrogen, the deposited thin films are monoclinic in nature whereas, when silicon substrate is passivated in nitrogen at 500 °C, the deposited thin film shows orthorhombic nature.

3.2 X-ray reflectivity (XRR) measurements and analysis

After deposition of the thin film, X-ray reflectivity (XRR) was utilized for the measurement of thickness, surface and interface roughness, and the density of the HfO_2 thin film deposited on silicon. There is slight variation in the density of the HfO_2 thin film for passivated and non-passivated thin films of HfO_2. Density of the HfO_2 was found to be approximately equal to 9.62 and 9.64 g/cc for passivated and non-passivated thin films respectively. Roughness of the deposited oxide films were found to be around 2–3 Å.

3.3 Electrical characterization

The electrical parameters such as leakage current, variation in capacitance and conductance as a function of applied voltage, density of interface states can be used to enumerate the quality of oxide layer [27]. The same parameters were measured and analyzed by the author for the HfO_2 based MOS capacitors in both the processing conditions. Nitration of silicon surface was done at two different temperatures: 350 and 500 °C.

To characterize MOS capacitor for leakage current behavior, all the samples were measured in the accumulation region (negative bias), depletion region and in the inversion region (positive bias). Figure 2a shows effect of nitration at 350 °C on leakage current behavior by using semi logarithmic graph of current density (J) versus voltage (V). This butterfly curve is asymmetrical in nature. In the case of nitration at 350 °C, there is significant decrease in the leakage current in accumulation as well as in the inversion regions. Effect of nitration at 500 °C on leakage current behavior is shown in Fig. 2b. It also shows considerable decrease in leakage

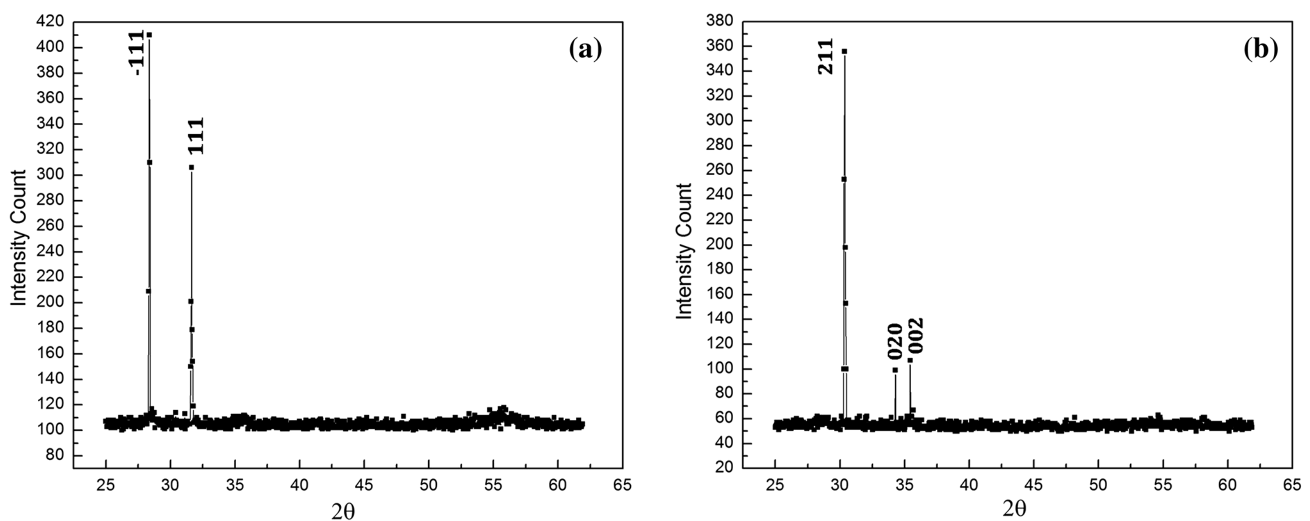

Fig. 1 **a** XRD spectra of HfO_2 without any pre annealing/passivation. **b** XRD spectra of HfO_2 with pre annealing/passivation at 500 °C

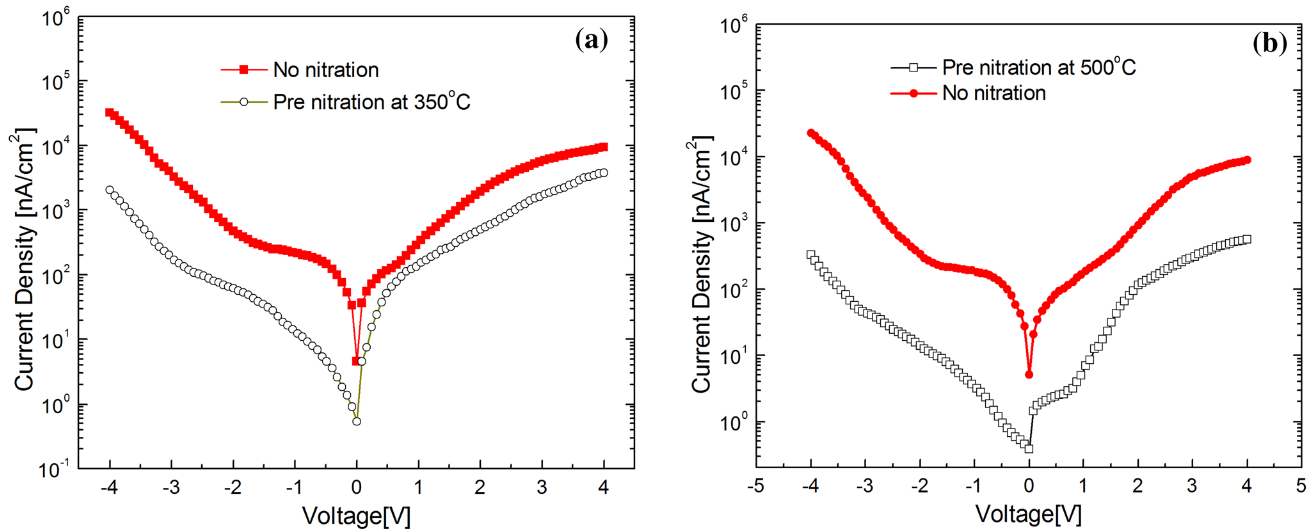

Fig. 2 Current density versus voltage curves **a** effect of pre nitration at 350 °C, **b** effect of pre nitration at 500 °C

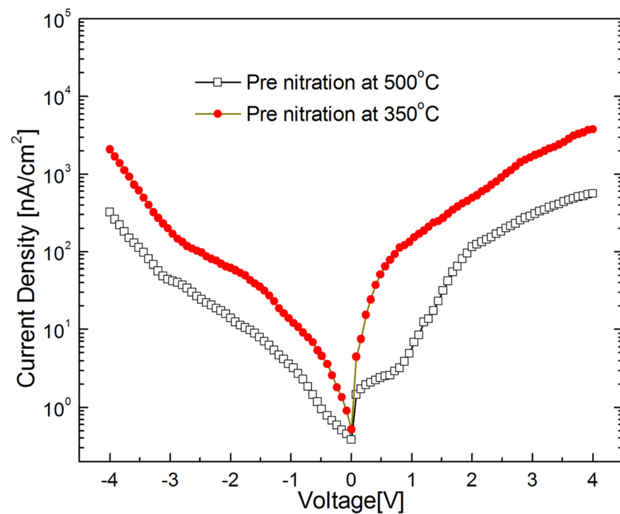

Fig. 3 Current density versus voltage curves: comparison of pre nitration at 350 °C and at 500 °C

current for samples pre-nitrated at 500 °C. Figure 3 shows a comparison of nitration at 350 and 500 °C. It can be seen from the Figs. 2 and 3 that the leakage currents are nearly two to three orders in magnitude lower for pre nitrated/passivated sample. Although, reduction in leakage current is observed for both the nitration temperatures, but higher temperature of nitration (500 °C) shows better leakage current behavior, when both the nitration temperature are compared. Lower value of leakage current in pre nitrated/passivated samples indicate improved interface behavior after nitration.

Capacitance–voltage (C-V) and conductance–voltage (G–V) measurements have been carried out on samples at frequencies of 50 kHz, 100 kHz, 200 kHz, 500 kHz and 1 MHz and several parameters has been computed from the measured C–V and G–V curves to quantify effects of pre nitration/passivation.

C–V curve in accumulation and in depletion region is dominated by majority carrier charge density at the silicon surface whereas minority carriers govern steady state C–V response in inversion region. Minority carrier density is negligible compared to that of majority carrier density at silicon surface in accumulation and in inversion region [25, 27]. Majority carrier responds quickly to the ac voltage applied to the gate for all measurement frequencies (50 kHz–1 MHz) used in the experiments here. Response of minority carriers is much slower over the frequency range of interest therefore affecting C–V response in inversion region [20]. Various types of charges are present in the oxide and they affect the C–V response in a complex manner. There are two fundamental types of charges in the oxide layer above the silicon substrate. One is interface trap charges located at or near the interface of silicon and oxide and the other is bulk trap charges, uniformly distributed throughout the Si-substrate. Distinguishing feature of bulk charges with that of interface charges is that the amount of interface charges varies with the applied gate bias whereas bulk trap charges are independent of gate bias. Bulk trap charges are predominantly measured in strong inversion region and create measurable capacitance. This can be considered as a parallel plate capacitance, which is in series with the oxide capacitance and in parallel to that of substrate capacitance. The measured capacitance in the accumulation region is mostly contributed by oxide capacitance. If the density of interface charge defect (D_{it}) is large enough, it contributes to the measured total capacitance in depletion and inversion regions. These

interface charge defects can deform the profile of the C–V curve and create bumps [25, 27].

Figure 4a shows effect of pre-nitration at 350 °C on C–V characteristics measured at 1 MHz. Figure 4b shows effect of pre-nitration at 500 °C on C–V characteristics measured at 1 MHz. Oxide capacitance decreases with pre-nitration of silicon substrate at both the temperatures i.e. that pre-annealing (pre-nitration) of silicon samples in nitrogen just before ALD deposition decreases dielectric constants of the oxide. Pre-nitration of silicon wafer affects the surface and since ALD is a surface dependent process, it affects the properties of the deposited oxide as can be seen from Fig. 4 and Tables 1 and 2. Pre-nitration reduces interface charge density (D_{it}) effectively, and it is true for both the temperatures 350 and 500 °C, of passivation. While pre-nitration reduces interface trap charge density (D_{it}), it also increases the effective oxide charge (Q_{eff}), and effective number of charges per unit area (N_{eff}), as seen from the shift of C–V curve and flat band voltage to more negative values. Reduction of capacitance, increase in effective oxide charge and reduction in interface trap charge are just opposite to that of other results in the literature [19, 21, 22]. The difference in the behavior can be attributed to the manner in which nitrogen is incorporated. In this study, nitrogen incorporation was achieved by annealing the silicon substrate in nitrogen at 350 and 500 °C for 30 min, before the deposition of HfO_2 by ALD. In the literature, nitrogen was introduced by plasma immersion ion implantation in the presence of different gases. Nitrogen incorporation by annealing affects the silicon wafer surface (with native oxide) effectively by reducing the leakage current density and interface trap charge density. But it increases the effective bulk charge density. The other possible reason for reduction of capacitance is, formation of low dielectric constant $HfSiyO_XN_{1-x}$ interface layer, although, presence of nitrogen is not confirmed by EDX spectrum of the deposited thin films.

As stated earlier, five different frequencies have been used for the measurement to make an estimate of interface states

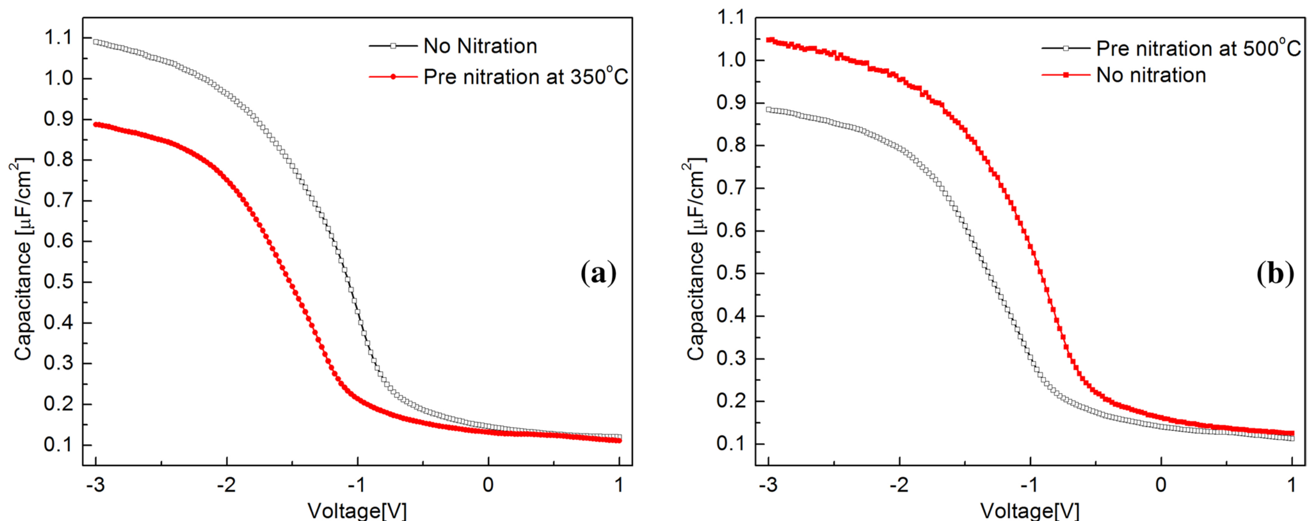

Fig. 4 Effect of pre nitration/passivation at **a** 350 °C, **b** 500 °C

Table 1 Calculated parameters for Fig. 4a showing effect of pre-nitration at 350 °C

Sample	V_{FB} (V)	$Q_{eff} \times 10^{-6}$ (C/cm^2)	$N_{eff} \times 10^{12}$ (cm^{-2})	$D_{it} \times 10^{-12}$ (cm^{-2} eV^{-1})
No nitration	−1.25	1.18451	7.40319	2.87146
Pre-nitration at 350 °C	−1.61	1.18451	8.0212	1.57044

Table 2 Calculated parameters for Fig. 4b showing effect of pre-nitration at 500 °C

Sample	V_{FB} (V)	$Q_{eff} \times 10^{-6}$ (C/cm^2)	$N_{eff} \times 10^{12}$ (cm^{-2})	$D_{it} \times 10^{-12}$ (cm^{-2} eV^{-1})
No nitration	−1.06	0.944316	5.90197	2.48664
Pre-nitration at 500 °C	−1.42	1.11125	6.94531	1.78855

that are frequency dependent. For every applied frequency a particular portion of interface states respond to the AC signal. Since the substrate in this case is p-type, holes are majority carriers. The hole emission rate of these affected states is within the frequency range of the applied frequency. This means that at high frequency (1 MHz) a smaller number of interface charge states respond to the exciting signal and those interface charge states are filled with holes, giving rise to a shift (or stretching) of the C–V curve. When applied frequency is lowered, a larger part of the interface charge states are able to follow the applied frequency that results in shift (or stretching) of the C–V curve corresponding to the interface charges that responded to the applied frequency. The slope of C–V curve in transition region i.e. from C_{max} to C_{min} gives a direct measure of interface states/defects present at the interface. A sharp slope indicates presence of fewer defects at the interface.

Figure 5a shows normalized C–V curve for pre nitrated (350 °C) and non-nitrated samples at five different frequencies. Figure 5b shows normalized C–V curve for pre nitrated (500 °C) and non-nitrated samples at five different frequencies. There is a relative shift among the C–V curves obtained at different frequencies. Ideally, there should not be any shift in flat band with change in measurement frequency. The observed shift at different measurement frequencies is indicative of the presence of a number of traps with varying time constants at the interface. One can also observe a lateral shift in C–V curves of Fig. 5a, b. The observation is prominent for nitrogen passivated samples in comparison to the samples that are not annealed in nitrogen before HfO_2 deposition.

4 Conclusion

Effect of pre-annealing/nitration/nitrogen passivation of silicon wafer in nitrogen ambient at two different temperatures of 350 and 500 °C has been studied. Non pre nitrated samples are monoclinic while pre nitrated samples are orthorhombic in nature. Pre-nitration decreases leakage current density and interface trap charges. As the pre-nitration temperature increases from 350 to 500 °C, further reduction in leakage current density and interface trap charge density were observed. Improvement in the leakage current behavior and interface properties are obtained on account of decrease in the oxide capacitance and increase in effective oxide charges. Shift in flat band voltage is also observed with the increase in pre-nitration temperature.

To conclude the extensive set of measurements of the electrical parameters such as leakage current, flat band voltage, density of interface states and hysteresis were evaluated using MOS C–V and I–V characteristics. This clearly demonstrates that nitrogen incorporation helps to improve the electrical properties. Pre-deposition annealing in nitrogen/pre nitration of Si can be used as one of the ALD surface preparation techniques to fabricate high quality of ultrathin oxides with very low leakage current.

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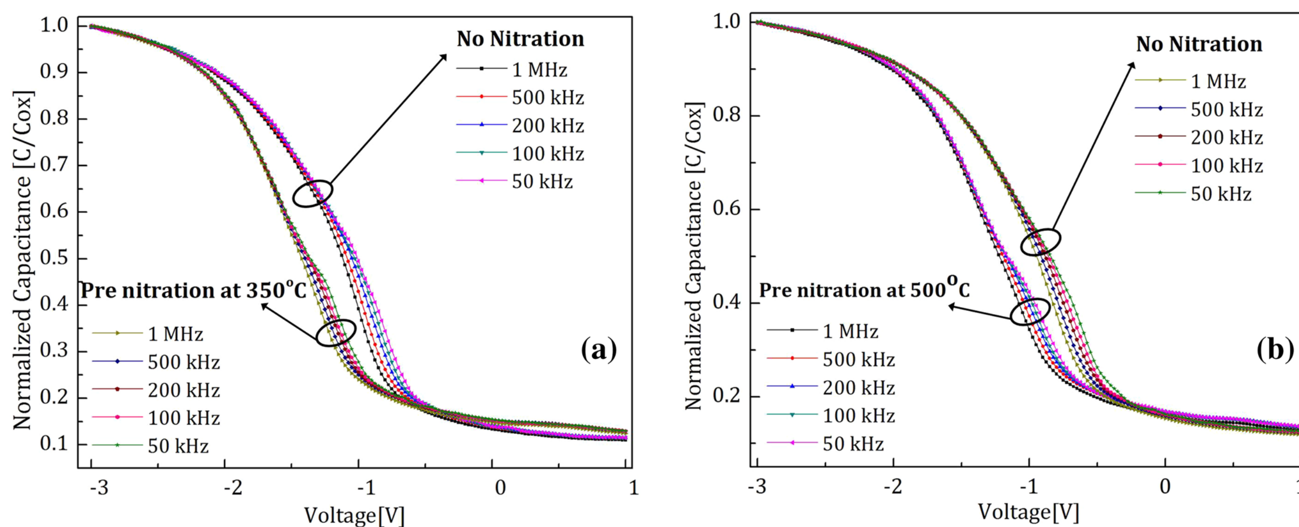

Fig. 5 Effect of pre nitration/passivation at **a** 350 °C, **b** 500 °C at different applied frequencies

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