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Current–voltage characteristics of Au/ZnO/n-Si device in a wide range temperature

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Abstract Au/ZnO/n-Si device was obtained by using atomic layer deposition (ALD) technique, and it was characterized by I–V measurement in a wide temperature from 100 to 380 K with 20 K steps. XRD measurements were performed on ZnO thin film layer, and (002) and (201) peaks were seen in XRD pattern of the film. Surface morphology and cross section of the device were taken by SEM and discussed in the details. Some device parameters such as barrier height, ideality factor, series resistance were calculated by thermionic emission theory (TE), using Cheung's and Norde's functions. The Calculation results revealed that all device parameters strongly depended on temperature changing. In addition, interface states (N_{ss}) graphs were plotted and discussed according to energy levels and measurement temperatures. It can be concluded that this device can be used in various technological applications in wide range temperatures in industry.

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1 Introduction

Metal–semiconductor devices are very interesting and promise for electronic applications [1–5]. These devices can be used as rectifiers, inverters, photodiode and photodetectors [6–9]. Changing properties of these devices can be accomplished by inserting some kind of metal oxide or insulator layers between the metal and semiconductor [10–12].

The ZnO can be inserted as a metal oxide layer between the Au metal and n-type Si semiconductor for controlling of properties of this metal and semiconductor device because the ZnO metal oxide layer has high direct band gap (3.37 eV) [13, 14]. Also, the ZnO layer can be obtained low cost and low temperature deposition technique [15]. The ZnO as a semiconductor can be used in lasers, solar cells, photodetectors and varistors [16–19]. To obtain a ZnO thin film layer, it can be used chemical vapor deposition [20], spray pyrolysis [21], sol gel [22] and atomic layer deposition techniques (ALD) [23]. Among them, ALD technique has more advantageous for obtaining uniform film and definite thickness control [24, 25].

The measurement temperature of the sample is very important parameter for metal–semiconductor devices because it can affect main properties of those kinds of devices, and these devices can be used at various temperature after understanding temperature dependent features [26, 27]. When it can be checked in the literature, it can be seen many investigations on temperature-dependent electrical properties of metal–semiconductor devices. For instance, Mtangi et al. [28] investigated temperature-dependent current–voltage (I–V) characteristics of Pd/ZnO Schottky barrier diodes in 60–300 K temperature range. They showed that ZnO has different conduction mechanism in different temperatures, and has stable ideality factor and barrier height in this temperature range. Yadav et al. [7] studied high

temperature-dependent electrical properties of Pd/ZnO/*n*-Si/Ti/Al device. They obtained ZnO layer using sol–gel spin coating technique and concluded that the saturation current and barrier height increased with the temperature increment. Khare et al. [29] researched the temperature-dependent current–voltage (*I–V*) characteristics of ZnO/P3HT:PCBM junctions. ZnO layer were obtained atmospheric pressure spatial ALD and electrodeposition techniques. In this junctions barrier height decreased and ideality factor increased with increasing temperature. They emphasized that the samples need to be thermally annealed for higher photoresponse properties of the junctions in their study. These are three different studies, but there is no any investigations about the temperature-dependent *I–V* characteristics of Au/ZnO/n-Si devices in the literature. This is important for better understanding of ZnO role in the interface of the metal–semiconductor devices.

In this context, the aim of this study is to investigate the temperature-dependent *I–V* characteristics of the Au/ZnO/*n*-Si device for technological applications in the wide range temperatures from 100 to 380 K with 20 K steps.

2 Materials and methods

n-Type Si substrate, which has (100) orientation, was used for producing Au/ZnO/*n*-Si device. Firstly, Si wafer was cut into 1 cm^2 pieces (square shape), and they were cleaned and etched with various solvents and acids (H_2SO_4:H_2O_2:H_2O (5:1:1) for 1 min). Secondly, high purity gold was evaporated thermally back side of the Si wafers for ohmic contact, and then wafers were annealed in N_2 atmosphere at 450 °C for 3 min. Thirdly, ZnO layer was deposited on front side of Si wafers for 10 nm ZnO layer with 1.45 Å growth rate at per cycle by ALD technique which had 5×10^{-3} Torr vacuum, 180 °C temperature and zinc acetate and water sources. Fourthly, Au metal was doped on the ZnO surface as metallic contacts using a mask with 1.0 mm diameter holes on the device. Shematic diagram of the device has been shown in Fig. 1. The ZnO film layer in the device was characterized with Bruker D8 Discover XRD. SEM images were obtained ZEISS Sigma 300. The *I–V* measurements of the device were obtained by using a homemade liquid nitrogen cryostat equipped with a temperature controller in darkness in the range of 100–380 K temperatures with 20 K steps at 500 kHz frequency.

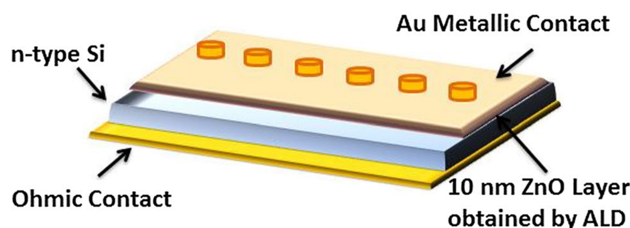

Fig. 1 Schematic diagram and image of Au/ZnO/n-Si device

3 Result and discussion

XRD graph of ZnO thin film layer has been indicated in Fig. 2 from 20° to 80°. It can be seen two peaks in that figure: one of them and severe one is (201) peak, other and weak one is (002) peak. These peaks have implied that ZnO thin film layer was obtained successfully by the ALD technique. XRD peaks also referred to the hexagonal structure of the ZnO [30].

Surface and cross-section images of the device were taken to investigate surface morphology properties of the device using SEM. These images have been given in Fig. 3a, b for surface of the ZnO thin film and cross-section of the Au/ZnO/n-Si, respectively. Figure 3a has pointed out that ZnO thin film, which has smooth and homogenous surface, has been obtained successfully by ALD technique. Figure 3b has showed that device was composed also successfully on Si wafer. The surface morphology of the ZnO thin film has revealed that ALD technique is promising technique to deposit good films on a substrate [31, 32].

The *I–V* characteristics of Au/ZnO/*n*-Si have indicated for changing temperature from 100 to 380 K for 20 K steps in Fig. 4 (inset figure shows 300 K *I–V* characteristics of the device). The device has good rectifying property at all temperatures, and this indicates that the temperature increase or decrease do not change rectifying properties of the device. This conclusion implied that this device can be used for wide temperature ranges [33, 34].

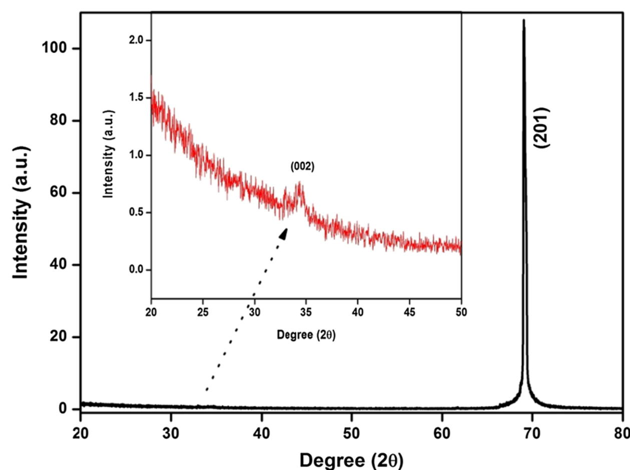

Fig. 2 XRD graphs of ZnO layer obtained by ALD technique

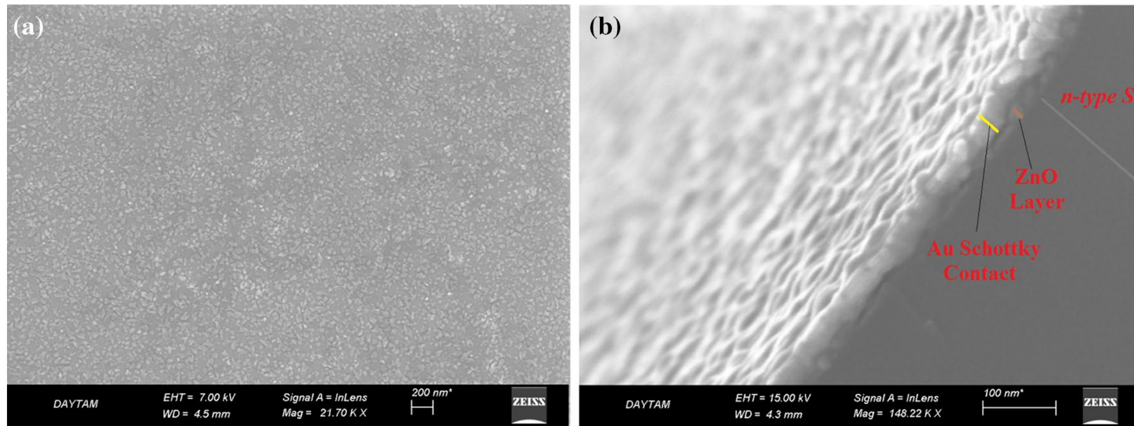

Fig. 3 **a** Surface SEM image, **b** cross-section image of the Au/ZnO/*n*-Si

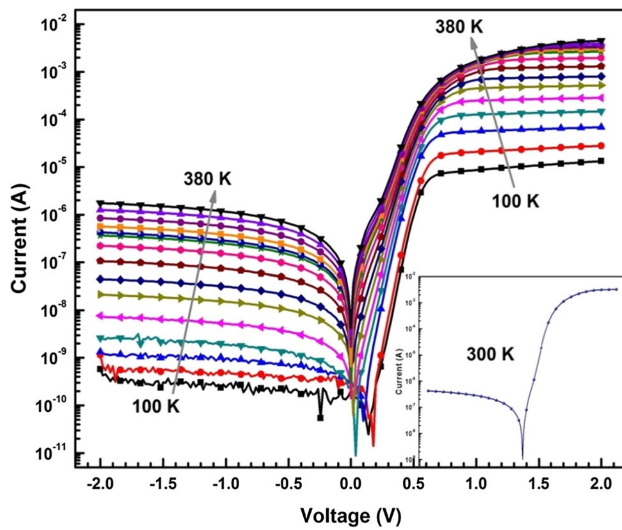

Fig. 4 (online color) *I–V* characteristics of Au/ZnO/*n*-Si device at various temperature

Barrier height and ideality factor were calculated by using thermionic emission theory. According to this theory, current (I) is given below equation:

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(\frac{qV}{nkT}\right)\right] \tag{1}$$

in here, I_0 (saturation current) is intercept value of the linear portion of ln$I$–V plot at $V = 0$, and is given

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \tag{2}$$

In these equations, q is charge of the electron; n, k, T, are ideality factor of device, Boltzman's constant and device temperature, respectively. A and A^* are metallic contact area of the device and Richardson constant (A^* = 112 A cm^{-2} K^{-2} for n-type Si), respectively. Φ_b is the barrier height at zero bias for device. If n and Φ_b is rearranged using Eqs. (1) and (2), they can be typed as follow:

$$n = \frac{q}{kT}\left(\frac{dV}{dlnI}\right) \tag{3}$$

and

$$\Phi_b = \frac{kT}{q} \ln\left(\frac{A^*AT^2}{I_0}\right) \tag{4}$$

n and Φ_b values for all temperature have been listed in Table 1. When n values have decreased from 4.34 at 100 K to 2.40 at 380 K with increasing temperature, Φ_b values increased from 0.39 at 100 K to 0.91 eV at 380 K. These change in n and Φ_b values have been shown in Fig. 5 as a graph. All n values are bigger than one, and it implied that there is no pure thermionic emission (TE) in this device. This difference can be attributed to interface states or barrier inhomogeneity in the interface of the device [35, 36]. At the same time, increasing temperature has increased the saturation current values of the device. Saturation current values have also been listed in Table 1. This device can be used depending on temperature for different applications in technology [37].

Figure 5 shows how barrier height and ideality factor changed with the changing temperature. While the barrier height values have increased with increasing temperature, the ideality factor values have decreased. These changes clearly have concluded that there is no pure TE current in the device [38]. The charge carriers have no enough energy to cross the high barrier height in the lower temperature, but current transport is provided by lower parts of barrier height [39]. If barrier height is not homogeous, this case usually happens, and this causes to increase in the barrier

Table 1 The some electrical parameters of Au/ZnO/n-Si device obtained *I–V* measurements

T (K)	I_0 (saturation current)	*n* (TE)	*n* (Cheung)	Φ_b (TE)	Φ_b (Cheung)	Φ_b (Norde)	R_s (Cheung) (*dv*/*dlnI*–*I*) (kΩ)	R_s (Cheung) (*H*(*I*)–*I*) (kΩ)	R_s (Norde) (*F*(*V*)–*V*) (kΩ)
100	2.47×10^{-11}	4.34	3.42	0.29	0.31	0.39	31.0	28.50	9.370
120	1.42×10^{-11}	3.82	4.23	0.36	0.19	0.46	8.99	12.98	2.815
140	4.74×10^{-11}	3.40	4.99	0.40	0.18	0.49	3.667	5.092	2.417
160	1.35×10^{-10}	3.22	5.50	0.45	0.15	0.53	1.456	2.813	1.049
180	6.11×10^{-10}	3.08	5.86	0.49	0.15	0.57	0.833	1.684	0.671
200	6.42×10^{-10}	2.83	6.14	0.55	0.14	0.65	0.501	1.371	0.560
220	2.86×10^{-09}	2.97	6.45	0.58	0.14	0.70	0.400	1.085	0.041
240	8.19×10^{-09}	2.95	6.70	0.61	0.14	0.74	0326	0.827	0.036
260	1.39×10^{-08}	2.98	6.91	0.65	0.14	0.78	0.283	0.678	0.010
280	2.72×10^{-08}	2.92	7.13	0.69	0.15	0.81	0.259	0.617	0.035
300	4.64×10^{-08}	2.79	7.52	0.73	0.15	0.81	0.247	0.540	0.285
320	3.96×10^{-08}	2.62	7.26	0.79	0.16	0.90	0.250	0.546	0.087
340	5.45×10^{-08}	2.54	7.48	0.83	0.16	0.93	0.240	0.486	0.097
360	7.44×10^{-08}	2.47	7.65	0.87	0.17	0.96	0.237	0.416	0.100
380	9.82×10^{-08}	2.40	7.90	0.91	0.17	1.00	0.228	0.393	0.098

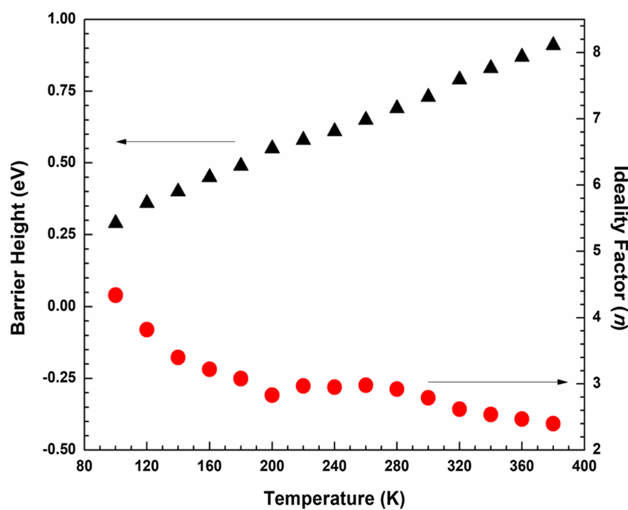

Fig. 5 (online color) Changing of barrier height and idealty factor of Au/ZnO/n-Si device at various temperature

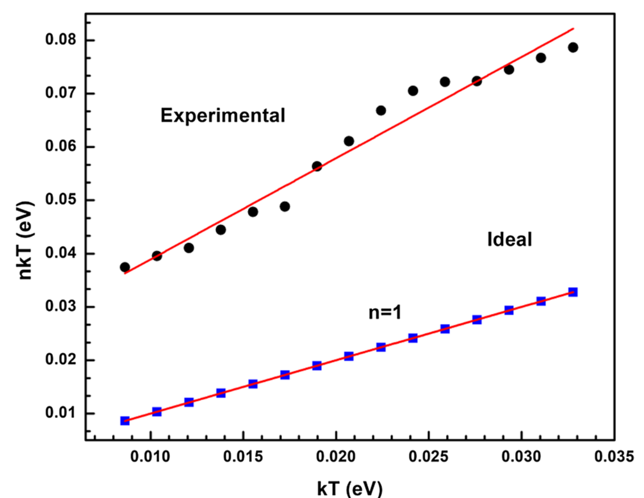

Fig. 6 (online color) The *nkT* versus *kT* plot of Au/ZnO/n-Si device

height and decrease in the ideality factors with increasing temperature [40–42].

To better understand currrent mechanism, the *nkT* versus *kT* plot of Au/ZnO/*n*-Si device has been plotted in Fig. 6. If a diode is ideal, pure thermionic emission happens, and its ideality factor values do not change with increasing temperature as can be seen in Fig. 6. In this device, *nkT* versus *kT* plot have showed almost parallel line to the ideal device but not exactly parallel. It means that associated with TE, other current transport mechanism such as thermionic fileld emission (TFE) has also effectiveness in this device [42]. In addition, this conclusion also have referred to barrier inhomogenity in the interface of the device [38].

The $\ln(I_0/T^2)$ versus $(kT)^{-1}$ or $(nkT)^{-1}$ plots of Au/ZnO/*n*-Si device have been given in Fig. 7. The value of Richardson constant for *n*-type Si is 112 A/(cm K)$^{-1}$, but here, Richardson constant values (can be seen on Fig. 7) are very small from the value of 112 A/(cm K)$^{-1}$. This result showed that there is some barrier inhomogeneity in the interface [42].

The other way to determine the diode parameters, Cheung's functions can be used for this case. Current

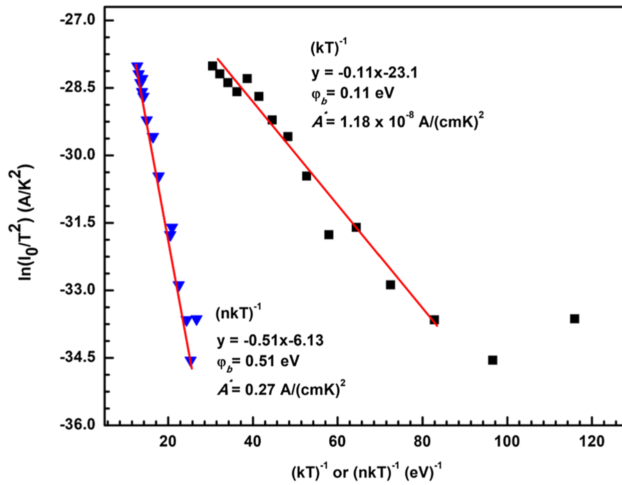

Fig. 7 (online color) The experimental Richardson plots of Au/ZnO/n-Si device

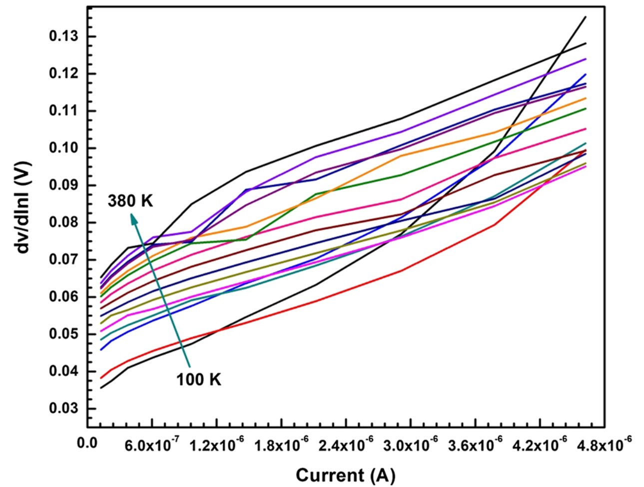

Fig. 8 (online color) *dv/dln(I)* versus *I* plots of Au/ZnO/n-Si device with the changing temperature

expression with considering series resistance of device could be calculated below equation [43]:

$$I = I_0 \exp\left(\frac{q(V - IR_s)}{nkT}\right) \quad (5)$$

where, IR_s voltage dropping which is reasoned by series resistance of the device. This series resistance can be calculated using following expression:

$$\frac{dV}{d(\ln I)} = IR_s + n\frac{kT}{q} \quad (6)$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \quad (7)$$

where $H(I)$ can be arranged as follow:

$$H(I) = IR_s + n\Phi_b \quad (8)$$

Equation (6) is a straight line equation, and if $dV/d(\ln I)$ versus I are plotted, this graph should be linear. According to the Cheung's functions, using this linear plotting, R_s and n values can be obtained slope and intercept of the plots, respectively. Also, expression (8) is again a straight line equation. If obtaining ideality factor is written in this equation to its place, same plotting way, barrier height and series resistance can be calculated. In this plotting, y-axis intercept is equal to $n\Phi_b$ and slope of this plot also provides a different obtaining of R_s which could be controlled the accuracy of Cheung's approximation [43].

The $dV/d(\ln I)$ versus I and $H(I)$ versus I plots of device for different temperatures have been shown in Figs. 8 and 9, respectively. Although there is some deviations in $dV/d(\ln I)$ versus I plots of the device, these plots are good agreement and almost periodic with the changing temperature. $H(I)$ versus I plots have showed very good periodicity with changing temperature. The calculated n, Φ_b and R_s values have been given in Table 1. While n values are increasing, Φ_b values almost stay constant for the changing temperature. The difference in n and Φ_b values obtained from TE current theory can be attributed that TE theory and Cheung's functions obtained different regions of I–V measurements [44]. R_s values which were obtained $dV/d(\ln I)$ versus I and $H(I)$ versus I plots were not so different from each other. These results have corrected consistency of Chung's functions. At the same time, R_s values for two calculations have decreased with increasing temperature because of increasing number of carriers [45].

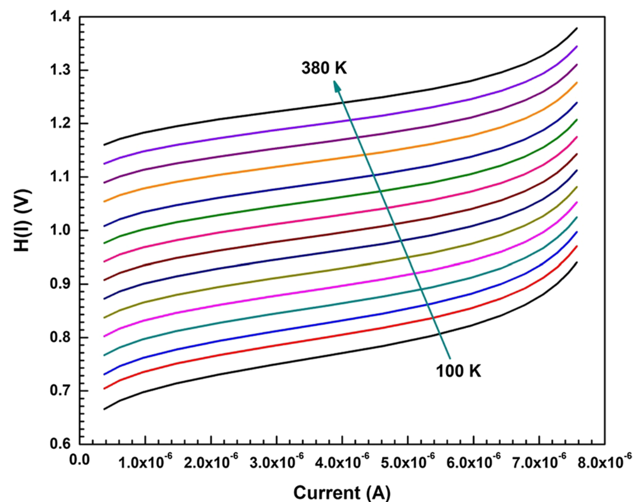

Fig. 9 (online color) $H(I)$–I plots of Au/ZnO/n-Si device in the temperature range of 100–380 K

As another method, Norde's approximation can be used for calculating series resistance and barrier height of the device. Respect to this method, R_s and Φ_b values are given as follow:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{9}$$

where γ is an integer (dimensionless) greater than n and $I(V)$ is current which is acquired from the I–V curve. With aid of this equation, R_s and Φ_b can be rearranged following relations:

$$\Phi_b = F(V_0) + \left[\frac{V_0}{\gamma} - \frac{kT}{q}\right] \tag{10}$$

here $F(V_0)$ is the minimum point of $F(V)$ and V_0 is the corresponding voltage and R_s is with below equation

$$R_s = \frac{\gamma - n}{I}\quad\frac{kT}{q} \tag{11}$$

The $F(V)$ versus V plots of Au/ZnO/n-Si device have been shown in Fig. 10 for the changing temperature from 100 to 380 K. Calculated Φ_b and R_s values were listed in Table 1. While Φ_b values were increased with increasing temperature, R_s values decreased. This decrease can be attributed to increasing carriers in the device with increasing temperature [46]. There are also differences Φ_b and R_s values between obtained Norde's method, TE theory and Cheung's method. These differences can be attributed to that while Cheung's method is applied non-linear region (high voltage), Norde's method is performed all forward bias ln$I$–V plots [47].

The ln$I$–V plot which has a non-linearity part at high forward bias voltages shows a continuous of the interface state density (N_{ss}) in balance with semiconductor. The N_{ss} values for Au/ZnO/n-Si device with changing temperature were calculated from the forward bias I–V by considering efficient barrier height (Φ_e), ideality factor $n(V)$ which is depend on the voltage and R_s. The Φ_e can be written as following equation [48]:

$$\Phi_e = \Phi_b + (1 - 1/n(V))(V - IR_s) \tag{12}$$

Since the ideality factor of a diode become all time greater than one, it was suggested below formula by Card and Rhoderick [48].

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_d} + qN_{ss}(V)\right] \tag{13}$$

where W_d is depletion layer width and δ is the thickness of the insulator sheet at the interface. ε_i and ε_s are permittivity of interfacial layer and the semiconductor, respectively. Rearranges of Eq. (13), the N_{ss} can be expressed as follow:

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_d})\right] \tag{14}$$

In addition, for n-type semiconductors, the energy of the N_{ss} as regards the conductance band edge (E_c) at the semiconductor surface can be calculated as

$$E_c - E_{ss} = q(\Phi_e - (V - IR_s)) \tag{15}$$

where the IR_s term is the voltage drop on the device. The energy density distribution profile of N_{ss} with R_s, which was obtained from the forward-bias I–V measurements, has been indicated in Fig. 11 for the changing temperature. It can be seen from Fig. 11 that N_{ss} values has been affected by

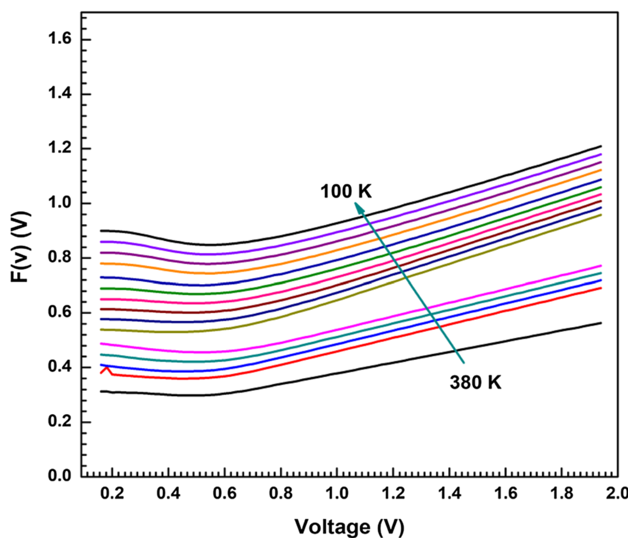

Fig. 10 (online color) $F(v)$–V plots of Au/ZnO/n-Si device changing temperature from 100 to 380 K

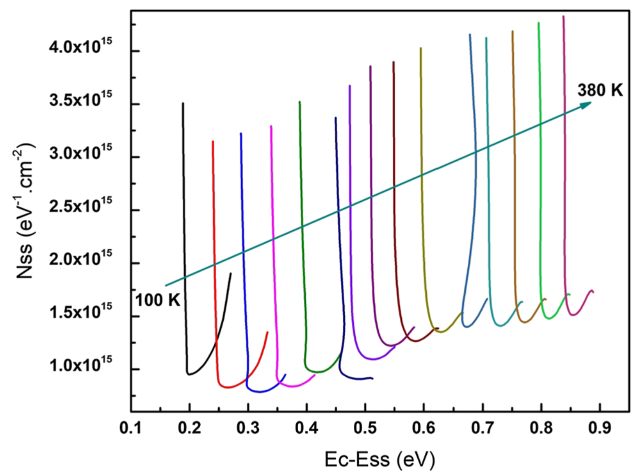

Fig. 11 (online color) N_{ss} versus E_c—E_{ss} plots of Au/ZnO/n-Si device changing temperature

changing temperatures. In addition, relatively higher N_{ss} values can be ascribed to the very thin (10 nm) ZnO interface layer [49, 50]. These results have also advised that the N_{ss} values should be considered as distinguishing parameters for determining properties of the device [51].

4 Conclusion

Au/ZnO/n-Si device was composed by ALD technique as a thin layer ZnO film at the interface, and device was characterized with XRD, SEM and temperature dependent *I–V* measurements. XRD measurements showed that ZnO thin film layer has (002) and (201) orientation peaks which are referred to hexagonal structure of the ZnO layer. SEM images of the device showed that ZnO layer has smooth surface and, Au/ZnO/n-Si device was obtained successfully. Ideality factor and barrier height values were calculated using TE theory for various temperatures. While n values decreased with increasing temperature, Φ_b values increased. These changings at n and Φ_b values confirmed that device was not ideal diode and charge transport mechanism was not just TE. Also, these parameters and R_s values were calculated using Chung's and Norde's methods. The increasing temperature caused generally decreasing R_s values. N_{ss} versus (E_c–E_{ss}) plots have shown that N_{ss} values increased with increasing temperatures. These results have implied that this device can be used for diodes applications in the wide range temperatures.

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