

# Effects of CdCl<sub>2</sub> annealing temperatures on the properties of pulsed laser deposited CdS thin films and CdS/CdTe solar cells

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**Abstract** In this work, a post annealing process in CdCl<sub>2</sub> was applied to improve the quality of pulsed laser deposited CdS films, and the effect of annealing temperature on the quality of CdS films was studied. The research indicated that the grain size of CdS thin films obviously increased after the annealing process, and crystallinity and optical transmission performance of CdS films were enhanced as well. Moreover, the CdTe solar cell with the annealed CdS window layer obtained better performance. The annealing temperature is a significant factor in the annealing process. 420 °C may be an optimistic annealing temperature, since not only the CdS layer annealed at this temperature had good crystallinity and optical transmission performance with a relatively smooth surface, but also the photovoltaic device with this window layer obtained the best performance among all the samples, including higher short-circuit current, open-circuit voltage and efficiency, corresponding to 26.97 mA/cm<sup>2</sup>, 760.80 mV and 12.37% respectively.

## 1 Introduction

In the CdTe thin film solar cell, the window layer plays a crucial role [1]. The window layer must have good optical transmission performance in order to ensure photons pass through the window layer and reach the CdTe absorption layer. Also, the p-type CdTe layer forms the p-n junction with the n-type window layer, and the build-in potential

inside the p-n junction will separate photon-generated electron–hole pairs, which finally result in the photo-voltage [2]. Commonly, CdS, a kind of II–VI compound semiconductor materials with a direct band-gap of 2.42 eV, is utilized as the window layer for the CdTe solar cell [3].

CdS layer is usually deposited via chemical-bath deposition [4–7], thermal evaporation deposition [8, 9] and electro-deposition [10] radio frequency sputtering [11, 12]. In our previous work, the CdS window layer was prepared using pulsed laser deposition and then applied in the CdTe thin film solar cells [13]. However, the performance of the device is not as well as we expected. This is probably because the as-deposited CdS thin film has a relatively rougher surface, smaller crystal size and smaller band gap, which results in poor match with the CdTe layer and further affects the performance of the device after the subsequent deposition of CdTe layer. Consequently, the performance of CdTe solar cells can be promoted via improving the crystallinity, optical properties and surface morphology of the CdS thin films.

A feasible solution is a post annealing treatment on the CdS window layer, which optimize crystal structure and improve thin film crystallinity through a recrystallization process. In addition, annealing can reduce the recombination center and the defects of CdS thin films at grain boundary area, and improve not only the surface roughness but also the optical transmission [14–16].

In this paper, we have studied the influence of annealing treatment on the properties of PLD-CdS films. Due to the annealing temperature in CdCl<sub>2</sub> annealing process is a key parameter, this article focuses primarily on the effects of different annealing temperatures on the performance of pulsed laser deposition CdS thin films as well as CdS/CdTe thin film solar cells.

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## 2 Experimental details

In this work, CdS thin films were obtained using a KrF Excimer Laser (Lambda Physik Compex 201,  $\lambda=248$  nm, pulse duration=20 ns) in the vacuum chamber which is maintained at  $\sim 10^{-5}$  torr utilizing a molecular pump together with a mechanical pump. The substrates were 20 mm×60 mm commercial fluorine-doped tin oxide (FTO, the surface conductivity is  $15 \Omega/\text{cm}^2$ ) glass. The CdS target (purity 99.99%) was installed in a rotating target base and the speed was set as 4 rpm. There is a resistive type heater to heat the substrate, and the temperature was set at 200°C. The pulsed laser energy and frequency was 90 mJ and 6 Hz respectively. The distance between the target and FTO substrate was set as 7 cm. Before deposition, the CdS target was irradiated by pulsed laser for  $\sim 30$  s to remove the oxides and contaminations. Six CdS film samples of 100 nm were deposited under the above-mentioned condition via PLD, and five of these pulsed laser deposited CdS samples were annealed in CdCl<sub>2</sub> atmosphere subsequently under five specific temperatures, which is 380, 400, 420, 440 and 460°C. During the annealing process, CdCl<sub>2</sub> was ultrasonic-sprayed onto the surface of these five CdS layers initially. Then CdS layers were annealed in a tube furnace respectively for 30 min with a flow of 20 sccm N<sub>2</sub> and 20 sccm O<sub>2</sub>.

Optical transmittance spectra were measured using the UV/Vis spectrophotometer (Perkin Elmer-Lambda 950) and X-ray diffraction (XRD) patterns were recorded with Dandong Fangyuan DX-2600 diffractometer using CuK $\alpha$  radiation. Scanning electron microscopy (SEM) (Hitachi S-4800) and Atomic force microscopic (AFM) (Asylum Research MFP-3D) were utilized to monitor surface morphology. X-ray photoelectron spectroscopy (XPS) (Kratos AXIS Ultra DLD) was also applied to analyze surface elemental composition of the six different CdS layers.

CdTe thin film solar cells based on these six PLD-CdS window layers were synthesized by the following procedures. First, CdTe layers were deposited on the six different layers using close-space sublimation (CSS) under the mixture gases of Ar and O<sub>2</sub> maintained at 3 kPa. During deposition, the substrate temperature and the source temperature were 540 and 620°C respectively. The thickness of CdTe polycrystalline layer was about 5–6  $\mu\text{m}$  for 3 min deposition. Next, all the samples were annealed in a tube furnace for 35 min at 385°C under CdCl<sub>2</sub> atmosphere and then corroded using bromine-methanol solution. The cells were completed with the pulsed laser deposition of copper doped zinc telluride

back contact layer and electron beam evaporation of Au electrodes before characterization of the solar cell performance. CdTe solar cells were characterized by current density–voltage (J-V) measurements under an AM 1.5 illumination and external quantum efficiency (EQE) both at room temperature.

## 3 Results and discussion

### 3.1 Atomic force microscopic surface morphology

The instrument for the AFM characterization of CdS samples annealed at different temperatures together with an as-deposited film is Asylum Research MFP-3D, and its measurement range is 2  $\mu\text{m}$ ×2  $\mu\text{m}$ . The summary of surface roughness is shown in Table 1.

As can be seen from Fig. 1, as-deposited PLD-CdS thin films have continuous surface without obvious pinholes. However, the root mean square (RMS) roughness is up to 13.4 nm. After the 380°C annealing treatment, RMS roughness of CdS layer slightly reduce to 13.1 nm. The surface of sample annealed at 400°C is further improved because of grain growth, and RMS roughness drops to 12.2 nm. The RMS roughness of 420°C-annealed sample decreased to 9.1 nm, and the surface has been greatly improved with a flat surface due to the crystal grains further grow up.

However, when the annealing temperature continues to rise up, the surface of CdS sample becomes more roughness instead. RMS roughness even goes up to 18.4 nm when the annealing temperature is 460°C. Obviously, CdS grains are prone to agglomerate when the annealing temperature rises, probably due to the high energy obtained by the atoms after the high-temperature annealing process leads to occur a great degree of diffusion. Since CdS layer always used as the window layer in CdTe thin film solar cells, its surface roughness will have a significant impact on CdTe layer and the performance of the device as a consequence.

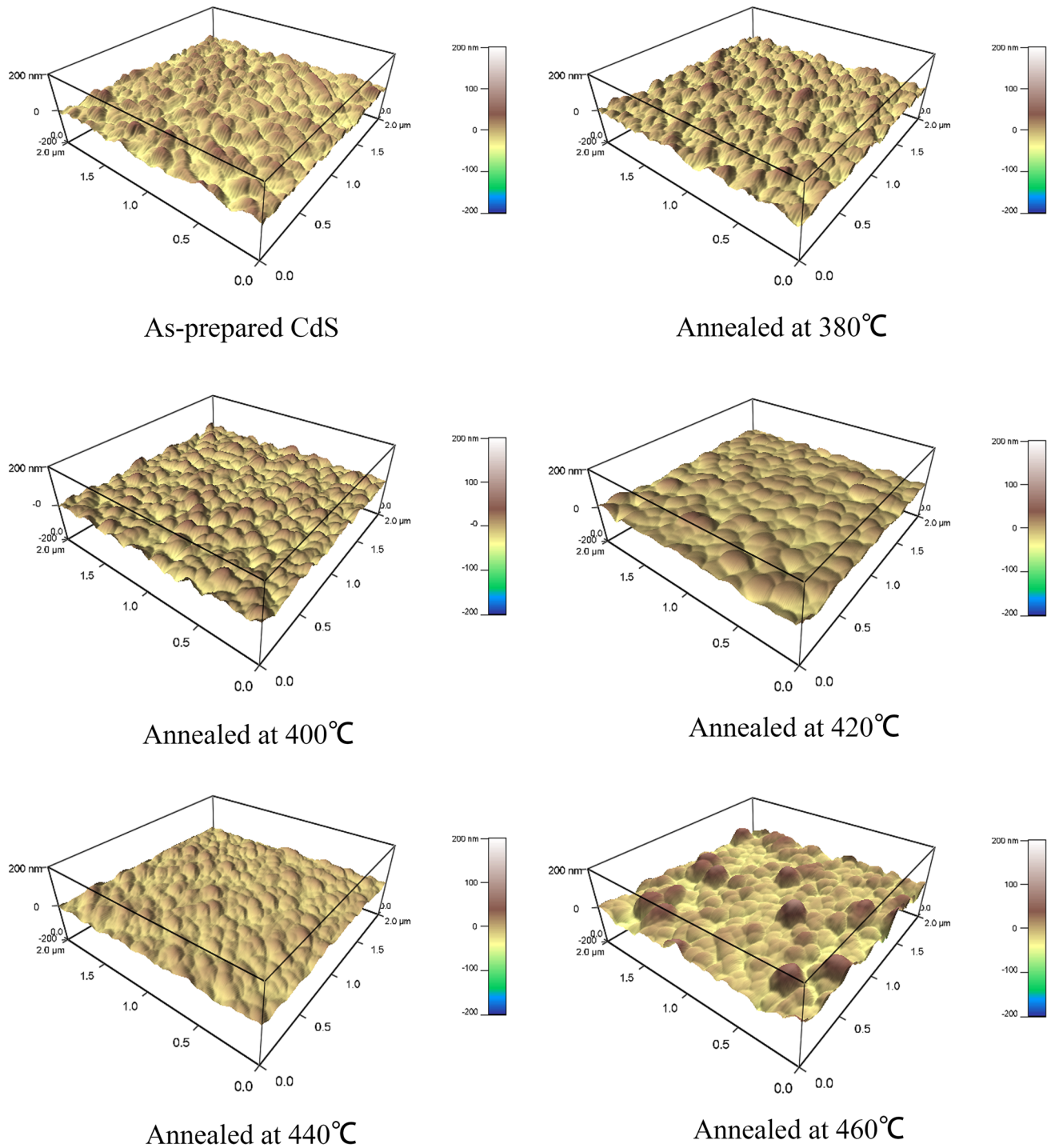
### 3.2 X-ray diffraction

X-Ray diffraction (XRD) pattern of window layer samples annealed at different temperatures were recorded with Dandong Fangyuan DX-2600 diffractometer using CuK $\alpha$  radiation (shown in Fig. 2). The pattern for FTO is also shown in Fig. 3 for comparison.

Diffraction peaks locate at 26.5°, 43.6° and 47.7° are corresponding to (002), (110) and (103) hexagonal-CdS crystal plane, respectively. As can be seen from Fig. 2,

**Table 1** The surface roughness (RMS) of different temperatures annealed together with as-deposited PLD-CdS films

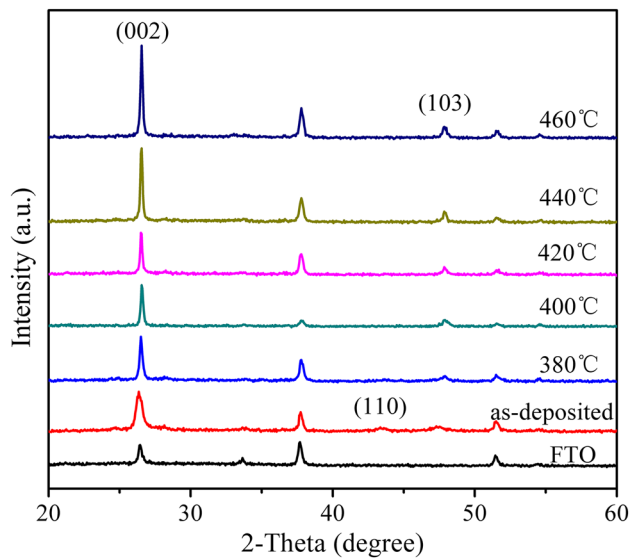
	As-deposited	After annealing				
		380°C	400°C	420°C	440°C	460°C
RMS/nm	13.4	13.1	12.2	9.1	9.8	18.4



**Fig. 1** AFM images of different temperatures annealed together with as-deposited PLD-CdS films

pulsed laser deposited CdS films maintained hexagonal (002) orientation after the annealing process. After  $\text{CdCl}_2$  annealing treatment on CdS thin films, the original (110) diffraction peak disappears, while (002) diffraction peak becomes more intense and sharper, indicates better crystallinity in the CdS film. Furthermore, as

the annealing temperature increases, the peaks intensity ratio of the (002) peak and the (103) peak become larger, meaning that the (002) orientation of the CdS thin films get enhanced with the increment of the annealing temperature. Since the lattice mismatch between hexagonal-CdS (002) crystal plane and cubic-CdTe (111) crystal



**Fig. 2** X-ray diffraction pattern of different temperatures  $\text{CdCl}_2$  annealed and as-deposited PLD-CdS films

plane is the lowest, (002) preferred orientation of the annealed CdS will have a good effect on CdTe layer as well as the performance of the solar cell device.

### 3.3 Scanning electron microscopic surface morphology

Figure 3a–f show the surface morphology images of the as-deposited and annealed CdS layer measured by HITACHI S4800 Scanning Electron Microscope.

In Fig. 3a, the surface of CdS thin film prepared by PLD at 200 °C substrate temperature is relatively compact, but grain size is small with invisible grain boundaries. In Fig. 3b, grain boundaries have emerged, indicating the recrystallization process occurred when annealing at 380 °C, but the grain size is still too small. As the annealing temperature increased to 400, 420, and 440 (Fig. 3c–e), the grain become larger gradually and are about 20–40, 40–50, 80–100 nm, respectively. And first the surfaces get further more smooth, then, the surface roughness gets the trend of rise. At the annealing temperature of 460 °C (Fig. 3f), transverse grain size of CdS thin films rise to even more than 100 nm, and the surface roughness even deteriorate further, which is corresponding to AFM tested results. In conclusion, it's unnecessary for the annealing temperature of CdS thin film to rise too high. On the contrary, the surface morphology would be damaged, if the annealing temperature rose to some extent.

### 3.4 Ultraviolet–visible transmission spectra and spectral absorption coefficient

UV spectrum of samples measured by the Lambda 90 UV/VIS/NIR spectrophotometer, and is shown in Fig. 4.

When annealing temperature is 380, 400 and 420 °C, the transmittance of CdS samples has been greatly improved in the wavelength range of 500–700 nm compared with the as-deposited one, reflecting the reduction of defects inside films to some extent. Moreover, transmittance of annealed samples in the short-wave region (<500 nm) has been improved, rendering more short-wave region photons entering into the absorption layer of CdTe solar cell and finally promote the battery shortwave response. Another effect of the annealing is the blue shift of the absorption edge. Since the location of absorption edge is mainly determined by the band gap ( $E_g$ ), this result clearly shows that the band gap of CdS changes after  $\text{CdCl}_2$  annealing treatment.

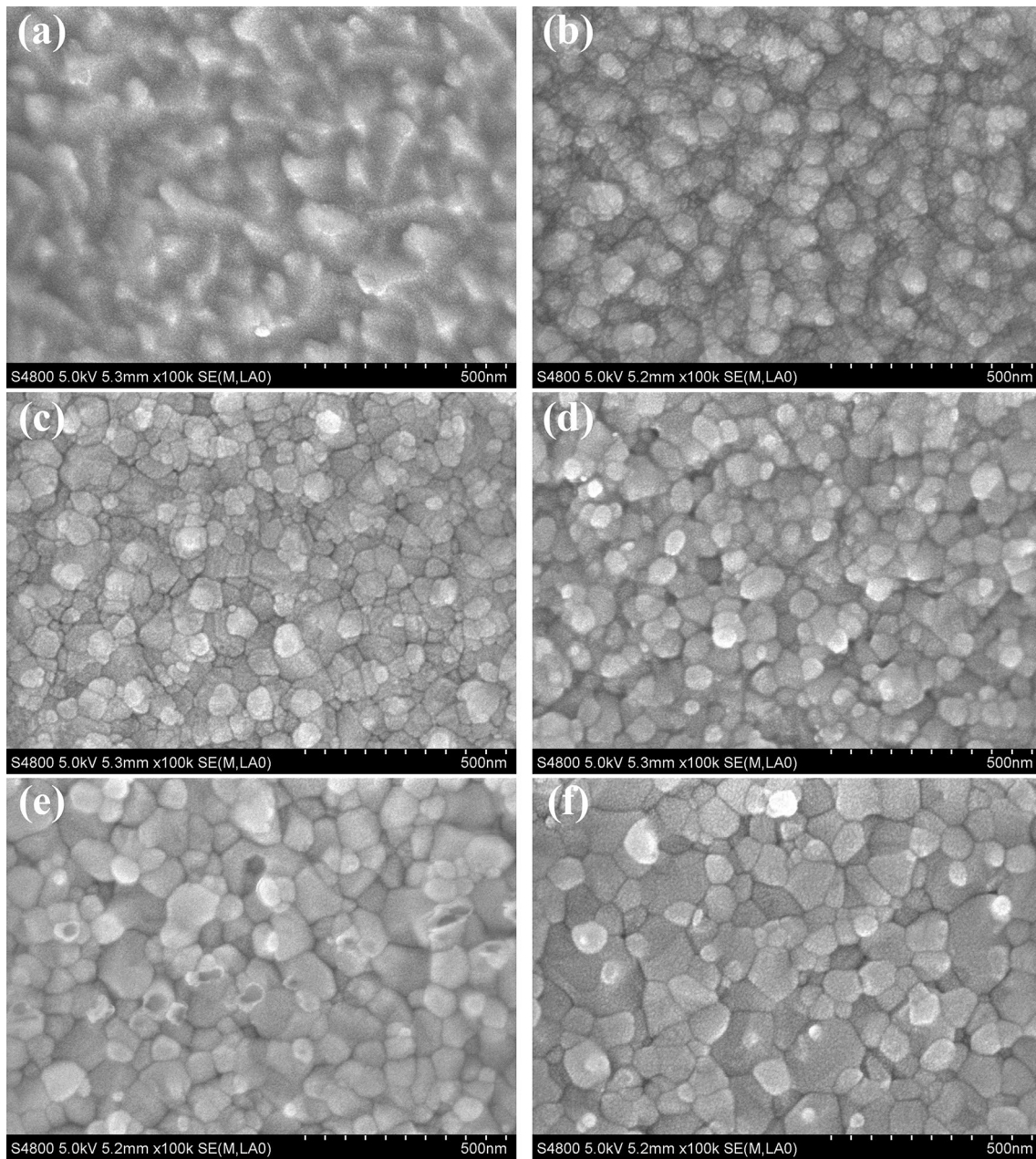
CdS is a direct band gap semiconductor,  $(ah\nu)^2 \sim h\nu$  (Fig. 5) using Tauc mapping and the curve tangent line extends to the X-axis, the intercept is the band gap of CdS thin film samples. The band gap of as-deposited CdS sample is only about 2.35 eV. After annealing treatment at 380, 400 and 420 °C, the band gap approximately rises to 2.43, 2.43 and 2.44 eV respectively. However, when annealing temperature rises to 440 and 460 °C, the band gap relative to the first three samples even approximately declines to 2.43 and 2.42 eV respectively.

### 3.5 X-ray photoelectron spectroscopy

X-ray photoelectron spectra (XPS) were measured using the Kratos AXIS Ultra DLD. Ar ion sputtering is used on all samples to remove the contaminations on the surface at first. Due to the weak ion energy, there would be no obvious damage on the CdS surface. After ion sputtering treatment, only a weak carbon signals can be detected from survey scans, which is utilized for calibration of XPS spectra.

The survey scan spectra are shown in Fig. 6. From the survey scan spectra, all samples are consisted of Cd and S atoms. However, Cl peak does not appear on the survey scan spectra. The absence of Cl peak indicated Cl atoms were not doped into the pulsed laser deposited CdS layer through the  $\text{CdCl}_2$  annealing process.

Figure 7 shows Cd 3d core level spectra. Cd 3d<sub>3/2</sub> and 3d<sub>5/2</sub> peaks of as-deposited CdS sample locate at 411.90 and 405.14 eV respectively. After annealing at 380, 400 and 420 °C, the position of Cd 3d<sub>3/2</sub> peak and 3d<sub>5/2</sub> peaks are not substantially changed. However, when the annealing temperature increased to 440 °C, especially 460 °C, Cd 3d<sub>3/2</sub> peak and 3d<sub>5/2</sub> peak shift a little to the lower binding energy direction. The fitted Gaussian peaks of Cd 3d peaks from the CdS sample annealed at 460 °C are

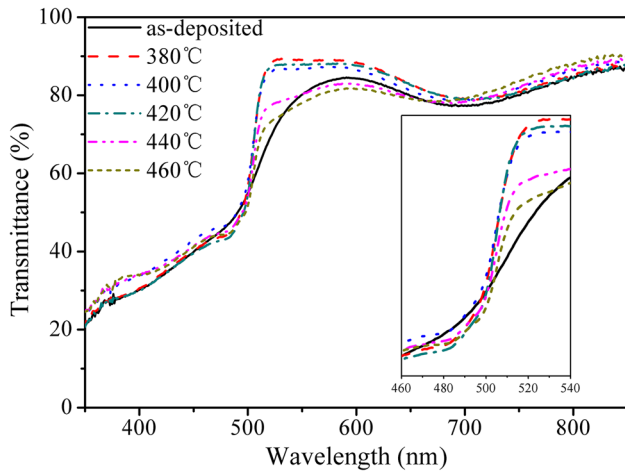


**Fig. 3** SEM images of different temperatures annealed and as-deposited PLD-CdS films. **a** 200 °C as-deposited, **b** CdCl<sub>2</sub> annealing at 380 °C, **c** CdCl<sub>2</sub> annealing at 400 °C, **d** CdCl<sub>2</sub> annealing at 420 °C, **e** CdCl<sub>2</sub> annealing at 440 °C, **f** CdCl<sub>2</sub> annealing at 460 °C

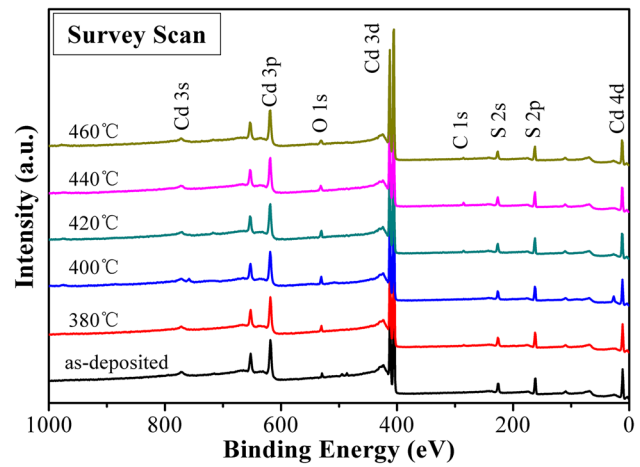
shown in Fig. 8. According to relevant literature [17, 18], the two peaks positioned at 410.55 and 403.83 eV belong to Cd 3d<sub>3/2</sub> peak and 3d<sub>5/2</sub> peak of CdO respectively. The emergence of CdO may be due to partial oxidation during high temperature annealing treatment on CdS thin films. Also it can be speculated that partially oxidation of CdS layer annealed at 440 and 460 °C is one of the reasons leading optical transmittance (Fig. 4) and band gap (Fig. 5) to decline.

### 3.6 Energy conversion efficiency

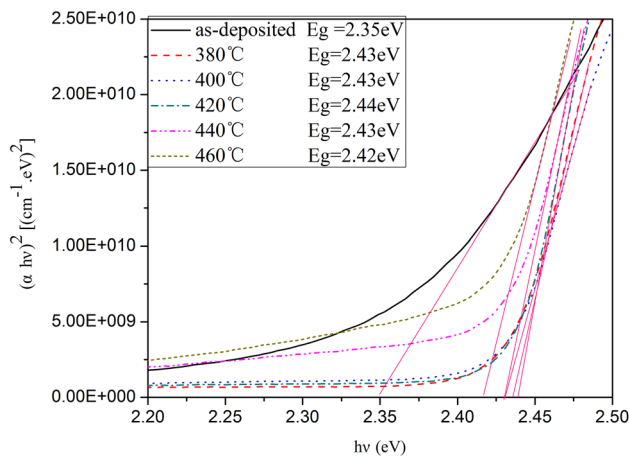
CdS thin films with annealing treatment as window layers were applied on CdTe solar cells, which were tested using a Solar Cell Tester (Gsolar XJCM-9) under AM1.5 and 25 °C. Figure 9 provides the J-V curves of the dot cell with the best performance of each sample, and the associated performance parameters are summarized in Table 2.



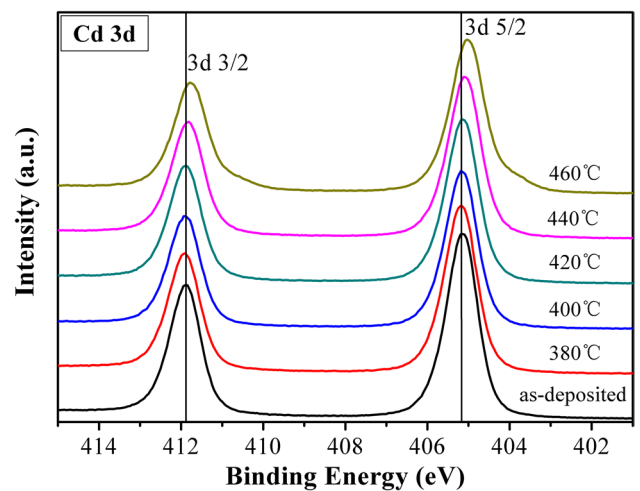
**Fig. 4** Optical transmittance spectra of different temperatures annealed together with as-deposited PLD-CdS films



**Fig. 6** XPS spectra of different temperatures CdCl<sub>2</sub> annealed together with as-deposited PLD-CdS films



**Fig. 5** Re-plotted  $(\alpha h\nu)^2 \sim h\nu$  curves of different temperatures annealed together with as-deposited PLD-CdS films

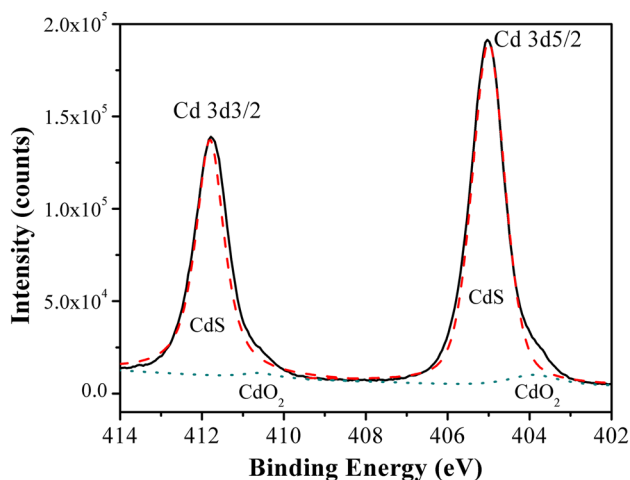


**Fig. 7** Cd 3d core levels of different temperatures CdCl<sub>2</sub> annealed and as-deposited PLD-CdS films

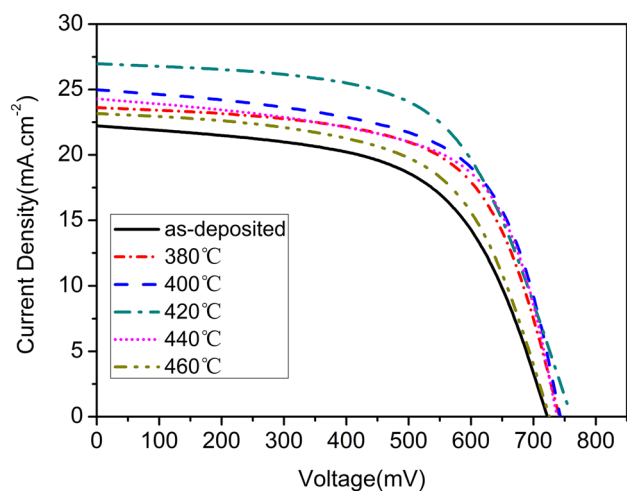
CdTe solar cell with as-deposited CdS window layer obtains only 8.59% energy conversion efficiency, due to lower  $V_{OC}$ ,  $J_{SC}$  and FF. After the CdS layer was annealed, the performance of CdTe cells with CdS window layers annealed at different temperatures has changed in different degree. The dot cells showed a better performance when annealing temperature were 380, 400 and 420 °C. The energy conversion efficiency was increased to 10.98, 11.51 and 12.37% respectively.  $J_{SC}$  was increased to 23.62, 24.9 and 26.97 mA/cm<sup>2</sup> respectively.  $V_{OC}$  was rose to 741.48, 742.9 and 760.80 mV respectively, and FF% also to 62, 62 and 63. The main reason combined with these test results took earlier is that the recrystallization of CdS film after CdCl<sub>2</sub> annealing leads to the grain grow up, the crystalline quality be improved, and reduce grain boundaries and defects in the lattice, thus effectively reduce the

photo-generated carrier recombination. Meanwhile, the improved of crystalline quality enhances optical transmission, especially for the short wavelength region, thereby promotes shortwave response to some extent. The surface roughness of CdS film annealed at 380,400 and 420 °C was improved obviously, thus reduced flaws at CdS/CdTe interface. Above all of these contribute to improving  $J_{SC}$  and  $V_{oc}$ .

However, the performances of the best dot cells with 440 °C-annealed and 460 °C-annealed window layer are declined, as compared to its 420 °C counterparts, especially 460 °C-annealed window layer. The performance of cell is relatively dropped from previous analyzing because of the following reasons. One is relatively lower shot wave optical transmission of CdS window layer annealed at 460 °C



**Fig. 8** Cd<sub>3d3/2</sub> and Cd<sub>3d5/2</sub> with the Gaussian peak fitting of CdS thin films at 460 °C annealed



**Fig. 9** J-V curves of the best dot cell on the six samples with different temperatures CdCl<sub>2</sub> annealed and as-deposited PLD-CdS window layers

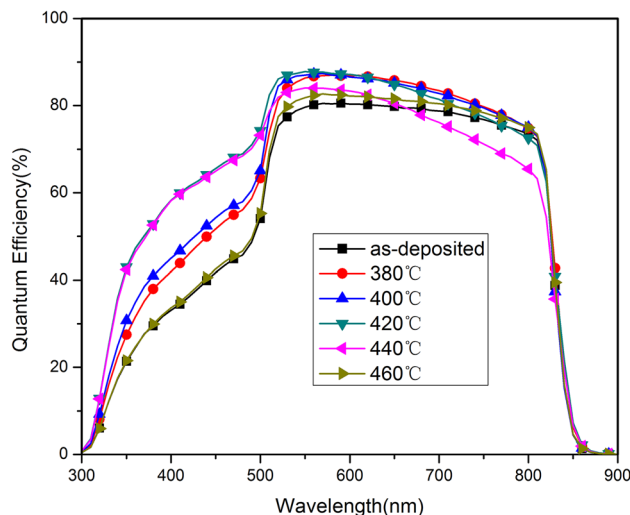
leading to wake shot wave response. Another is CdS surface roughness becomes heighten due to that part of the surface reunites after 460 °C annealing, and further leads to generate defects at CdS/CdTe interface. These defects eventually become trapping centers. As a result, depletion region carrier compounds are enlarged. So, from the experimental results it can be concluded that the best performance of CdS/CdTe thin film solar cell was obtained by using 420 °C annealed CdS thin film as window layer.

**3.7 External quantum efficiency**

Figure 10 presents the EQEs of the dot cell on the six samples. For the six dot cells, the EQE exhibits an

**Table 2** Main performance parameters of the best dot cell on the six samples with different temperatures CdCl<sub>2</sub> annealed and as-deposited PLD-CdS window layers

Sample	Efficiency (%)	V <sub>OC</sub> (mV)	J <sub>SC</sub> (mA/cm <sup>2</sup> )	FF (%)
As-deposited	9.41	722.24	22.22	59
Annealed at 380 °C	10.98	741.48	23.62	62
Annealed at 400 °C	11.51	742.91	24.98	62
Annealed at 420 °C	12.37	760.80	26.97	63
Annealed at 440 °C	11.22	738.03	24.29	63
Annealed at 460 °C	10.09	725.48	23.17	60



**Fig. 10** The EQEs of the dot cell on the six samples with different temperatures CdCl<sub>2</sub> annealed and as-deposited PLD-CdS window layers

average quantum efficiency of 80–87% in the range of 500–800 nm, one of the biggest distinguish is in the range of 300–500 nm. As can be seen from Fig. 10, the dot cell showed a better EQE when the annealing temperature were 420 °C. The better shot wave response, the better energy conversion efficiency the dot cells will have. Meanwhile, if the dot cell has much more shot wave absorption, the J<sub>sc</sub> of the dot cell will be higher. The shot wave absorption decreased obviously when the annealing was 460 °C, reflecting the surface of CdS roughness leads to exist lots of defects in CdS/CdTe interface. Which can capture the charge carriers leading to the carriers can't be valid collected by electrode.

## 4 Conclusions

In summary, this research indicated that the grain size of CdS thin films obviously increased after the annealing process, and crystallinity and optical transmission performance of CdS films were enhanced as well. Moreover, the CdTe solar cell with the annealed CdS window layer obtained better performance. In addition, the annealing temperature is a significant factor in the annealing process. At relatively high annealing temperature, agglomeration occurred at parts of the film surface, leading to a rougher surface as a result. Taking this discussion into consideration, 420 °C may be an optimistic annealing temperature, since not only the CdS layer annealed at this temperature had good crystallinity and optical transmission performance with a relatively smooth surface, but also the photovoltaic device with this window layer obtained the best performance among all the samples. And the best efficiency of the dot cell is 12.37%.

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