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Impact of tunneling conductance on the performance of multi walled carbon nanotubes as VLSI interconnects for nano-scaled technology nodes

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Abstract Multi walled carbon nanotube (MWCNT) has received most of the attention for their unique characteristics as a possible alternative for copper as a VLSI interconnects for future integrated circuits. Multiple equivalent single-conductor circuit (ESC) models are reported in the literature for analysis of MWCNT as an interconnect, however most of them have neglected the impact of intershell tunneling conductance on the performance of MWCNT as interconnect. In this paper, a model is proposed for deriving equivalent impedance parameters by including tunneling conductance in order to study the impact of intershell tunneling conductance on the performance of MWCNT interconnect in terms of delay. Based on the derived equivalent impedance parameters, existing ESC model is modified. Further, the analytical and simulated results obtained from proposed model are compared with the results of existing models. It is revealed from the comparative analysis that the tunneling conductance has considerable impact on the impedance parameters and the propagation delay of an MWCNT bundle interconnect at variable interconnects length for nano-scaled technology nodes i.e. 32, 22 and 16 nm.

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1 Introduction

Carbon nanotubes (CNT) are hollow cylindrical tubes with its diameter in nanometers formed by rolling of graphene sheets. Based on the directions in which a CNTs is rolled, different chirality arrangements observed are armchair (metallic), zigzag (mostly semiconductor) or chiral (mostly semiconductor) [1, 2]. The CNT as an interconnect possesses highly desirable properties, which is its current carrying capacity, high thermal conductivity, high thermal mechanical stability and long mean free path (MFP) [3–5]. Based on number of shells CNTs are divided into single walled CNT (SWCNT) which is single shell CNT and multi walled CNT (MWCNT) which has multiple shells arranged in a concentric cylindrical tube form with each adjacent shell separated by a Van der Waal distance of 0.34 nm [6–8].

The major drawback of SWCNT is its complex and uncontrollable growing process due to which the growth type can either be metallic or semiconductor and this cannot be determined beforehand. SWCNTs with metallic chirality are better conductor than copper, but this is not true with semiconductor chirality. To avoid this uncertainty, MWCNT bundle are the better alternative as interconnects which always acts as metal conductor irrespective of its chirality [9–12]. The electrical properties of MWCNTs is similar to that of metallic SWCNTs for global interconnects length. Thus, MWCNTs are preferred over SWCNT as they are easy to fabricate and provides better control on its growth process, whereas SWCNT structure is simple and can be modeled more easily when compared with MWCNT. However, few models have been proposed in the literature for the better study of MWCNT bundle as an interconnect [13–20].

An MWCNT bundle consists of several shells like SWCNTs with varying diameter are nested concentrically

inside one another and two adjacent shells of MWCNT bundle are separated with the Van der Waals distance i.e. 0.34 nm. The intershell interaction between two adjacent shells of MWCNT is caused due to intershell tunneling where tunneling is a quantum phenomenon which comes into effect when a particle travels through a forbidden region neglecting the laws of classical physics [4, 11, 12]. When a thin film of insulator is placed between two conductors and an electron of one conductor tries to tunnel through this thin insulator to reach the other conductor is known as tunneling. The intershell interaction due to this tunneling conductance has a considerable impact on the performance of MWCNT bundle as an interconnect [13–15]. Most of work reported in the literature, has ignored the impact of intershell tunneling conductance for MWCNT bundle as an interconnect. This paper analyzes the impact of intershell tunneling conductance of adjacent shells of a MWCNT bundle and proposed an ESC model to evaluate of its performance in terms of impedance parameters and propagation delay. Further, a similar analysis is also performed for the model without considering the tunneling impact and results are compared with proposed ESC model for MWCNT bundle as an interconnect for variable lengths at 32, 22 and 16 nm technology nodes [11–16].

This paper focus on the intershell tunneling conductance for electrical transport in MWCNT bundle interconnect. An equivalent impedance circuit model of MWCNT bundle is presented in Sect. 2 of the paper. Section 3 presents the impact of intershell tunneling conductance on the impedance parameters and a Multiple Conductor Circuit (MCC) model for MWCNT bundle interconnects is presented. Realization of ESC model from proposed MCC model including the tunneling conductance is presented in Sect. 4. The impact of intershell tunneling conductance on the performance of MWCNT bundle terms of impedance parameters and propagation delay is analyzed in Sect. 5 and outcomes from the results are summarized in Sect. 6.

2 Modeling of MWCNT

An isolated MWCNT is placed onto an infinite ground plane as shown in Fig. 1 with the outermost shells diameter $D_{\max}$, innermost shells diameter $D_{\min}$, separation between outermost shell and the ground is Y, where adjacent shells are separated by a Van der Waal distance ($d = 0.34$ nm) [7].

2.1 Parameters of MWCNT bundle

Every shell in MWCNT has multiple conducting channels which provide the path for an electron to flow. These

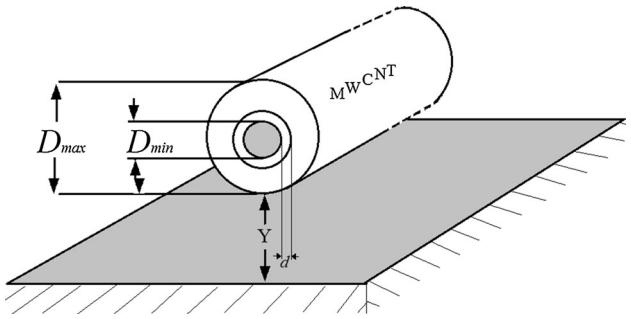

Fig. 1 MWCNT structure on a ground plane [8]

conducting channels are formed due to the spin and sublattice degeneracy of electron in MWCNT [7, 8]. The equation for number of conducting channels in an individual shell is given as

$$N_{shell}(D_j) \approx a \cdot D_j + b, \quad for\, D_j > 3\,\text{nm} \tag{1}$$

where D_j is the diameter of any jth shell of MWCNT bundle, $a = 0.0612\ \text{nm}^{-1}$, and $b = 0.425$. The ratio between $D_{\min}$ and $D_{\max}$ is known as diameter ratio and has a range from 0.3 to 0.8 and it is considered for this work is 0.5. The number of shells (p) in a MWCNT bundle [8] is obtained by

$$p = 1 + Inter\left[\frac{D_{\max} - D_{\min}}{2 \cdot d}\right] \tag{2}$$

where "Inter[·]" refers that the integer part is only considered, d denotes the Van der Waals gap i.e. the minimum distance between two adjacent shells.

The number of shells are counted from the outermost shell towards the innermost shell and ranges from 1, 2,…, j up to p (innermost shell), the diameter of any jth shell is:

$$D_j = D_{max} - 2d \cdot (j-1), \quad 1 \le j \le p \tag{3}$$

where, the diameter of the outermost shell is technology dependent and will be equal to the width of the technology node [8–13].

2.2 Impedance parameters of an individual shell in MWCNT bundle

The impedance parameters of an individual shell of metallic MWCNT are discussed on the basis of its electrical equivalent circuit. Based on different interconnect impedance parameters such as resistance, capacitance and inductance, the impedance model of an individual shell for MWCNT is shown in Fig. 2 [8].

2.2.1 Resistance

Resistance arises in a conducting material when electrons while moving inside a conducting medium gets scattered

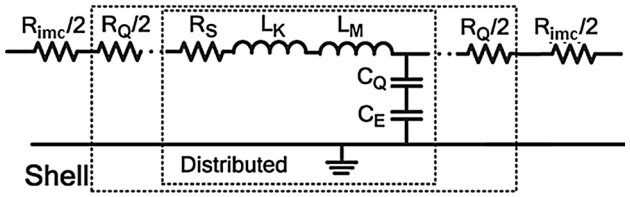

Fig. 2 Equivalent electrical circuit model for a shell of MWCNT [8]

due to impurities or defects. The fundamental resistance (R_F) of a shell of MWCNT mainly arises due to contact quantum resistances (R_Q) and scattering resistances (R_S). A contact quantum resistance arises due to ballistic transport phenomena i.e. when the mean free path (λ) of electron is larger than the length of the medium, the electrons alters their motion due to collisions with walls and fundamental resistance (R_F) depends only on contact quantum resistances (R_Q). However, the scattering resistance (R_S) is considered for the interconnects having the interconnect length greater than the electrons MFP [8, 18] and is distributed along the length of the interconnect. Therefore, the fundamental resistance (R_F) of an individual shell [7, 8, 17, 19] is given as

$$R_F = R_Q + R_S \cdot L = \frac{h}{2e^2 N} + \frac{h}{2e^2 N} \cdot \frac{L}{\lambda} \tag{4}$$

where, $h/2e^2 \sim 12.9\ \text{k}\Omega$, and L, N, λ are the length, conducting channels and MFP of an individual shell of MWCNT respectively. However, practical observations show that the resistance value of interconnect is greater than the resistance of a shell of MWCNT calculated using Eq. 4. This is the due to the effect of imperfect contact resistance (R_{imc}), as it adds to the resistance of a shell and increasing the overall resistance of the interconnect. It is reported in the literature that R_{imc} in MWCNT could be small (i.e. 2–20 kΩ) compared to the equivalent resistance for global lengths. The MFP depends on the diameter of the shell and is considered as $\lambda \approx 1000D$ [8].

2.2.2 Inductance

MWCNT contains magnetic inductance (L_M) caused by the magnetic field formed by an isolated current carrying wire of diameter D_j placed at Y distance above ground plane (as shown in Fig. 1) and kinetic inductance ($L_{K/channel}$) caused due to the kinetic energy stored in a conducting channel [8]. Each shell of MWCNT has N parallel conducting channels which forms effective kinetic inductance ($L_{K/shell}$) for each shell [8]. The per unit length expression for magnetic inductance (L_M), kinetic inductance ($L_{K/channel}$) and effective kinetic inductance ($L_{K/shell}$) are given as

$$L_M = \frac{\mu}{2\pi} \cosh^{-1}\left(\frac{2Y}{D_j}\right) \tag{5}$$

$$L_{K/channel} = \frac{h}{2e^2 v_F} \times \frac{1}{2} \tag{6}$$

$$L_{K/shell} = \frac{L_{K/channel}}{N}. \tag{7}$$

It is seen that magnetic inductance (in pH/μm) is negligible small as compared to kinetic inductance (in nH/μm) [8].

2.2.3 Capacitance

In CNTs different capacitance are quantum capacitance (C_Q), coupling capacitance (C_S) and electrostatic capacitance (C_E). Quantum capacitance ($C_{Q/channel}$) is due to quantum electro-static energies stored within a channel of CNT while carrying current. Each shell of CNT has 'N' parallel conducting channels therefore contributing to form an effective quantum capacitance ($C_{Q/shell}$) for each shell [8, 17, 19]. The per unit length expression C_Q (in aF/μm) is

$$C_{Q/channel} = 2 \times \frac{2e^2}{v_F} \tag{8}$$

$$C_{Q/shell} = C_{Q/channel} \times N. \tag{9}$$

Now, electrostatic capacitance (C_E) is obtained by treating the nanotube as a thin cylindrical conductor of diameter 'D_{max}' (outermost shell), placed at a 'Y' distance above ground plane (Fig. 1).

$$C_E = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{2Y}{D_{\max}}\right)} \quad \text{for} \quad Y > 2.d \tag{10}$$

As MWCNT bundle consists of several graphene sheets, arranged in parallel to one another which is folded to form concentric shell such that each shell has a different diameter, which translate to different number of channel and different MFPs, resulting in different circuit parameters. Therefore, the parameters of each shell of MWCNT cannot be combined in a simple way as in case of SWCNT. Moreover, the potentials of different shells cannot be assumed to be equal as circuit parameters of each shells vary with one another in MWCNTs, and therefore shell-to-shell coupling capacitance (C_S) is induced [8, 17]. The value of coupling capacitance (C_S) is quite large due to the small separation between adjacent shells. Therefore, in order to obtain shell-to-shell capacitance per unit length (Cs) there is a need to use the coaxial capacitance equation as given by

$$C_S = \frac{2\pi\varepsilon}{\ln\left(\frac{D_{Out}}{D_{In}}\right)} \tag{11}$$

where, D_{In} and D_{Out} are the diameters of the inner and outer shells of adjacent coaxial shells.

2.3 Multiple conductance circuit of MWCNT bundle

Based on the impedance parameters, the equivalent multiple conductor circuit model (MCC) for MWCNT bundle interconnect is shown in Fig. 3.

3 Intershell interaction

Intershell interaction in MWCNT is caused due to intershell tunneling where tunneling is a quantum phenomenon which comes into effect when a particle travels through a forbidden region neglecting the laws of classical physics [4]. In other words, in classical physics electrons move through conductors only and not through insulators, however if a thin film of insulator is placed between two conductors, the electrons can tunnel through one conductor to reach the other conductor. This happens due to extended wave function of the conductors into the insulating layer.

In a MWCNT shell, each carbon atom contains four valance electrons, three are tightly bonded by the neighboring carbon atoms while the fourth electron (called π-orbital electron) is independent and moves freely contributing to the conduction phenomena of CNT. In MWCNT adjacent shells are separated by a small Van der Waal distance ($d \approx 0.34$ nm), this causes π-orbital overlap resulting in intershell interaction caused due to intershell tunneling or hopping [5]. These intershell interactions are responsible for electromagnetic propagation in MWCNT [14].

3.1 Intershell tunneling conductance

In MWCNT bundle, ideally the two adjacent shells are insulated and separated by a small distance 'd', but when the electrons in a shell get excited it crosses the small distance 'd' reaching to the adjacent shell and thus creating a conductive path between two shells. As the conductive path is due to the tunneling of electrons from one shell to another and therefore the conductance introduced is called intershell tunneling conductance [5] and is given by

$$G_{T_j} = \frac{\sigma}{d} \cdot \pi D_j \quad for\,(j = 1, 2, \ldots p-1). \tag{12}$$

In this σ is tunneling conductivity $(\Omega\ \mathrm{m})^{-1}$ and D_i is the outer shell diameter of the two adjacent shells of a MWCNT bundle. The σ/d is called as normalized tunneling conductivity and for $d = 0.34$ nm its given as 0.3 $(\mu\Omega\ \mathrm{cm}^2)^{-1}$ [8]. It is reported in the literature that there is considerable tunneling conductance impact on the performance if the distance between the two adjacent shell 'd' is nearly less than or equal to the Van der Waal distance ($d \leq 0.34$ nm). The intershell distance in this paper is considered equal to Van der Waal distance, therefore the impact of tunneling conductance is non-negligible [14].

3.2 Tunneling conductance dependent multiple conductance circuit of MWCNT bundle

Based on the above parameters, tunneling conductance dependent equivalent multiple conductor circuit model (MCC) for MWCNT bundle interconnect is shown in Fig. 4. The figure shows that all the individual shells are considered as parallel shells.

4 Realization of ESC model from MCC model

The tunneling conductance dependent multiple conductor circuit (MCC) as shown in Fig. 4, needs to be converted into equivalent single conductor (ESC) model to evaluate the performance of MWCNT bundle [18]. In Fig. 4, p represents the total number shells of MWCNT bundle and each shell of the bundle is connected in parallel to each other.

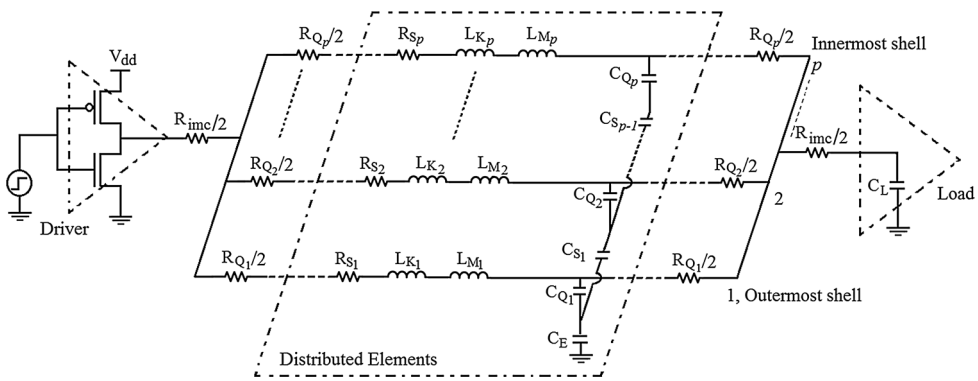

Fig. 3 MCC model of a p shell MWCNT bundle [8]

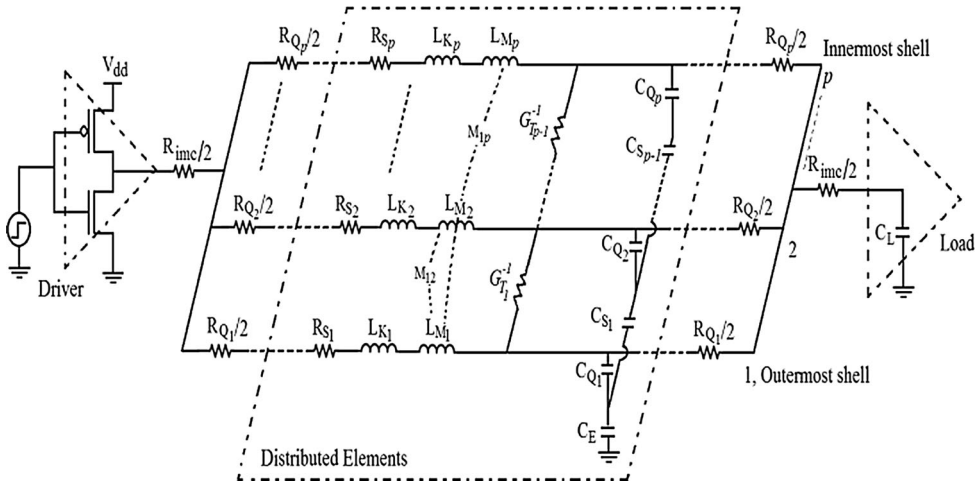

Fig. 4 MCC model of p number of shells MWCNT with tunneling conductance [8, 17]

4.1 Realization of ESC resistance with tunneling conductance

To evaluate tunneling conductance dependent ESC resistance model MWCNT bundle from the multiple conductor circuit (MCC) model proposed as shown in Fig. 4, is needs to be realized in simplified circuit as shown in Fig. 5.

In order to obtain equivalent resistance considering tunneling. Let,

$$R_{SS}(j) = R_S(j) + R_Q(j)/2 \tag{13}$$

where, $R_S(j)$ and $R_Q(j)$ are the scattering and quantum resistances of jth shell of an MWCNT bundle. The equivalent resistances are to be calculated using Star to Delta transformation technique and given as [11–14]. Assume,

$$R_a(1) = R_{SS}(1) \quad \text{and} \quad R_b(1) = R_Q(1)/2 \tag{14}$$

$$\Delta R(j) = R_a(j) \times G_T^{-1}(j) + R_a(j) \times R_b(j) + R_b(j) \times G_T^{-1}(j) \qquad j = 1, 2 \ldots p \tag{15}$$

Now applying Star to Delta transform as shown in Fig. 6,

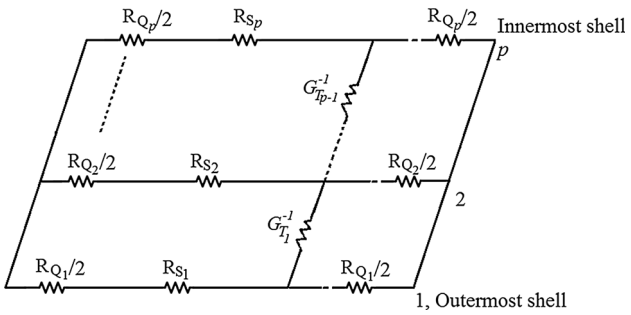

Fig. 5 Realization of equivalent resistance circuit model including tunneling conductance for an MWCNT bundle

$$R_X(j) = \frac{\Delta R(j)}{R_b(j)}, \quad R_Y(j) = \frac{\Delta R(j)}{R_a(j)}, \quad R_Z(j) = \frac{\Delta R(j)}{G_T^{-1}(j)} \tag{16}$$

$$\begin{cases} R_a^{-1}(j+1) = R_{SS}^{-1}(j+1) + R_X^{-1}(j) \\ R_b^{-1}(j+1) = R_Q^{-1}(j+1) \big/ 2 + R_Y^{-1}(j) \end{cases} \tag{17}$$

where $j = 1, 2 \ldots p$.

$$G_Z = \sum_{j=1}^{p-1} R_Z^{-1} \tag{18}$$

Therefore, the equivalent resistance for MWCNT bundle as single conductor resistance including tunneling conductance (R_T) is given as.

$$R_T^{-1} = \left(R_a(p) + R_b(p)\right)^{-1} + G_Z \tag{19}$$

Therefore, using the Eq. 19, the equivalent single conductor resistance with tunneling conductance (R_T) can be obtained.

4.2 Realization of ESC capacitance with tunneling conductance

The calculation of equivalent single conductor (ESC) capacitance for a MWCNT bundle is slightly difficult and has to be done in parts [18]. To obtain ESC capacitance for an MWCNT bundle, a simplified circuit is shown in Fig. 7.

Let $\overline{C}_Q$ be equivalent capacitance, C_Q is quantum capacitance and C_S is scattering capacitance [18].

$$\overline{C}_Q = C_1 \tag{20}$$

where C_1 is calculated in a recursive way.

$$C_p = C_{Qp} \tag{21}$$

$$C_{j-1} = \left(C_j^{-1} + C_{S(j-1)}^{-1}\right)^{-1} + C_{Q(j-1)} \quad for\ (j = p \ldots, 3, 2) \tag{22}$$

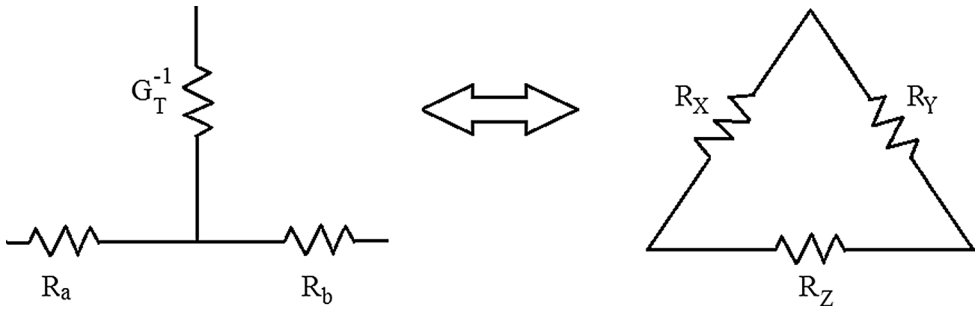

Fig. 6 Star–Delta transformation

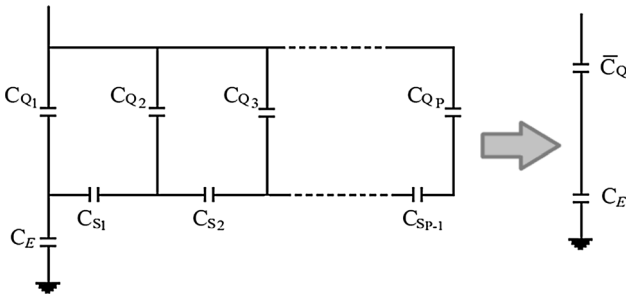

Fig. 7 Realization of ESC capacitance of an MWCNT bundle [18]

The values obtained are put in ESC model as shown in Fig. 2 and the obtained circuit is simulated. The total capacitance in ESC model is taken as:

$$C = \left(C_1^{-1} + C_E^{-1}\right)^{-1}. \quad (23)$$

The equivalent single conductor inductance is the sum of all the parallel combinations of magnetic inductance (L_M) and kinetic inductance (L_K) of all the shells and given as

$$L^{-1} = \sum_{j=1}^{p} \left(L_{Kj} + L_{Mj}\right)^{-1} \quad for\,(j = 1, 2, \ldots p). \quad (24)$$

5 Results and discussion

This paper presents the impact of tunneling conductance on performance of MWCNT bundle as interconnect in terms of impedance parameters and propagation delay. The conducting channels in a shell of MWCNT and number of shells in MWCNT bundle depend upon the technology node as the diameter of outermost shell (D_{max}) of MWCNT bundle will be equal to the width of the interconnect as shown in Fig. 8b. Hence, the conducting channels of an individual shell and number of shells in MWCNT bundle for different interconnects lengths at 32, 22 and 16 nm technology nodes are calculated using Eqs. 1–3. The equivalent impedance parameters without considering the tunneling conductance of MWCNT bundle are obtained by using the Eqs. 4–11. All the interconnect parameters used for calculations are obtained from International Technology Roadmap for Semiconductors, 2013 Edition (ITRS-2013) based simulation parameters [16], as summarized in Table 1. Further, the calculations for impedance parameter of proposed ESC model which include the impact of tunneling conductance on MWCNT bundle are obtained using ESC model Eqs. 12–24. All the impedance parameter calculations are obtained by writing the script in MATLAB. Based on these impedance parameters, a simulation setup is used to evaluate the propagation delay using SPICE simulation tool as shown in Fig. 8a. A CMOS inverter based driver interconnects load structure (*DIL*) is used for the interconnect to achieve its fast switching, small size and moderate noise margin, C_L depicts the input capacitance of the fan-out gates acting as a load to the interconnect line [19, 20, 21]. The basic interconnect structure with DIL is shown in Fig. 8a.

The results obtained from above mentioned calculations are shown in Table 2 which represents the ESC resistance of MWCNT bundle interconnects with and without tunneling conductance impact for variable interconnects length ranging from 100 to 3000 μm at 32, 22 and 16 nm technology nodes. The impact of mutual inductance is still

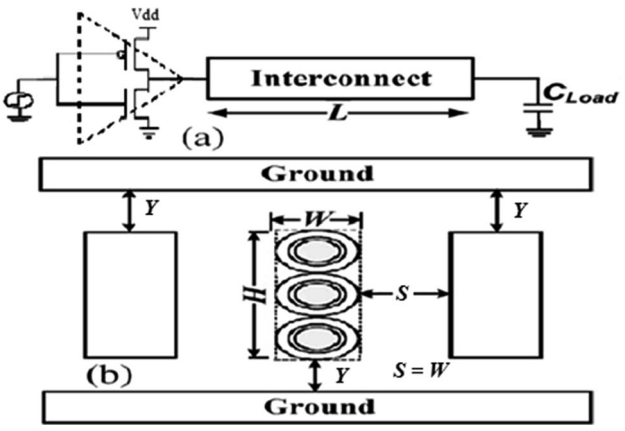

Fig. 8 (*a*) CMOS based driver interconnect load (DIL) structure. (*b*) Basic structure of interconnects for its aspect ratio of 3(*W*/*H*) along with its surroundings [8]

Table 1 International technology roadmap for semiconductors, 2013 edition (ITRS 2013) based simulation parameters for global interconnects [16]

Technology node	32 nm	22 nm	16 nm
Width, W (nm)	40	28	18
Thickness, H (nm)	120	84	54
Aspect ratio (A/R)	3	3	3
Oxide thickness, Y (nm)	93.6	65.5	40
V_{dd} (V)	0.9	0.8	0.7
Dielectric constant (ε_r)	2.77	2.59	2.31
ρ_{Cu} (μΩ cm)	3.66	4.2	5.69

ignored in the paper therefore, the equivalent inductance and capacitance remains unchanged for both the cases.

5.1 Comparison between resistance with and without considering tunneling conductance

The results present in the Table 2, show the comparison of equivalent single conductor (ESC) resistance without considering tunneling effect (R) and equivalent single conductor (ESC) resistance with tunneling conductance (R_T). It is shown that the variation in R_T is due to change in scattering resistance (R_S) as well as tunneling conductance (G_T) where in case of R is mainly due to change in scattering resistance (R_S) only.

It is revealed from the results shown in Table 2, that the difference of resistances with and without considering tunneling conductance of MWCNT bundle i.e. $R_T - R$, increases as interconnect length increases and technology node decreases as shown in Fig. 9. Similarly, the ratio between ESC resistances (R/R_T) with and without tunneling conductance also increases with increase in interconnects length and decrease in technology nodes as shown in Fig. 10. It is concluded that as the interconnects length increases, the effect of tunneling conductance also increases.

However, the overall impact of tunneling conductance onto the equivalent resistance as shown in the 3rd column of Table 2 as ESC resistance change (%) decreases with respect to increase in interconnect length and shown in Fig. 11. It is also revealed from the results shown in Fig. 11 that there is sharp decrease in case of 16 nm technology nodes as compare to 22 and 32 nm technology nodes. Further, the increasing trend for ESC resistance is observed with decrease in technology nodes for all the interconnect lengths less than 1500 μm but this trend is in increasing order for all the interconnects lengths above 1500 μm as shown in Fig. 11. This is due to the higher rate of increase in scattering resistance for larger interconnects lengths as compare to the impact caused by the tunneling conductance but for small interconnects lengths the rate of increase in scattering resistance is less and hence impact of tunneling resistance become non-negligible. Therefore, it is concluded that for longer (global) interconnect lengths scattering resistance becomes dominant and reduces the impact of tunneling conductance on equivalent resistance, but for smaller (local) interconnect lengths tunneling conductance is still a serious concern and need to considered for accurate performance evaluation of MWCNT bundle interconnect.

5.2 Comparison between delay with and without considering tunneling conductance

Due to the impact of tunneling conductance, ESC resistance increases there is need to analyze the impact on the propagation delay of MWCNT interconnect for different interconnect lengths at 32, 22 and 16 nm technology nodes. A interconnects structure shown in Fig. 8a is used as simulation setup [11]. The input excitation is assumed to be

Table 2 Determining difference, ratio and percentage change between resistance with and without considering tunneling conductance at different technology nodes

Length (μm)	Equivalent resistance difference ($R_T - R$) (kΩ)			Equivalent resistance ratio (R/R_T)			Equivalent resistance change in % $\frac{(R_T-R)}{R} \times 100(\%)$		
	32 nm	22 nm	16 nm	32 nm	22 nm	16 nm	32 nm	22 nm	16 nm
100	0.008	0.024	0.11	0.966	0.956	0.923	3.5398	4.5540	8.3334
500	0.028	0.087	0.31	0.970	0.963	0.950	3.0701	3.6667	5.2013
1000	0.048	0.13	0.385	0.9736	0.971	0.968	2.7118	2.9545	3.2766
1500	0.09	0.148	0.413	0.9777	0.978	0.977	2.2813	2.2561	2.3536
2000	0.07	0.16	0.43	0.980	0.982	0.982	2.0057	1.8369	1.8423
2500	0.075	0.17	0.441	0.983	0.9846	0.985	1.7281	1.5653	1.5136
3000	0.08	0.175	0.45	0.985	0.9867	0.9877	1.5384	1.3440	1.2882

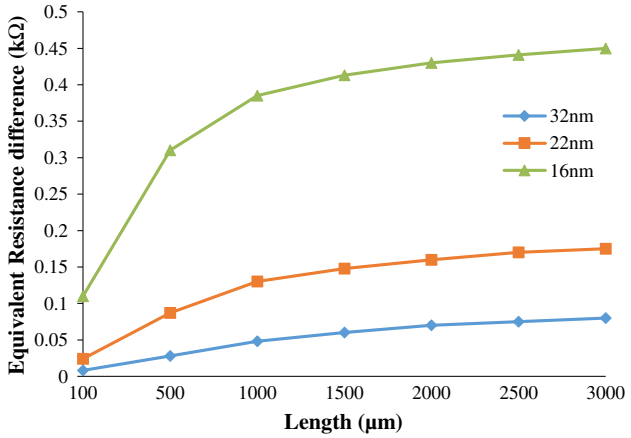

Fig. 9 Equivalent single conductor (ESR) resistance difference ($R_T - R$) between resistance with and without considering tunneling conductance with respect to length at different technology nodes

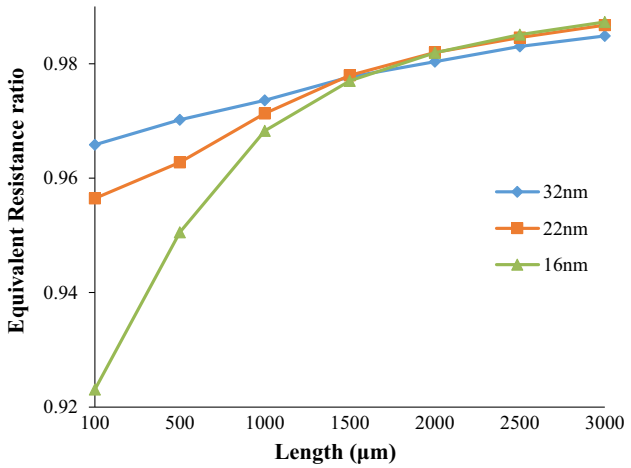

Fig. 10 Equivalent single conductor (ESC) resistance ratio (R/R_T) with and without considering tunneling conductance with respect to length at different technology nodes

pulse signal with same rise and fall time durations. For the comparative analysis of delay, the 'interconnect' can be replaced with tunneling conductance dependent and independent ESC impedance parameters calculated from Sect. 5.1 [20, 21].

The comparison of simulation results obtained for tunneling conductance dependent and independent propagation delay of MWCNT bundle interconnect at different interconnects lengths for 32, 22 and 16 nm technology nodes are shown in Table 3.

It is revealed from the results shown in Table 3 that as the interconnect length increases, normalized delay difference ($\Gamma_T - \Gamma$) which is the difference of delay with tunneling effect (Γ_T) and delay without tunneling effect (Γ), for all the technology nodes increases and shown in Fig. 12.

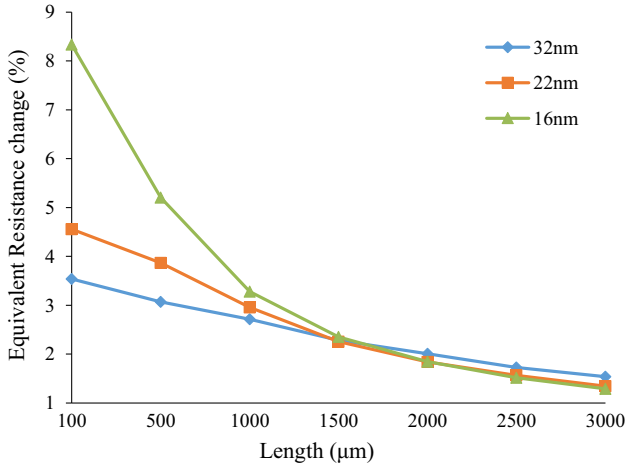

Fig. 11 Equivalent single conductor (ESC) resistance change (%) with and without considering tunneling conductance with respect to length at different technology nodes

The similar trend is also observed i.e. increase in normalized delay difference ($\Gamma_T - \Gamma$) for scaled down technology nodes at same interconnects length. It is also observed that normalized delay ratio (Γ_T/Γ) also increases with increase in interconnects length shown in Fig. 13.

However, the overall impact of tunneling conductance on the normalized delay change (%) as shown in the Table 3 decreases with respect to increase in interconnects length and shown in Fig. 14. It is because of the rate of change of scattering resistance is high compared to rate change of tunneling conductance for larger interconnects length. Further, the normalized delay change (%) is observed to be in increasing order with scaled down technology nodes at same interconnects length. It is concluded that the tunneling conductance has more serious impact on the performance of MWCNT bundle for smaller interconnects length and scaled down technology nodes and cannot be ignored.

6 Conclusion

This paper discussed the various impedance parameters of MWCNT bundle as interconnect for deep submicron technology nodes and based on which a multiple conductor circuit (MCC) model is presented. The impact of tunneling conductance on MCC is included and a modified MCC model is proposed for MWCNT bundle as interconnect. An analytical model is realized to convert tunneling dependent MCC model into ESC model for the better analysis of MWCNT bundle as interconnects. All the impedance parameters of ESC model for MWCNT bundle are obtained using the interconnect parameters proposed in International Technology Roadmap for Semiconductors,

Table 3 Determining difference, ratio and percentage change between delay with and without considering tunneling conductance at different technology nodes

Length (μm)	Normalized delay difference ($\Gamma_T - \Gamma$) in psec.			Normalized delay ratio (Γ_T/Γ)			Normalized delay change (%) $\left[(\Gamma_T - \Gamma)/\Gamma\right] \times 100(\%)$		
	32 nm	22 nm	16 nm	32 nm	22 nm	16 nm	32 nm	22 nm	16 nm
100	0.53	1	2.06	0.9777	0.9691	0.9488	2.277	3.184	5.395
500	3	7	21	0.9809	0.9739	0.9596	1.948	2.671	4.20
1000	7.6	19	54	0.9832	0.9778	0.9705	1.704	2.262	3.034
1500	13	32	88	0.9854	0.9818	0.9776	1.479	1.849	2.285
2000	19	45	123	0.9869	0.9849	0.9820	1.319	1.525	1.833
2500	25	58	156	0.9885	0.9872	0.9850	1.162	1.289	1.514
3000	32	72	187	0.9895	0.9887	0.9873	1.063	1.134	1.276

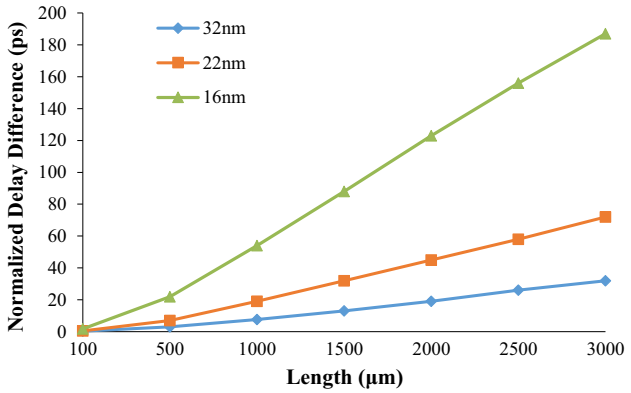

Fig. 12 Normalize difference between delay with and without considering tunneling effect with respect to length at different technology nodes

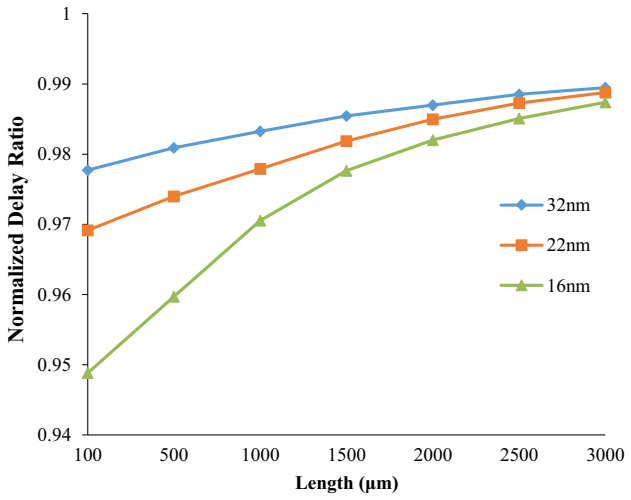

Fig. 13 Normalize delay ratio with and without considering tunneling effect with respect to length at different technology nodes

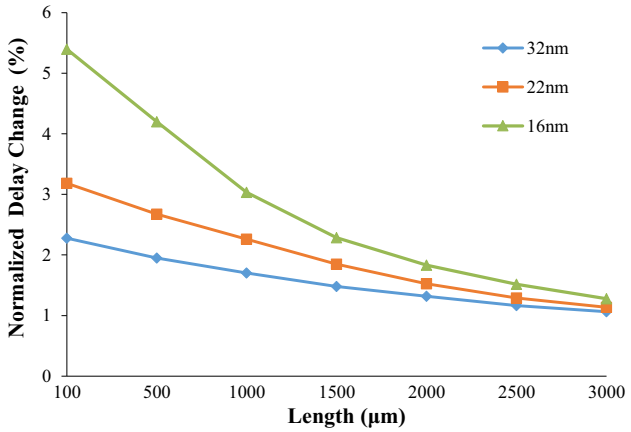

Fig. 14 Normalized percentage change between delay with and without considering tunneling effect with respect to length at different technology nodes

2013 Edition. Based on the impedance parameters obtained from proposed model, the SPICE simulations are performed for both tunneling dependent and independent ESC models for variable interconnect length ranging from 100 to 3000 μm at 32, 22 and 16 nm technology nodes. A comparative study is presented to analyzed the impact of tunneling conductance on equivalent resistance and propagation delay. It is observed from the results that with increases in interconnects length impact of tunneling on the resistance and propagation delay is increases, however the overall percentage change brought by tunneling conductance decrease with interconnects length. On the basis of the analysis and results presented in the paper, it is concluded that tunneling conductance is a serious issue as it has a comparable effect on the performance of the MWCNT bundle at local interconnect lengths. Further, it is also concluded that with scaled down technology nodes,

the effect of tunneling conductance on the performance of MWCNT bundle interconnects in terms of equivalent resistance and propagation delay increases and no longer be ignored to evaluate the accurate performance of MWCNT bundle interconnects.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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