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# A detailed study on the frequency-dependent electrical characteristics of Al/$HfSiO_4$/p-Si MOS capacitors

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**Abstract** The detailed electrical characterizations of Al/$HfSiO_4$/p-Si (MOS) capacitors were investigated. $HfSiO_4$ thin films were fabricated by RF sputtering system with the power of 300 W onto p-type (100) Si substrate and then annealed at 750 °C in Nitrogen environment for 40 min. After fabrication of ohmic contacts, the electrical characteristics of the capacitors were determined by C–V and G/ω–V measurements for several frequencies from 50 kHz to 1 MHz. It is observed that the measured capacitance and conductance curves are quite sensitive to applied voltage frequency due to time dependent interface states ($D_{it}$), border traps ($N_{bt}$), and series resistance ($R_s$). We have observed that the series resistance may significantly deviate from the MOS capacitor characteristics and the relevant correction must be performed. In addition, the calculated interface state density was found to be in the order of $10^{10}$ $eV^{-1}$ $cm^{-2}$ which is in good agreement with reported convenient dielectric layers for MOS based technology. Moreover flat band voltage variation also observed under applied voltage frequencies and this behavior were attributed the basically border states. On the other hand, barrier potentials varied from 0.615 to 0.559 eV with increasing in frequencies depending on the charge accumulations due to time dependent trap sites. Consequently, $D_{it}$, $N_{bt}$, $R_s$ are important factors that can affect electrical characteristics of the MOS capacitors. Although the reported values vary under different applied frequencies, the fabricated $HfSiO_4$ dielectric layer exhibits demanding electrical characteristics to be used in MOS-based technologies.

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## 1 Introduction

Metal–oxide–semiconductor (MOS) capacitors have been widely used for various applications because of their excellent optical and electrical properties [1]. The usability and suitability of a MOS capacitor in nanotechnology and semiconductor device industry depend on devices characteristic which are directly related to the gate dielectrics and their interfaces with the underlying semiconductors, especially for their electrical characteristics [2–5].

Hafnium silicates ($HfSi0_4$) may be a good alternative gate material with high dielectric constant. Hafnium silicate dielectric constant changed between 15 and 25 [6] depending on halfnium (Hf) content. It has excellent thermal stability, adequate band gaps, and compatibility for future MOS-based devices [7–10]. These characteristics of Hafnium silicate are related to the electrical stability of interface between gate oxide and underlying semiconductors [10]. In MOS capacitors, low interface quality causes some defects which can be examined under two headings. One of which is the surface state such as border traps, mobile ionic charges and oxide trapped charges. The other is series resistance. Due to the surface states and the series resistance defects, the electrical characteristics of MOS capacitor deviate from ideal behaviours [11, 12].

In this study, our aim is to investigate the frequency dependent electrical characteristics of Al/$HfSiO_4$/p-Si (MOS) capacitors, especially focussing on oxide–semiconductor interface effect, i.e., interface states, border states and series resistance effects. In addition, the possible uses of $HfSiO_4$ as a dielectric layer in MOS based

technology were discussed from the obtained results. To do this, the electrical characterizations were investigated in the frequency range of 50 kHz to 1 MHz by the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements at room temperature. The measured capacitance and conductance were corrected in order to eliminate series resistance effects and find the real MOS capacitance. Using the corrected $G_c/\omega$–V and $C_c$–V characteristics, the real interface state density ($D_{it}$) for each frequency was calculated. In addition, the capacitance hysteresis were measured and also corrected to examine borders state ($N_{bt}$) effects under applied voltage frequencies. Moreover, the doping concentration ($N_A$), Fermi energy level ($E_F$), diffusion potential ($V_d$), and barrier height ($\Phi_B$) as a function of frequency were obtained by corrected $C_c^{-2}$–V plots.

## 2 Experimental details

In order to fabricate the $HfSiO_4$ thin film, silicon wafer which is 500 μm thick, p-type < 100 > Si substrate with a resistivity of 1–4 Ω was cleaned by the standard Radio Corporation of America (RCA) cleaning process firstly. In RCA cleanning process, silicon wafers were cleaned in 6:1:1 deionized (DI) water–$H_2O_2$–$HNO_3$ for 5 min to get rid of organic residue and then to remove ionic residue silicon wafers were cleaned in a mix of 5:1:1 DI water–$H_2O_2$–HCL solution for 5 min. In order to eliminate naturel oxides in Si surface, the wafers were cleaned in 100:1 DI water–HF solution for 30 s and the cleaning wafers were dried by pure $N_2$ gas lastly. Immediately after surface cleaning, a wafer was loaded in the chamber of the sputter system for $HfSiO_4$ deposition onto Si layer. $HfSiO_4$ target with dimensions of 4-inch and purity of 99.99 %, was used for the deposition of the oxide layers. The base pressure of the sputter chamber was adjusted below $4.0 \times 10^{-4}$ Pa. Then, Ar flow rate was adjusted to be 16 sccm and sputtering pressure was adjusted to be at 1.0 Pa, then the pre-sputtering were performed for 3 h in order to get rid of any impurities on the target surface at 300 W and commercial sputtering was performed following the pre-sputtering in same parameters for 30 min. After deposition of $HfSiO_4$, the $HfSiO_4$/p-Si films were annealed at 750 °C for 40 min in the Nitrogen ambient and the thickness of the film was measured by spectroscopic reflectometer found as 300 nm. After annealing of the films, high-purity aluminum (Al) metal (99.999 %) was deposited by sputtering onto the whole back surface of the wafer and then Schottky contact was also formed by sputtering of Al dots with diameter of about 1.5 mm. The capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements for fabricated Al/$HfSiO_4$/p-Si (MOS) capacitor were performed at different frequencies of 50, 100, 250, 500 750 kHz and 1 MHz at room temperature using an Impedance Analyzer (MODEL HIOKI 3532-50 LCR meter) to study electrical characteristics of fabricated MOS capacitors.

## 3 Results and discussion

The capacitance voltage (C–V) and conductance voltage (G/ω–V) measurements were performed for each frequency between 50 kHz and 1 MHz at room temperature to study electrical instability and possible usage of $HfSiO_4$ in MOS based technology. The measured C–V characteristics curves of Al/$HfSiO_4$/p-Si (MOS) capacitors at different frequencies are shown in Fig. 1. Each C–V curves shows three regimes of accumulation–depletion–inversion region. It is observed that each C–V curves is a function of frequency and bias voltage. Especially, the flat band voltages ($V_{fb}$) are sensitive to the applied voltage frequency and it shifted to higher values than ideal one (−0.55 V) constantly by decreasing the frequency. This behaviour can be attributed to the frequency dependent interface states and border traps localized close to the interface between $HfSiO_4$/Si that exchange mobile carriers with Si [13]. The contribution of these two trap state effects on flat band contribution will be discussed in details further. In addition, as seen in Fig. 1, the capacitance decreases with increasing frequency. This behaviour may be caused by time depended surface states and interface state. The variation in measured capacitance could be explained by the equivalent capacitance circuit [14, 15] observed in Fig. 2.

At the lower frequencies (<500 kHz) the effective capacitance $C_{LF}$ is expressed as

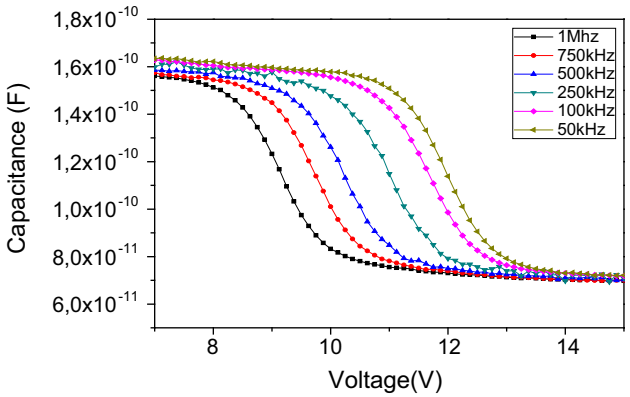



**Fig. 1** C–V characteristics of Al/$HfSiO_4$/p-Si (MOS) capacitor in various frequencies range from 50 kHz to 1 MHz

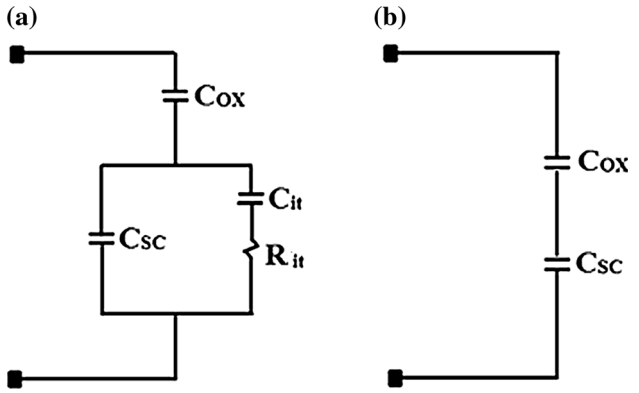



**Fig. 2** Equivalent circuit diagram under **a** low and **b** high frequency regions of MOS capacitors

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + (C_{it}/(1+\omega^2\tau^2))} \quad (1)$$

where $C_{ox}$, $C_{sc}$, are the oxide capacitance, space charge capacitance, respectively, while $C_{it}$ is capacitance associated with the interface traps, ω (ω = 2πf) is angular frequency. Interface trap lifetime (τ), which is on the order of $10^{-6}$–$10^{-7}$ s in the literature, is defined as product of $C_{it}$ and $R_{it}$ where $R_{it}$ is resistance associated with the interface traps. The ωτ is very small at lower frequency, i.e., $(\omega\tau)^2$ can be ignored in the Eq. 1 [16, 17]. This means that if interface trapped charges and defects are easily follow the applied voltage, it leads to yield an excess capacitance at lower frequencies. On the other hand, interface states do not contributed to the total capacitance at the high frequencies (500 kHz>) [15, 18] since interface states are not fast enough to rearrange in response to the applied voltage excitation provided that ωτ > 1. The effective capacitance represented by $C_{HF}$ is expressed by the following expression.

$$\frac{1}{C_{HF}} = \left(\frac{1}{C_{ox}} + \frac{1}{C_{sc}}\right) \quad (2)$$

Considering the interface states contribution to the MOS capacitor characteristic, the C–V curves at all frequencies show three separated regimes, which are called inversion, depletion and accumulation as ideal MOS capacitors. In addition to these, C–V curves do not show kinks measured capacitance at all frequencies. The meaning of this is to highlight that there is a low defect and a good interface between $HfSiO_4$ and p-Si [17, 19, 20]. Moreover, it can be seen in Fig. 1 that each C–V curves shifted to right side with increasing voltage frequency. The variation in C–V curves may be caused by the frequency dependent surface state. The interface states and series resistance are examples of the frequency dependent surface states.

The conductance is a significant parameter to investigate interface quality of the fabricated MOS capacitor [21]. When a small AC signal is applied to MOS capacitor, the conductance caused by interaction between interface states and majority carrier densities in the silicon losses [17]. Hence, it is direct measure of interface states and mobile carriers of Si. Interface traps somewhere near the band edge may be easily intercept and release carriers under different gate voltage influencing the charge and field distribution caused by different curves ideal behaviour of MOS capacitor. Frequency dependent measured conductance is shown in Fig. 3. The measured conductance curves increase with increasing applied voltage frequencies, except at 50 kHz. In addition, measured G/ω–V curves peaks move toward higher voltages with decreasing frequency. This behaviour may be related to relaxation time of trap states, series resistance and interfacial dielectric layer [21].

The series resistance corrections were performed to MOS capacitor characteristics in order to eliminate possible noise effects on the MOS capacitor characteristics. The measured admittance $Y_{ma}$ at strong accumulation of the MOS structure using the parallel RC circuit, is equal to the total circuit admittance [22, 23].

$$Y_{ma} = G_{ma} + j\omega C_{ma} \quad (3)$$

where ω is angular frequency, $C_{ma}$ is measured capacitance and $G_{ma}$ measured conductance in strong accumulation region. Comparing the real and imaginary part of the impedance, the series resistance is given by the following equation [24].

$$R_s = \frac{G_{ma}}{(G_{ma})^2 + (\omega C_{ma})^2} \quad (4)$$

The $R_s$ values of the Al/$HfSiO_4$/p-Si (MOS) capacitor were calculated and are tabulated in Table 1. It is observed that the series resistance values decrease with increasing applied frequency. These behaviours may be explained by re-contraction and re-ordering of defect sites under

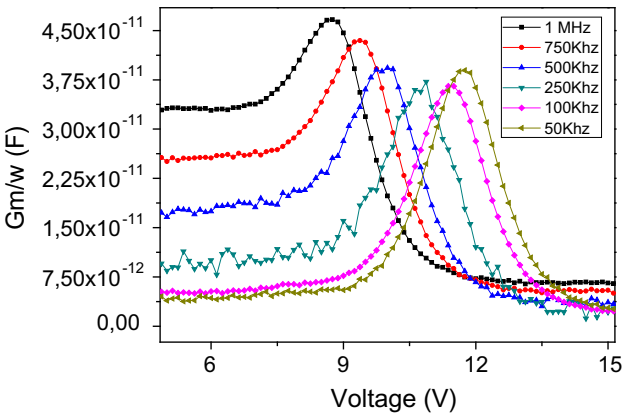



**Fig. 3** Conductance curves for Al/$HfSiO_4$/p-Si (MOS) capacitors for diffrent frequencies

**Table 1** Various calculated frequency-dependent electrical parameters for Al/$HfSiO_4$/p-Si (MOS) capacitors

| Frequency (kHz) | $R_s$ (Ohm) | $G_{c,max}$ ($\times 10^{-11}$ F) | $C_c$ ($\times 10^{-11}$ F) | $D_{it}$ ($\times 10^{10}$ $eV^{-1}$ $cm^{-2}$) | $N_{bt}$ ($\times 10^{11}$ $eV^{-1}$ $cm^{-2}$) |
|---|---|---|---|---|---|
| 50 | 460 | 2.68 | 1.50 | 3.42 | 5.81 |
| 100 | 285 | 2.55 | 1.49 | 3.15 | 4.62 |
| 250 | 215 | 3.01 | 1.36 | 2.97 | 5.49 |
| 500 | 200 | 3.22 | 1.25 | 2.76 | 5.85 |
| 750 | 193 | 3.36 | 1.30 | 2.71 | 5.44 |
| 1000 | 183 | 3.67 | 1.50 | 2.55 | 5.40 |

frequency dispersion [14, 20, 25]. In order to remove series resistance effect from the G–V, G/ω–V curves, the correction of capacitance and conductance characteristic can be calculated by the following equations;

$$C_C = \frac{\left[(G_m)^2 + (\omega C_m)^2\right] C_m}{a^2 + (\omega C_m)^2} \tag{5}$$

and

$$G_C = \frac{\left[(G_m)^2 + (\omega C_m)^2\right] a}{a^2 + (\omega C_m)^2} \tag{6}$$

where ω is angular frequency, $C_m$ is measured capacitance and $G_m$ measured conductance measured voltage range, $a = (G_m) - [(G_m)^2 + (\omega C_m)^2]R_s$. The comparison of the measured and corrected MOS capacitor characteristics, corrected capacitance and conductance curves are shown in Fig. 4a–d. As seen in Figs. 4a, c, the series resistance deviates from the MOS capacitor characteristics, especially, for high frequency measurements. On the other hand, the corrected capacitance did significantly not deviated from the originals. The corrected conductance deviated from originals ones. The measured conductance curves almost increase with increasing frequency while they decrease constantly after correction was performed. This behaviour is expected as indicated in the literature [20, 26, 27]. The observed results indicate that series resistance is an important parameter that is the masking real MOS capacitor characteristics and elimination should be performed before detailed electrical analysis.

Density state of interface state ($D_{it}$), which is the most important parameter affecting C–V characteristics, can be found using following equation [28].

$$D_{it} = \frac{2}{Aq} \frac{G_{c,max}/\omega}{(G_{c,max}/\omega C_{ox})^2 + (1 - C_c/C_{ox})^2} \tag{7}$$

where q is elementary charge, A is front area of MOS capacitor, $C_{ox}$ ($A\varepsilon_0\varepsilon_i/d$) is the oxide capacitance whose value is $1.04 \times 10^{-9}$ F, $\varepsilon_0$ (=$8.85 \times 10^{-14}$ F/cm) is the permittivity of free space [29], $G_{c,max}/\omega$ is peak value of corrected $G_{c,max}/\omega$–V curve, $C_c$ is corrected capacitance of the MOS corresponding to $G_{c,max}/\omega$. Some required values and calculated density of state values are given in Table 1. Frequency dependent interface state density under frequency dispersion is also depicted in Fig. 5. The $D_{it}$ values decrease with increasing applied voltage frequency as expected [30, 31] and the order of $D_{it}$ approximately was calculated as $10^{10}$ $eV^{-1}$ $cm^{-2}$. The calculated values are in the same order as other promising dielectrics reported in [20, 32–34].

Since the $D_{it}$ values are in the expected order, the abnormal changes of the $V_{fb}$ under frequency dispersions probably were caused by border states. In order to calculate border state density, the capacitance hysteresis were measured and then corrected. The corrected capacitance hysteresis curve is shown in Fig. 6 for 1 MHz and 50 kHz. Using the hysteresis curve obtained from flat band voltage shift ($\Delta V_{fb}$), the border state density ($N_{bt}$) in oxide layers were calculated by Eq. 8, assuming the total contribution interface states are almost zero for flat band shift in hysteresis [35, 36], and border state densitises $N_{bt}$, is given by

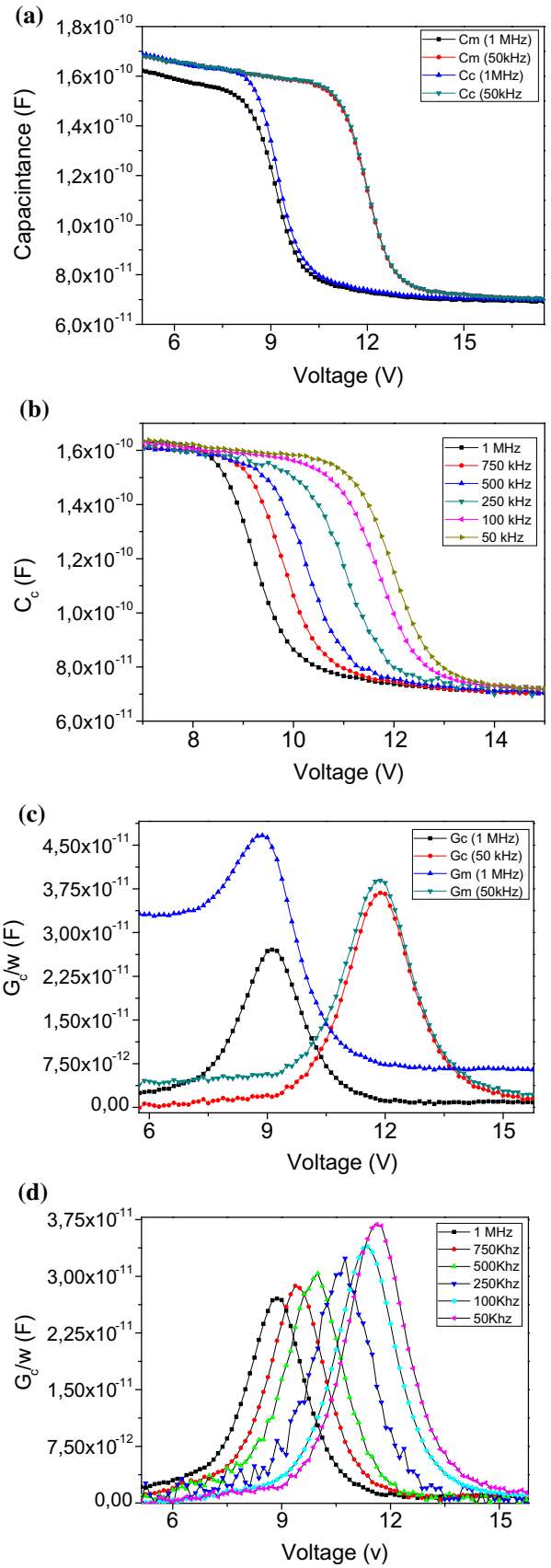
$$N_{bt} = \frac{(C_{acc} \times \Delta V_{FB})}{qA} \tag{8}$$

where $C_{acc}$ is accumulation capacitance. The calculated $N_{bt}$ are given in Table 1. The usual $N_{bt}$ values are in the order of $10^{10}$ $eV^{-1}$ $cm^{-2}$ for real MOS capacitor. However, calculated $N_{bt}$ is in the order of $10^{11}$ $eV^{-1}$ $cm^{-2}$ for fabricated Al/$HfSiO_4$/p-Si (MOS) capacitor. Hence, the abnormal frequency variations on the flat band voltages of the MOS capacitors can be attributed to the frequency dependent border states. In addition, the observed hysteresis is in the counter clockwise direction which clearly reveals a larger reduction of the acceptor-like border traps. Thus, the donor-like border traps play the dominant role [37, 38].

The intercept of $C_c^{-2}$ versus V is plotted in Fig. 7. It has been observed that linearity of the obtained $C_c^{-2} - V$ curves indicates the uniform distribution of interface states in the MOS capacitor structure. The relation between $C_c^{-2}$ and V can be expressed as in the following equation [39, 40].

$$C_c^{-2} = \frac{2(V_0 + V)}{\varepsilon_s \varepsilon_0 q A^2 N_d} \tag{9}$$

where $V_0$ is the applied voltage and $V_0$ (=$V_D - kT/q$) is the intercept of the $C_c^{-2}$ versus V plot with the voltage axis




◀**Fig. 4** Variations on the **a** corrected and measured capacitance for 50 kHz and 1 MHz frequencies, **b** corrected capacitance for various frequencies between 50 kHz and 1 MHz, **c** corrected and measured conductance for 50 kHz and 1 MHz, **d** corrected conductance for various frequencies between 50 kHz and 1 MHz

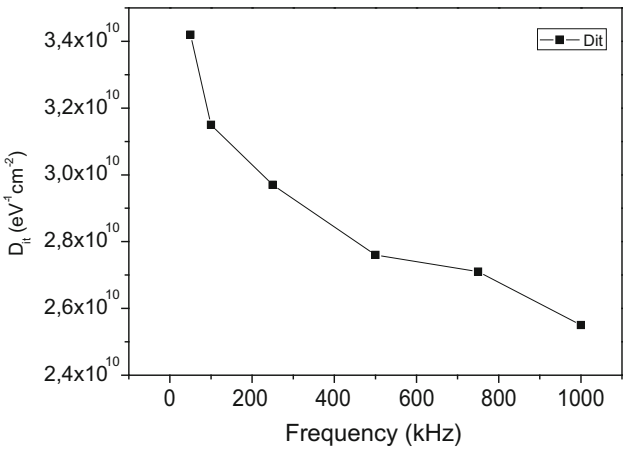



**Fig. 5** Variations of $D_{it}$ as a function voltage for Al/$HfSiO_4$/p-Si (MOS) capacitor

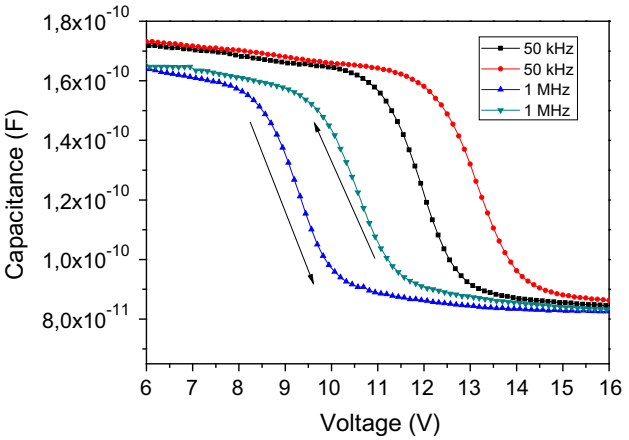



**Fig. 6** Hysteresis C–V characteristics for 1 MHz and 50 kHz

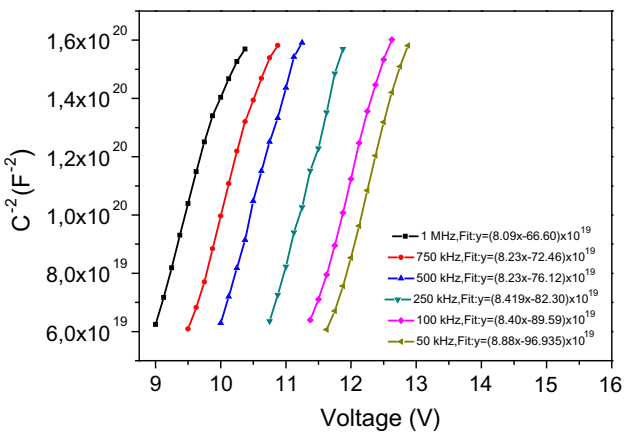



**Fig. 7** $C_c^{-2}$–V characteristics and corresponding linear fit function of Al/$HfSiO_4$/p-Si (MOS) capacitor at various frequencies from 50 kHz to 1 MHz

**Table 2** Barrier potentials and related electrical parameters under frequency dispersion of Al/$HfSiO_4$/p-Si (MOS) capacitors

| Frequency (kHz) | $V_d$ (eV) | $N_A$ ($\times 10^{14}$ $cm^{-3}$) | $E_f$ (eV) | $\Delta\Phi_b$ (meV) | $\Phi_b$ (eV) | $c_2$ |
|---|---|---|---|---|---|---|
| 50 | 0.31 | 4.36 | 0.2850 | 9.06 | 0.615 | 0.02611 |
| 100 | 0.32 | 4.57 | 0.2838 | 26.8 | 0.618 | 0.02735 |
| 250 | 0.30 | 4.57 | 0.2838 | 26.2 | 0.600 | 0.02734 |
| 500 | 0.28 | 4.66 | 0.2832 | 26.0 | 0.584 | 0.02792 |
| 750 | 0.27 | 4.66 | 0.2832 | 26.0 | 0.571 | 0.02791 |
| 1000 | 0.26 | 4.74 | 0.2828 | 25.9 | 0.559 | 0.02840 |

at various frequencies from 50 kHz to 1 MHz, $\varepsilon_s$ is relative permittivity of Si, $\varepsilon_0$ is the permittivity of free space and $N_a$ is the doping concentration obtained from the slope of $C_c^{-2}$ versus V characteristics. The values of barrier potentials ($\Phi_B$) can be obtained by means of the following equation [41].

$$\varphi_B = C_2 V_0 + \frac{kT}{q} + E_F - \Delta\varphi_B \tag{10}$$

where $E_f$ (kT/q) ln($N_v/N_a$) is the energy difference between the bulk Fermi level and valance band edge, $N_v$ is the effective density of state in valance band, $C_2$ is the rate of $N_a$ (experimental)/$N_a$ (Theoretical) [42]. Theoretical value of $N_a$ is 1.67 $\times$ $10^{16}$ $cm^{-3}$. Barrier potential, $\Delta\phi_B$, can be calculated from the following equation.

$$\Delta\varphi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon_s\varepsilon_0}} \tag{11}$$

where $E_m$ is the maximum electric field. These calculated electrical characteristic are tabulated in Table 2. Diffusion potentials are located at the positive voltage since the negative charges are trapped in the MOS capacitor by virtue of the fabrication process. Moreover, doping concentration increase with the increasing applied voltage frequency because of decline in the slope of $C_c^{-2}$ versus V plot. As data in Table 2 show, the $E_f$ is almost constant as excepted under frequency dispersion. Moreover, variations on $V_D$ and $\Delta\phi_B$ were also observed under applied voltage frequency dispersion. This may be related to existence of the interfacial layer $HfSiO_4$, especially, time dependent interface state at the $HfSiO_4$/Si interface. On the other hand, the $\Phi_B$ values varied from 0.615 to 0.559 eV depending on the charge accumulations due to time dependent trap sites.

## 4 Conclusion

In summary, the detailed electrical characteristics of Al/$HfSiO_4$/p-Si MOS capacitor have been investigated for different voltage frequency at the room temperature. According to the results of the study, the capacitance and conductance are sensitive to applied voltage frequency due to frequency dependent charges, e.g., interface states, border traps, and series resistance. Seri resistance decreases with increasing applied voltage frequency and the seri resistance corrections must have been performed before detailed electrical analysis to obtain accurate results. The calculated $D_{it}$ values were found to be in the order of $10^{10}$ $eV^{-1}$ $cm^{-2}$, which is in good agreement with other reported dielectric layer for MOS based technology. In addition, high sensitivity of the $V_{fb}$ voltage variations was attributed to the interface states, especially, time dependent border states. On the other hand, it is observed that barrier potential values are also sensitive to the applied voltage frequencies. However, its values are expectable for elimination of leak charge injection from the substrate into the dielectric and thus the tunnelling effect does not significantly occur. In conclusion, fabricated $HfSiO_4$ dielectric layer exhibits demanding electrical characteristics to be used in MOS-based technologies.

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