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Investigations on high-κ dielectrics for low threshold voltage and low leakage zinc oxide thin-film transistor, using material selection methodologies

Kavindra Kandpal[1] · **Navneet Gupta**[1]

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Abstract This paper presents the investigations on high-κ dielectrics for low operating voltage and low leakage zinc oxide thin film transistor (ZnO TFT) using three material selection methodologies namely Ashby, *technique for order preference by similarity to ideal solution* (TOPSIS) and *VlseKriterijumska Optimizacija I Kompromisno Resenjein in Serbian* (VIKOR). Various material properties such as dielectric constant, conduction band offset to ZnO, band-gap and temperature coefficient mismatch of high κ to ZnO are investigated to find out the most promising gate dielectric material. The analysis concludes that lanthanum oxide (La_2O_3) is the most promising gate dielectric material for ZnO TFT transistor. The result shows a good agreement between Ashby's, TOPSIS and VIKOR approaches.

1 Introduction

From the last two decades, thin film transistors (TFTs) are mostly using polycrystalline silicon (poly-Si) or amorphous silicon (a-Si) as an active channel layer [1, 2]. However, these TFTs (especially the a-Si ones) suffer from various limitations such as low field effect mobility (μ_{FE}), light sensitivity, light degradation and threshold voltage shift. Fortunato et al. [3] suggested that utilization of efficient and reliable oxide based TFTs may overcome these problems. Transparent oxide semiconductor based transistors have recently been proposed using an active channel layer of zinc oxide, a *II–VI* compound semiconductor. ZnO possesses wide band-gap (3.4 eV), and has a stable wurtzite structure with lattice spacing $a = 0.325$ nm and $c = 0.521$ nm. It is a multifunctional material that can be applied to gas sensors, transparent electrodes, blue and UV light emitters, piezoelectric devices, photovoltaic devices, and bulk acoustic wave devices [4, 5]. Intrinsically it is an n-type semiconductor primarily due to presence of oxygen vacancies. As compared to a-Si, ZnO provides many advantages. It can be grown as a crystalline material at relatively low deposition temperature [6]. Further, it can be deposited on various substrates made of silicon or amorphous glasses [6], which make it possible to have a total transparent ZnO-TFT by depositing ZnO on the indium tin oxide (ITO) glasses. Because of its wide band-gap, the characteristics of ZnO-TFTs do not degrade in the exposure of visible light. Also, ZnO thin film used as an active channel layer can achieve a relatively high mobility.

The performance of a TFT depends fundamentally on the type of gate insulator and the quality of dielectric-channel interface because of the current flows in the ZnO channel next to the interface. In recent years, researchers have focused on high-κ dielectric materials as an alternative to SiO_2 in highly-scaled electronic devices [7–10]. However, despite the intensive work on high-κ dielectrics, the performance of the devices with high-κ dielectrics is still rather poorly analyzed compared to those with SiO_2 gate oxides. The use of high-κ gate dielectrics in TFTs is becoming increasingly necessary, as scaled transistors lead to unacceptable levels of gate leakage current. ZnO TFTs suffer from high operation voltage and threshold voltage compared to Si–H TFT, e.g. ZnO TFT with SiO_2 or Si_3N_4 gate dielectric exhibits a very high threshold voltage (V_T)

✉ Kavindra Kandpal
kavindra_ec@yahoo.com

Navneet Gupta
ngupta@pilani.bits-pilani.ac.in

[1] Department of Electrical and Electronics Engineering, Birla Institute of Technology and Science, Pilani, Rajasthan, India

value (10–20 V) [11]. An increase in coupling of gate field to the channel layer reduces the operating voltage of the transistor. This can be done either by reducing the gate dielectric thickness or by using a gate dielectric material with higher dielectric permittivity (high-κ gate dielectric). Both solutions increase the gate capacitance; however, high-κ material presents a more promising solution since a thicker high-κ layer may be used to produce an equivalent capacitance. But, the gate dielectric material selection is not straightforward. Many dielectric materials are currently under consideration as potential gate dielectric of ZnO thin film transistor. It includes HfO_2, Gd_2O_3, La_2O_3, ZrO_2, Ga_2O_3, Al_2O_3, $BaTiO_3$ etc. [20–26].

The key performance parameters for selection of a potential gate dielectric require permittivity, band-gap and band alignment to ZnO. However, together with these parameters; film morphology, stability, interface quality, reliability and process compatibility [12] are also important to further enhance the device performance. As there are various high-κ dielectric that have been reported in fabrication of ZnO-TFT, where each dielectric is having its own advantages and limitations, so in order to find out the best possible alternative, one can use multi-criteria decision making (MCDM) approach [14] when there are more than one attribute. The MCDM approach is further subdivided into multi-objective decision making (MODM) and multi-attribute decision making (MADM). These approaches are well studied by many researchers in engineering regime [14–19]. The most popular material selection methodologies are Ashby approach [15, 16], TOPSIS and VIKOR [17, 18].

This paper is organized as follows: Sect. 2 deals with ZnO thin film transistor and high-κ dielectrics. Section 3 deals with material selection methodologies used in this work. Section 4 consists of determination of material indices used in the analysis. Section 5 consists of results and discussion, and Sect. 6 presents the conclusion drawn from the study.

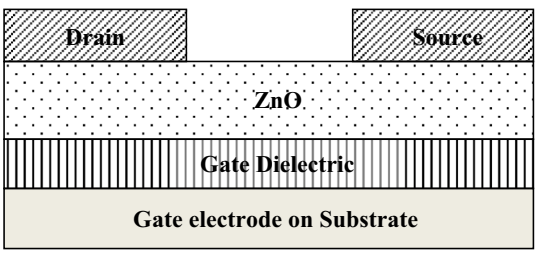

Fig. 1 Schematic view of bottom gate ZnO TFT structure

2 ZnO TFT and high-κ dielectric

Figure 1 shows a schematic view of bottom gate ZnO-TFT in which ZnO acts as a channel between drain and source of TFT. In bottom gate structure, ZnO thin film is deposited over gate dielectric. An interface between ZnO and gate dielectric is formed which is very crucial for the device performance. For enhanced performance, the interface needs to be clean and free from various defects. Therefore, the ZnO channel and underlying gate dielectric should not be subjected to excessive stress as it can give rise to interface defects or can raise reliability concerns. Moreover, the dielectric material and the channel should not react in elevated temperature. Thus, the interface should be chemically and thermodynamically stable.

According to the boundary condition, the transverse electric field density (D) should be continuous at the oxide-ZnO interface,

$$D_{oxide} = D_{ZnO} \tag{1}$$

In terms of electric field Eq. (1) can be written as,

$$k_{oxide}\varepsilon_0 E_{oxide} = k_{ZnO}\varepsilon_0 E_{ZnO} \text{ or } E_{ZnO} = \frac{k_{oxide}}{k_{ZnO}} E_{oxide}. \tag{2}$$

From the above equation it is clear that the higher the dielectric constant of gate oxide, the higher would be the electric field in the ZnO, which will result in same amount of charge in the ZnO with less applied gate bias, resulting in a lower threshold voltage V_T.

In terms of the voltage the Eq. (2) can be written as

$$E_{ZnO} = \frac{k_{oxide}}{k_{ZnO}} \frac{V_{ox}}{t_{ox}}. \tag{3}$$

Hence a reduction in oxide thickness can also results in high field with reduced gate bias.

Another term which is used to define the scaling capability of high-κ dielectric compared to SiO_2 is EOT (Effective oxide Thickness). The EOT of a high κ is the thickness required by SiO_2 to achieve same voltage modulation effect or same equivalent capacitance density [12]. EOT is defined as

$$EOT = \frac{k_{SiO2}}{k_{High-k}} t_{High-k}. \tag{4}$$

A lower value of EOT is helpful in reducing leakage.

There are advantages associated with high-κ gate dielectric in ZnO-TFTs. Using a thicker dielectric layer, will lead to reduction in gate field at the ZnO-Oxide interface and consequently reduce the effect of gate bias stressing on the threshold voltage V_T. The use of thicker high-κ dielectric layers also reduces gate leakage current without affecting the induced interface charge density. Moreover, since one needs high driving capacity of TFT to

drive the OLED pixel, one needs higher oxide capacitance and this can be achieved effectively by high-κ dielectric. However, a very large value of dielectric constant κ can lead to unfavorable large fringing field at source and drain region [13].

3 Material selection methodologies

Ashby approach is one of the most commonly used MODM approach as it optimizes alternatives based on the prioritized objectives. VIKOR and TOPSIS are MADM techniques and the alternatives are ranked on the basis of weighted attributes. Ashby approach is very easy when performance indices are less in number however, it does not generate ranking score. VIKOR and TOPSIS are widely used for a wide range of material selection problem which gives ranking solution. VIKOR and TOPSIS approaches differ in the fact that; VIKOR uses linear normalization method whereas TOPSIS uses vector normalization to convert different scales of various criteria into standard units [18, 19]. TOPSIS method gives the solution by finding the shortest distance from the ideal solution and longest distance from worst case solution whereas the VIKOR gives the compromise solution by determining least individual regret of the opponent and highest group utility of majority [18, 19].

Flow chart shown in Fig. 2 illustrates the various steps that are used to find out the best gate dielectric for ZnO TFT. First step is to find out the possible dielectric candidates those form stable interface with ZnO. Lei H. Wen et al. [20] has studied ZnO–Al_2O_3 heterojunction, which is formed by Laser Molecular Beam epitaxy (LMBE). Moon et al. [21] studied ZnO TFT using La_2O_3 gate dielectric, where La_2O_3 was deposited using electron cyclotron resonance-atomic layer deposition (ECR-ALD). Moreover, the ZnO and $BaTiO_3$ interface was studied and band offsets was measured by Jia et al. [22]. Similarly all the other dielectric materials used in this study has been successfully demonstrated by various researchers on ZnO [23–27]. Next step is to find out the material indices like Eg, κ and CBO and difference in temperature coefficient. This will lead to construction of fundamental decision matrix. This is followed by particular material selection methodology, to find out the best suitable material candidate out of all the possible alternatives.

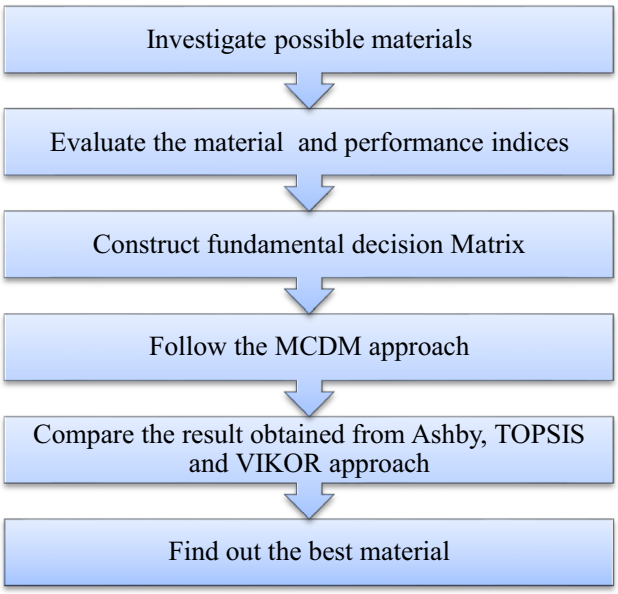

Fig. 2 Flow chart of material selection approach

3.1 Ashby approach

The Ashby approach involves mainly four steps, i.e.

1. Translation of design requirements, based on objective, design constraints and free variables.
2. Screening using various constraints
3. Finding out suitable set of solution using the objectives
4. Seeking additional information and validation with experimental results if available.

The objective is to minimize leakage and maximize dielectric constant so that ZnO TFT can be operated at low voltages. The constraints for Ashby analysis for this device are:

1. Band-gap should be high (>5 eV) [39]
2. Dielectric constant (κ) >15 [39]
3. Conduction band offset (ΔEc) >1 eV [40]

Here the variables are the choice of materials (from set of material reported for ZnO TFT in literature) and material indices (M) are band-gap (Eg), Dielectric constant (κ) and CBO (ΔE_c). The functional parameter (F) is leakage current and the geometrical parameter is scaling limit (t_{ox} or EOT). Now, one can define Ashby function A, which will determine the performance of TFT as: $A = f$ {F, G, M}.

In any field effect transistor, the leakage current density for the case when tunneling is dominated by ECB tunneling mechanism, can be modeled by a semi empirical equation [30] given by

$$J_G \propto \exp\left\{-\frac{4\pi(2q)^{\frac{1}{2}}}{h} * \left(m_{eff}\phi_b\right)^{\frac{1}{2}} k * EOT\right\} \quad (5)$$

where h is Planck's constant, q is electron charge, m_{eff} is electron tunneling mass, and ϕ_b is barrier height.

$$J_G = b * \exp\{-a * f * EOT\} \quad (6)$$

where $= \left(m_{eff}\emptyset_b\right)^{\frac{1}{2}}k$, a and b are the constant.

From Eq. (6) it is deduced that higher the value of f, lower will be the leakage current density. For a given value of supply voltage and maximum current density J_{Gmax} the scaling limit is reciprocally related to figure of merit as:

$$t_{ox} = \frac{\ln \frac{b}{J_{G,max}}}{a} f^{-1}. \tag{7}$$

3.2 TOPSIS approach

This approach was introduced by K. Yoon and H. C. Lai in 1981 [17]. This is used to find out the best alternative by finding out the shortest Euclidean distance (S*) from ideal solution (A*) and largest distance (S^-) from worst case solution (A^-) (or negative ideal solution). The steps followed in TOPSIS approach are:

Step 1 Preparation of normalized decision matrix N.

Normalized decision matrix N, consists of n_{ij}, elements with *i*th number of alternatives under *j*th number of criterion. This matrix is normalized with RMS value given by:

$$n_{ij} = \frac{x_{ij}}{\sqrt{\sum_{i=1}^{u}\left(x_{ij}\right)^2}} \tag{8}$$

where i represents the set of alternative $= 1, 2, 3, \ldots, u$, and j represents set of criteria $= 1, 2, \ldots, v$

Step 2 Preparation of weighted normalized matrix.

In this step we assign weight to all criteria where the value of weights is chosen such that $\sum_{J=1}^{v} w_j = 1$, now weighted normalized matrix $M_{ij} = n_{ij}$ x w_j.

Step 3 Computation of ideal and negative ideal solution.

The ideal solution $A^* = \{\max M_{ij} | \, j \in J_1\}$ or $(\min M_{ij} | \, j \in J_2) = \left\{M_1^*, M_2^*, M_3^*, \ldots, M_v^*\right\}$.

The worst case solution $A^- = \{\min M_{ij} \mid j \in J_1\}$ or $(\max M_{ij} \mid j \in J_2) = \{M_1^-, M_2^-, M_3^-, \ldots, M_v^-\}$.

where J_1 is associated with the benefit criteria and J_2 is associated with cost criteria.

Step 4 Calculation of separation measure from ideal and non ideal solution.

Now Euclidean distance can be measured as:

$$S_i^* = \sqrt{\sum_{j=1}^{v}\left(M_{ij} - M_j^*\right)^2} \tag{9}$$

i.e. Euclidean distance from ideal solution

$$S_i^- = \sqrt{\sum_{j=1}^{v}\left(M_{ij} - M_j^-\right)^2} \tag{10}$$

i.e. Euclidean distance from non ideal solution

For both i = 1, 2, 3… u.

Step 5 Measurement of relative closeness (C_i) from ideal solution.

The relative closeness from ideal solution can be measured as:

$$C_i = \frac{S_i^-}{S_i^- + S_i^*}, 0 < C_i < 1 \; for \; i = 1, 2, \ldots..u \tag{11}$$

The ranking of alternatives now depends upon the value of C_i, larger the value of C_i, better will be the performance of the alternative.

3.3 VIKOR approach

This approach was first proposed by Opricovic in 1998 [31] and widely accepted for selecting the material for engineering design. However, Chang [32] developed a modification in VIKOR method to simplify numerical calculation in solving problems. This method focuses on ranking and selecting from various alternatives. It is a fuzzy logic based methodology which provides a compromising solution based on the following steps.

Step 1 Determination of x_j^* and x_j^- values.

If x_{ij} element belongs ith row (belongs to alternative) and jth column (belongs to criterion) of fundamental decision matrix, then first we determine x_j^*, where j = 1,2,…, v, as $\max\{x_{ij}\}$ or $\min\{x_{ij}\}$ for i = 1,2,3,…, u,if it represents benefit criteria or cost criteria respectively. Similarly x_j^- is $\min\{x_{ij}\}$or $\max\{x_{ij}\}$ for i = 1,2,…, u, if it represents benefit criteria or cost criteria respectively.

Step 2 To construct the maximum group utility G_i and minimum regret of the opponent R_i.

The values for G_i and R_i where i = 1,2,3,…, u is given by the following equations.

$$G_i = \sum_{j=1}^{v} w_j \frac{\left(x_j^* - x_{ij}\right)}{\left(x_j^* - x_j^-\right)} \tag{12}$$

$$R_i = \max_j \left[w_j \frac{\left(x_j^* - x_{ij}\right)}{\left(x_j^* - x_j^-\right)} \right] \tag{13}$$

where w_j is the weight of *j*th criteria and $\sum_{j=1}^{v} w_j = 1$.

Step 3 Calculation of Q_i for *i*th alternative where i = 1,2,3,…, *u*.

This is done using

$$Q_i = \sigma \frac{(G_i - G^*)}{(G^- - G^*)} + (1-\sigma)\frac{(R_i - R^*)}{(R^- - R^*)} \quad (14)$$

where G^- is max$\{G_i\}$ and G^* is min$\{G_i\}$, R^- is max$\{R_i\}$ and R^* is min$\{R_i\}$ and σ weight of strategy G_i and (1-σ) is weight of strategy R_i, usually the value of σ is chosen 0.5.

Step 4 Sorting the value of *R*, *G* and *Q*.

Finding out the value of *R*, *G* and *Q* in increasing order compute the ranking order (A^1, A^2, A^3,…,A^u).

Step 5 Now the best alternative can be find out depending upon the flow chart illustrated in Fig. 3, where $DQ = 1/(U-1)$; where *U* is number of alternative.

4 Material indices of the gate-dielectrics

The value of band-gap (E_g) and dielectric constant for the high-κ material can be found easily in literature [27]. In literature the band offset value for various dielectrics are mentioned with respect to silicon. However, in present work it is required to calculate the band alignment of dielectrics on ZnO.

Figure 4 shows the dielectric-ZnO interface which is used to calculate the band offset of high-κ material on ZnO. From this figure it seems that conduction band offset (ΔE_c) is the difference between electron affinity of high-κ and ZnO. However, band offset also depends upon charge transfer across interface which creates interface dipole. J. Robertson and B. Falabertti [27, 28] have used charge neutrality level (CNL) method to find out the conduction band offset (ΔEc) of high κ gate oxide on III–V semiconductor. One can use the same model to find out the band

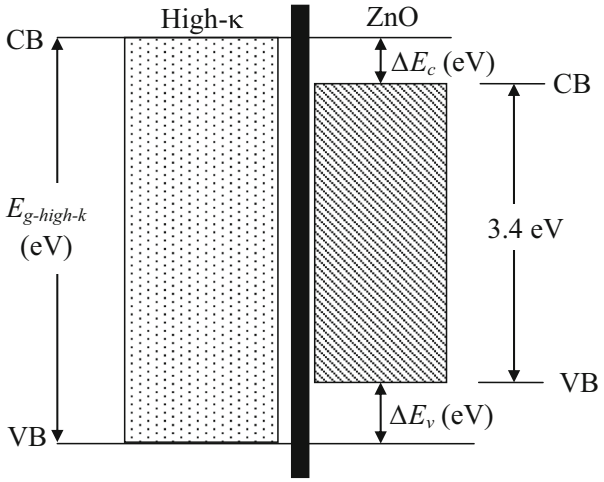

Fig. 4 Band offset of high-κ material on ZnO

offset value on ZnO semiconductor. According to this interface between oxide and semiconductor can be considered as an interface between two semiconductor, i.e. semiconductor *a* and semiconductor *b*. The conduction band (CB) offset is given by [27]

$$\Delta E_c = (\chi_a - CNL_{s,a}) - (\chi_b - CNL_{s,b}) + S(CNL_{s,a} - CNL_{s,b}) \quad (15)$$

where χ is electron affinity of semiconductor and *CNL* is the charge neutrality level of respective semiconductor measured from vacuum level. S is a Schottky barrier pinning factor, $0 < S < 1$. The value of S is 1 in the absence of dipoles i.e. wide band-gap material and the value of S is 0 for the strongly pinned interface. So we can simplify the Eq. (15) for ZnO-high κ interface as:

$$\Delta E_c = (\chi_{ZnO} - \chi_{High-k}) + (S-1)\left[(\chi_{ZnO} - \chi_{High-k}) - (CNL_{ZnO} - CNL_{High-k})\right] \quad (16)$$

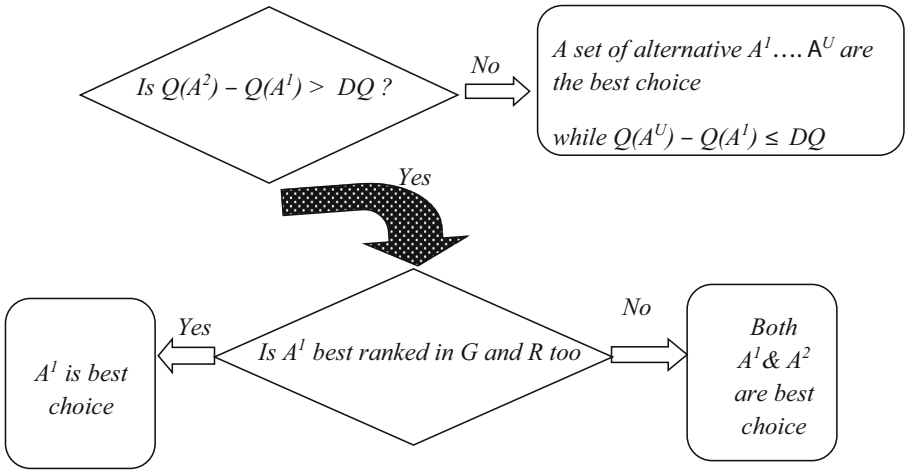

Fig. 3 Decision flow chart for VIKOR approach

The electron affinity and CNL of ZnO are 4.6 eV and 3.27 eV [27] respectively. The values of electron affinity of various dielectrics are found on J. Robertson [28] work. The value of S can be found by the empirical relation given by Monch [29].

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2} \quad (17)$$

where ε_∞ is electronic part of dielectric constant. The CNL values given in Table 1 are measured from the top of valence band. Like La_2O_3, Sc_2O_3 and Y_2O_3 show same bad offset performance of 3.1 eV as calculated from Eq. (16). Table 1 shows electron affinity, charge neutrality level, S and conduction band offset to ZnO of all possible high-κ gate dielectric and Table 2 provides the values for band-gap, dielectric constant and conduction band offset.

Most of the oxide e.g. La_2O_3, Al_2O_3, Gd_2O_3, ZrO_2 etc. show excellent CBO because ZnO possesses large value of electron affinity. Once the CBO values are known, the valence band offset (VBO) values can be easily computed. Figure 5 shows the CBO and VBO of various high κ oxides on ZnO. A positive value of VBO indicates that the holes need particular amount of energy to cross energy barrier i.e. ZnO valence band to high-κ valence band. Table 2 gives material indices of various dielectrics.

Together with the material indices listed in Table 2; thermal expansion coefficient mismatch (|ΔTEC|) also plays an important role in deciding the performance of TFT because deposition of thin film on a substrate or channel includes high temperature process. Also a significant amount of temperature coefficient mismatch may lead to considerable amount of stress which will eventually leads to defects in interface, or excessive stress which can cause the device failure. Table 3 shows the values of thermal coefficient mismatch in PPM/^{0}K of various gate dielectrics with ZnO.

ZnO has a thermal expansion coefficient close to 4.6×10^{-6}/ °C [33]. |Δ TEC| in PPM/ °C is computed by taking the difference between TEC of ZnO and dielectric irrespective of the nature of stress i.e. compressive or tensile. So |Δ TEC| is a cost criterion for TOPSIS and VIKOR approach.

Table 1 Materials and their conduction band offset (ΔE_c)

Dielectric Materials	$X_{\text{high-}\kappa}$ (eV)	*CNL* (eV)	S	CBO (eV)
HfO_2	2.4	3.7	0.52	2.2
ZrO_2	2.5	3.6	0.52	2.1
$HfSiO_4$	2	3.6	0.56	2.7
La_2O_3	2	2.4	0.53	3.1
$LaAlO_3$	2.5	3.8	0.53	1.9
$SrTiO_3$	3.9	2.3	0.28	0.8
Ta_2O_5	3.3	3.3	0.4	1.1
Ga_2O_3	3.5	2.8	0.49	1.5
Gd_2O_3	2.4	2.3	0.41	2.9
Al_2O_3	1	6	0.69	3.3
SiO_2	0.9	4.5	0.95	3.7
Si_3N_4	2.1	2.6	0.59	2.5
$BaTiO_3$	–	–	–	−0.75[a]

[a] Jia et al. [22], have measured the value of band offset using X-ray photoelectron spectroscopy

Table 2 Material indices matrix

Dielectric	E_g (eV)	κ	CBO (ΔE_c)
HfO_2	6	25	2.2
ZrO_2	5.8	25	2.1
$HfSiO_4$	6.5	11	2.7
La_2O_3	6	30	3.1
$LaAlO_3$	5.6	30	1.9
Ta_2O_5	4.4	22	1.1
Ga_2O_3	4.8	23	1.5
Gd_2O_3	5.8	16	2.9
Al_2O_3	8.8	9	3.3
SiO_2	9	3.9	3.7
Si_3N_4	5.3	7	2.5
Y_2O_3	6	15	3.1
Sc_2O_3	6.3	14	3.1
$BaTiO_3$	3.1	2000	-0.45
$SrTiO_3$	3.3	2000	0.8

5 Results and discussion

5.1 Ashby analysis

In Ashby approach first step is to plot the graphs in between various material indices. Then one needs to apply the constraints to find out possible sets of dielectrics.

Figure 6 shows the plot between conduction band offset and band-gap for all the possible high-κ dielectric. As one requires E*g* more than 5 eV and CBO more than 1 eV it is clear that Ga_2O_3, $SrTiO_3$, Ta_2O_5, $BaTiO_3$ do not fulfill the required conditions. The materials that satisfy the requirements are shown under the shaded rectangle.

Figure 7 shows the plot between band-gap and dielectric constant of all possible materials. As one needs E_g more than 5 eV and κ more than 15, SiO_2, Al_2O_3, $HfSiO_4$, Si_3N_4, Ta_2O_5, Ga_2O_3, Sc_2O_3, Gd_2O_3 violate the constraints and are removed from the selection of gate dielectric. Shaded rectangle shown in Fig. 7 covers all those materials that satisfy the conditions.

Figure 8 shows plot between CBO and dielectric constant. As stated one needs CBO greater than 1 eV and κ

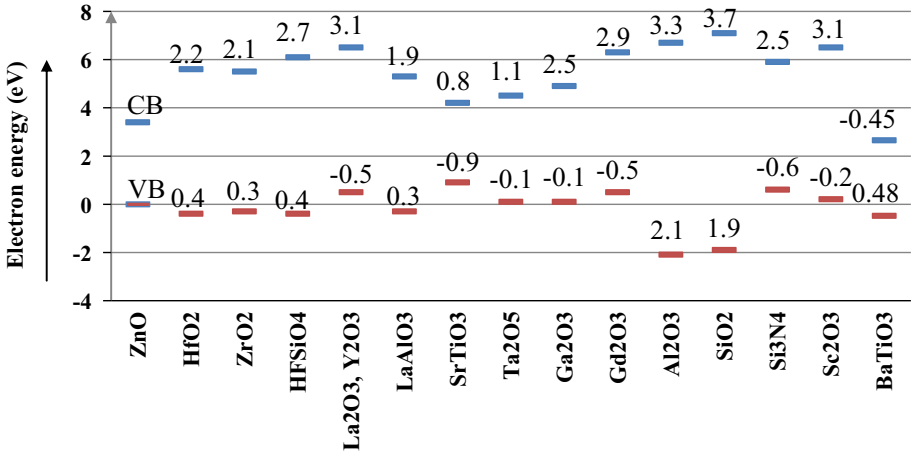

Fig. 5 The CBO and VBO of various high κ dielectrics on ZnO, the y axis is energy in (eV)

Table 3 Material indices |ΔTEC| PPM/^{0}K for various dielectrics [34–38]

Dielectric	|ΔTEC|PPM/^{0}K	Dielectric	|ΔTEC|PPM/^{0}K
HfO_2	0.1	Sc_2O_3	2.2
ZrO_2, Ga_2O_3	2.8	Gd_2O_3	1.26
$HfSiO_4$	6.3	Al_2O_3	3.9
La_2O_3	4.1	SiO_2	4
$LaAlO_3$	7.1	Si_3N_4	1.7
Ta_2O_5	0.5	Y_2O_3	2.9

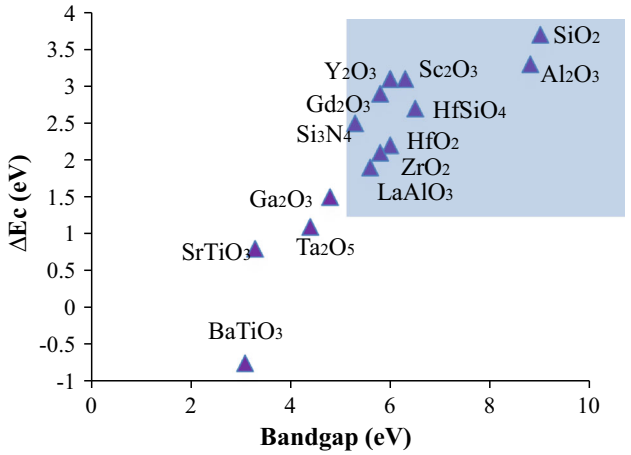

Fig. 6 Plot of conduction band offset versus band-gap of for various dielectrics

greater than 15, SiO_2, Al_2O_3, Sc_2O_3, $HfSiO_4$, Si_3N_4 don't fit in constraint. Hence the material left that satisfies all the constraints are HfO_2, ZrO_2, La_2O_3, $LaAlO_3$. Ga_2O_3 and Ta_2O_5 narrowly violate these constraints. However, by investigating the figure of merit (*f*) of these possible dielectrics it is clear that best alternative as a gate dielectric of ZnO TFT is La_2O_3. This is followed by $LaAlO_3$, ZrO_2 and HfO_2 (Fig. 9).

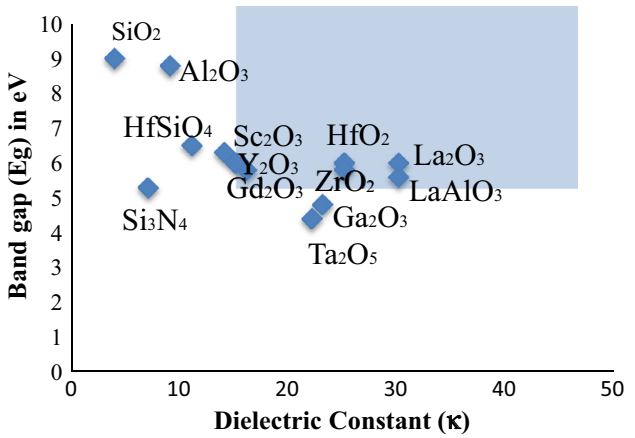

Fig. 7 Plot of band-gap versus dielectric constant for various dielectrics

5.2 TOPSIS analysis

For the TOPSIS and VIKOR one needs a weight matrix with proper justification. The dielectric constant κ can be given highest weight because of reason stated in Sect. 2. It

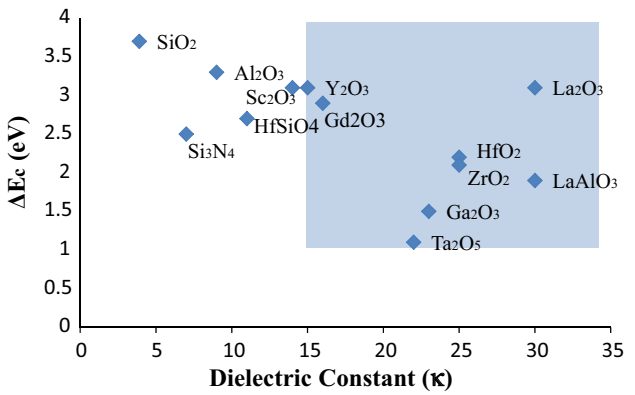

Fig. 8 Plot of conduction band offset versus dielectric constant

is followed by CBO and then by band-gap and the least weight is given to temperature coefficient mismatch because various process techniques are available which either can deposit oxides in low thermal budget or some additional deposition of stress relieving material which can overcome the induced intrinsic stress. So keeping $\sum_{J=1}^{v} w_j = 1$ in view, the weight matrix is W = [0.4, 0.3, 0.2, 0.1]. Table 4 shows the weighted normalized matrix as mentioned in Sect. 3.2.

The parameters in brackets in Table 4 are the normalized value of parameter with respect to root mean square value. From the Table 4 one can find out the ideal (A*) and negative ideal (A^-) solution as:

$$A* = \{0.1696, 0.115927, 0.079125, 0.000763\}$$
$$A^- = \{0.022048, 0.034465, 0.038683, 0.054171\}$$

Table 5 gives the values of Euclidean distance from ideal and non ideal solution, relative closeness from ideal solution (C) and the TOPSIS rank.

From the Table 5 it is observed that La_2O_3 is best ranked material followed by, HfO_2, ZrO_2 and $LaAlO_3$.

5.3 VIKOR analysis

From the calculation of maximum group utility G_i and minimum regret of the opponent R_i one can find out the following.

$$\text{Minimum } R_i = R^* = 0.130435,$$
$$\text{Maximum } R_i = R^- = 0.4$$
$$G* = \text{Minimum } G_i = 0.256808,$$
$$G^- = \text{Maximum } G_i = 0.674679$$

Table 6 shows the value R, G and Q for all the dielectrics and ranking based on the values of corresponding R, G and Q.

Since $Q(A^2) - Q(A^1) > 0.08334$ *a*nd A^1 is the same for R and G too hence La_2O_3 is best choice material followed by HfO_2. While comparing the result of all the three approaches all gives La_2O_3 a lead over other dielectrics. Other suitable dielectric materials that can be used are HfO_2, ZrO_2 and $LaAlO_3$.

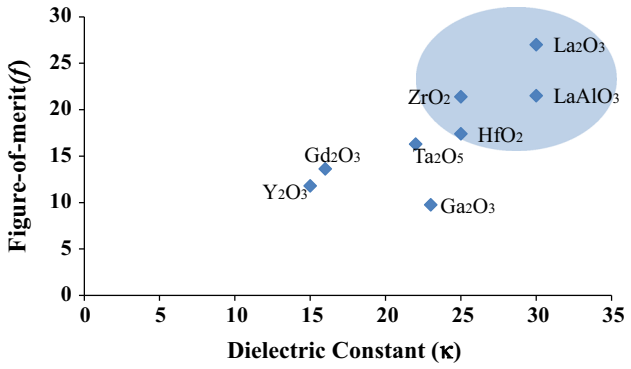

Fig. 9 Plot of figure of merit versus dielectric constant

Table 4 Weighted normalized matrix

Dielectric	0.4* [κ]	0.3* [CBO]	0.2*[Eg]	0.1* [|ΔTECl|]
HfO_2	0.141334	0.06893	0.05275	0.000763
ZrO_2	0.141334	0.065796	0.050992	0.021363
$HfSiO_4$	0.062187	0.084595	0.057146	0.048067
La_2O_3	0.1696	0.097128	0.05275	0.031282
$LaAlO_3$	0.1696	0.05953	0.049233	0.054171
Ta_2O_5	0.124374	0.034465	0.038683	0.003815
Ga_2O_3	0.130027	0.046997	0.0422	0.021363
Gd_2O_3	0.090453	0.090862	0.050992	0.009613
Al_2O_3	0.05088	0.103394	0.077367	0.029756
SiO2	0.022048	0.115927	0.079125	0.030519
Si_3N_4	0.039573	0.078329	0.046596	0.01297
Y_2O_3	0.0848	0.097128	0.05275	0.022126
Sc_2O_3	0.079147	0.097128	0.055388	0.016785

Table 5 TOPSIS results with rank

Dielectric	S^-	S^+	C	Rank
HfO_2	0.135894	0.060856	0.690695	2
ZrO_2	0.128213	0.06729	0.655811	3
$HFSiO_4$	0.067099	0.123451	0.352135	12
La_2O_3	0.162543	0.044502	0.785061	1
$LaAlO_3$	0.150037	0.083226	0.643211	4
Ta_2O_5	0.114045	0.101619	0.528809	7
Ga_2O_3	0.113601	0.090029	0.557881	5
Gd_2O_3	0.099984	0.088104	0.531581	6
Al_2O_3	0.087607	0.122863	0.416246	10
SiO_2	0.093974	0.150523	0.384356	11
Si_3N_4	0.063177	0.139742	0.31134	13
Y_2O_3	0.095337	0.093255	0.505521	8
Sc_2O_3	0.094147	0.096723	0.493251	9

In order to validate findings of this work, the results of proposed analysis are compared with the experimental data. Table 7 shows the comparative analysis of ZnO based TFT employing different dielectrics namely La_2O_3, HfO_2 and ZrO_2, which are deposited using RF sputtering. It clearly indicates that ZnO based TFT using La_2O_3 as a gate dielectric shows superior performance than HfO_2 and ZrO_2 in terms of threshold voltage (V_T) and leakage current (I_{off}). The close match between outcome of this work and experimental results shows the validity of the proposed analysis for the low voltage and low leakage TFT. In order to improve other performance indices like mobility and SS, the

Table 6 VIKOR R_i, G_i and Q_i values with respective ranks

Dielectric	R_i	Ranking based on (R)	G_i	Ranking based on (G)	Q	Ranking based on Q
HfO_2	0.173076923	2	0.380140058	2	0.2267	2
ZrO_2	0.184615385	3	0.4389456	4	0.3184	3
$HfSiO_4$	0.291187739	9	0.603839436	11	0.7134	10
La_2O_3	0.130434783	1	0.256808409	1	0	1
$LaAlO_3$	0.207692308	4	0.455518395	5	0.3811	4
Ta_2O_5	0.3	10	0.62831965	12	0.759	12
Ga_2O_3	0.253846154	8	0.582305972	10	0.6184	9
Gd_2O_3	0.214559387	5	0.462568943	8	0.4022	5
Al_2O_3	0.32183908	11	0.430974293	3	0.5634	8
SiO_2	0.4	13	0.455714286	6	0.738	11
Si_3N_4	0.352490421	12	0.674678668	13	0.9119	13
Y_2O_3	0.229885057	6	0.469550609	9	0.439	6
Sc_2O_3	0.245210728	7	0.461832802	7	0.4582	7

Table 7 Experimental data for the validation of proposed analysis

Performance parameter	La_2O_3 [41]	HfO_2 [42]	ZrO_2 [43]
μ_{eff} (cm^2/V-s)	12.1	7.95	28
V_T (V)	1.85	2	3.2
I_{on}/I_{off}	1.5×10^7	4.1×10^8	4.8×10^7
I_{off} (A)	3.29×10^{-11}	2.2×10^{-9}	$\sim 10^{-10}$
SS (V/Dec)	0.234	0.215	0.560
Deposition technique	RF sputtering	RF sputtering	RF sputtering

ZnO deposition techniques can be optimized so that it results in less number of grain boundary and large grain size.

6 Conclusion

This paper highlighted the importance of high-κ dielectric for low voltage and low leakage ZnO TFT. The values of band offset of various dielectrics on ZnO TFT are calculated analytically. Three different material selection methodologies like Ashby, TOPSIS and VIKOR are used to find out the best gate dielectric material. Dielectric constant, band-gap, conduction band offset and thermal coefficient mismatch are used as material indices in these methodologies. These analyses converge that La_2O_3 is the most promising gate dielectric material for low threshold voltage and low leakage TFT. The result shows good agreement among Ashby, TOPSIS and VIKOR approaches.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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