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Effects of anodization duration on the properties of sputtered samarium thin films on silicon substrate

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Abstract Sm_2O_3 was formed by anodization of sputtered Sm thin film on Si substrate at 20 V for different durations (10–25 min). In this study, Sm_2O_3 thin film formed at anodisation duration of 10 min exhibited the best electrical properties with smallest Q_{eff} value (2.78×10^{23} cm^{-2}), lowest STD (2.91×10^{22} cm^{-2}), minimum D_{total} value (1.98×10^{24} cm^{-2}) and κ-value of 1.33 in capacitance–voltage (C–V) measurement. From leakage current density electric field (J–E) measurement, Sm_2O_3 thin film formed at anodisation duration of 10 min consisted of two breakdowns, whereby the first breakdown was 3.48 MV/cm at 10^{-5} A/cm^2 and the second breakdown was 9.39 MV/cm at 10^{-4} A/cm^2. This sample showed the highest breakdown electric field among all the samples. This type of oxide may be served as possible candidate as gate dielectric in metal–oxide–semiconductor-based devices.

1 Introduction

SiO_2 has been widely used in semiconductor technology due to its excellent insulator for decades [1]. This type of oxide can be grown directly from Si semiconductor substrate by thermal oxidation and is typically amorphous with a small number of electronic defects thus perfectly lattice-matched with Si substrate without formation of interfacial layer (IL) in between the semiconductor and the oxide [2]. This type of oxide has low dielectric constant (κ) and was developed in the commercial ultra-large-scale-integrated (ULSI)-based devices and has good adhesion property between various substrates [1, 2]. The first integration of low-κ dielectric into 90-nm logic devices with κ value of 2.9 in 1999 [1, 2]. However, due to the challenge of device miniaturization, according to the International Technology Roadmap for semiconductors (ITRS) 2012 [3, 4], fabrication of next-generation 10-nm logic devices with optimized intermediary dielectric layers of lower effective dielectric constants (<2.5) are needed.

Dielectric isolation with low-κ materials in between the interconnect lines or intermetallic dielectrics (IMD) with minimum capacitive coupling is necessary in order to fabricate devices with multilevel dielectrics thus producing a device with high circuit density, low power consumption, and high thermal conductivity properties [5]. Furthermore, low-κ materials with minimum possible thickness are also introduced [6].

SiO_2 has been applied as the ILD surrounding metallic and/or semiconducting wires [7], as it has demonstrated its advantages such as thermal and chemical stability and moisture-absorption resistance up to the process temperature of integrated circuits [7]. However, the drawbacks of SiO_2 outweighed its advantages. SiO_2 would face parasitic capacitance delays, crosstalk noise across layers, high power consumption, and resistance–capacitance (RC) delay [7]. A signal propagating through interconnects would experience RC delay [8]. In order to overcome the aforementioned problem, materials of reduced dielectric constant with high crystallinity and reduced dipole strength in the polar chemical bonds or the dipoles number could be a possible solution. In other words, this could be achieved by introducing material with lower polarizability than Si–O, such as Si–F and Si–C bonds; or lower density materials by adding porosity [constitutive (1 nm in diameter) and subtractive (>2 nm in diameter)] in the material [9].

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Lanthanide oxide materials may be a possible replacement for SiO_2 [2, 10]. Of lanthanide oxide materials, Sm_2O_3 is an attractive material to attain the comparable dielectric properties as SiO_2 and is thermodynamically stable on the underlying Si surface [2, 10]. However, Sm atoms would present in different oxidation state, while the coordination number of Sm(III) atoms with respect to oxygen varies from 4 to 12 and coordination number of Sm(II) is 5, 7, or 9, which will vary the stoichiometry of Sm_xO_y [10]. Therefore, this study was aimed to control the stoichiometry to form only Sm_2O_3. Hypothesis stated that stoichiometry of the oxide may improve the electrical properties by increasing the n-type conductivity and field-effect mobility [11]. According to the previous researches [12–15], it is reported that the oxide stoichiometry could be controlled by sputtering of metallic layer followed by formation of oxide. To date, there is no report on the formation of Sm_2O_3 by sputtering of metallic Sm layer followed by anodization technique. Hence, in this study, it is aimed to report the effects of anodization durations of a sputtered Sm/n-Si system on their structural, physical, and electrical properties.

2 Experimental procedure

2.1 Preparation of Si substrate

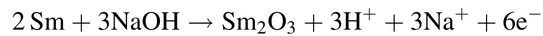
n-type and 100-oriented Si was used as starting substrate. The Si substrate was cleaned using standard RCA cleaning method and treated with diluted HF solution (1 HF: 50 H_2O) to eliminate native oxide before proceeded with sputtering process.

2.2 Sputtering process

Si substrates were placed under the samarium target in the RF magnetron sputtering system of Cesar RF Power Generator and SG Control Engineering Vacuum System to deposit 20 nm of samarium thin film, under low vacuum system of 3×10^{-5} torr pressure and 170 W power. Sputtering process was carried out under pure argon medium with the flow rate of 25 cm^3/min at room temperature. Prior to sputtering process, a pre-sputtering was undergo for 2 min to remove native oxide on the target surface and proceeded with 150 s of plasma-sputter to allow Sm to form thin film on Si. Then the confirmation of thickness for Sm/Si material was measured under Kla Tencor P-6 Stylus Profiler by comparing the optical path difference between a coated Sm surface and original Si substrate to give the accurate thickness of every point on the surface instead of taking the average thickness. Sm thicknesses deposited on Si were in the range of 21–22 nm.

2.3 Formation of samarium oxide gate dielectric

Anodising is the process of growing an oxide layer on the metal in the electrolyte medium, and the metal would lose electrons during the oxidation process.



$$2\,Sm + 3NaOH \rightarrow Sm_2O_3 + 3H^+ + 3Na^+ + 6e^-$$

Sm/Si material was taped on the copper holder and connected to the negative terminal of GW Instek GPS-30300, DC power supplies; whereas the positive terminal is connected to a platinum wire. The electrolyte used is 1 M of NaOH (pH = 14). Electroplating enables oxidation of Sm to form Sm_2O_3 on the Si substrate.

The anodisation voltage is fixed at 20 V and the anodisation times are varied from 10 to 25 min to obtain the desired electrical properties. Research showed that the activation energy for oxidation of Sm in required 90 kJ/mol (Nogami et al. [16]), and 10 min of anodisation duration is able to produce higher than 90 kJ/mol of energy to oxidised Sm metal. Hence 10 min is set as the starting point of anodisation duration to ensure complete anodisation of Sm to Sm_2O_3.

2.4 Metallization and photolithography process

Then, Sm layer was anodised using GW Instek GPS-30300 DC power supplies in 1 M of NaOH electrolyte. The parameters were varied from 10 to 25 V and 10–25 min to obtain the best characteristic among the combined parameters. Before carrying out the electrical characterization, the oxidised Sm films were fabricated into MOS. Al layer of 100 nm was thermally evaporated on the top of the film as gate electrode by using thermal evaporator under vacuum system of 3×10^{-6} mbar to avoid disturbance of Al deposition and 20 A of current was applied to the system. 3 mm diameter of Al electrode was deposited on the sample using shadow mask for electrical characterisation.

2.5 Physical characterization

Properties of the Si/Sm_2O_3 film were evaluated by PANalytical XRD X'Pert HighScore using low glancing angle X-ray diffraction (GAXRD) to identify crystalline surface phases and grain size of Sm_2O_3 with angle sweep from θ to 2θ with the scan speed of 0.026 θ/s. Besides that, transmission electron microscopy (TEM) TECNAI G2 F20 using accelerating voltage from 20 to 200 kV of electron beam and standard magnification from 22 x to 930 kx in an ultimate pressure camber of 2.7×10^{-5} Pa to observe the cross-section of MOS thin film and determine the presence of IL and the crystalline/semi-crystalline structure of Sm_2O_3. Prior to this, a Pt protective layer of resist was deposited on the top most layer of the sample to prevent

surface damage due to ion bombardment and it was ion-milled by a focused ion beam system [15].

2.6 Electrical characterization

The electrical properties of MOS capacitors were characterised through C–V and I–V measurement. In C–V measurement, high frequency (1 MHz) and applied DC voltage of 24 mV were introduced to MOS capacitance measured by Hewlett Packard 4194A Impedance/Gain-Phase Analyzer. Bias sweep was done in forward and backward cycle ranging from −5 to +1 V. I–V measurement at the frequency of 50 Hz and sweep mode was set at the range from 0 to 20 V using Keithley Instruments Model 236 Source Measure Unit to obtain the leakage current density against voltage (J–V) and leakage current density electric field (J–E) curves. From this measurement, current densities at different gate voltage and at various electric fields could be determined.

3 Results and discussion

The anodisation voltage was fixed at 20 V and the anodisation times were varied from 10 to 25 min to obtain the desired electrical properties. Research showed that the activation energy for oxidation of Sm in required 90 kJ/mol [16], and 10 min of anodisation duration was able to produce higher than 90 kJ/mol of energy to oxidised Sm metal. Hence 10 min was set as the starting point of anodisation duration to ensure complete anodisation of Sm to Sm_2O_3.

3.1 XRD analysis

Figure 1 displayed the XRD pattern of Sm anodised at various time (10–25 min) on Si substrate. According to International Centre for Diffraction Data (ICDD) card number 98-003-3650, cubic-Sm_2O_3 appeared at $2\theta = 27.8°$, 33.0°, 47.8°, 49.5°, 54.5°, 56.4°, 61.7°, and 75.6° in small concentration (relative intensity ≈ 0.01–0.25 %) as compared to the strong Si substrate peak at 69.2° in Fig. 1 [17–19].

Besides that, the two diffraction peaks at $2\theta = 47.8°$ and 54.5° were associated with hexagonal-Sm_2O_3 and monoclinic-Sm_2O_3 respectively [20]. Paper of Yang et al. [21] also stated that Sm_2O_3 exists in three types of crystal structures at room temperature: cubic, hexagonal and monoclinic. Furthermore, two humps which was located at $2\theta = 30.0°$ and 61.7° could be observed in the XRD profile, which might be belonged to the amorphous phase of IL which required further clarification.

Figure 2 showed the grain size and intensity of cubic-Sm_2O_3 at various time (10–25 min), based on the three highest peak, $2\theta = 33.0°$, 61.7° and 75.6°. While Fig. 3 showed the grain size and intensity of mixture hexagonal and cubic-Sm_2O_3 ($2\theta = 47.8°$) and monoclinic and cubic-Sm_2O_3 ($2\theta = 54.5°$) at various time (10–25 min).

The grain size of the cubic-Sm_2O_3 could be obtained through Scherrer equation [22]

$$D = \frac{K\lambda}{\beta cos\theta} \quad (1)$$

where, D was the grain size, K was the shape factor, also equal to 0.9, λ was the X-ray wavelength, β was the line broadening at full width at half maximum (FWHM) and θ was the Bragg angle. In XRD analysis, instrumental broadening which might be contributed by source of radiation (X-ray) with finite physical size [23], should be subtracted from the observed line broadening to give the accurate 2θ and hence predicted the grain size more accurately.

XRD intensity peaks of cubic-Sm_2O_3 in Fig. 2 showed the intensities were in the range of 18,000–20,000 a.u. over

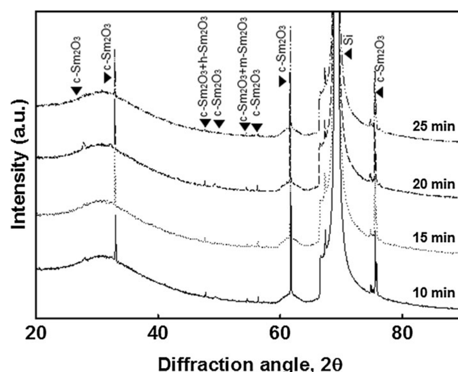


Fig. 1 XRD pattern of anodised Sm_2O_3 at various time (10–25 min) on Si substrate

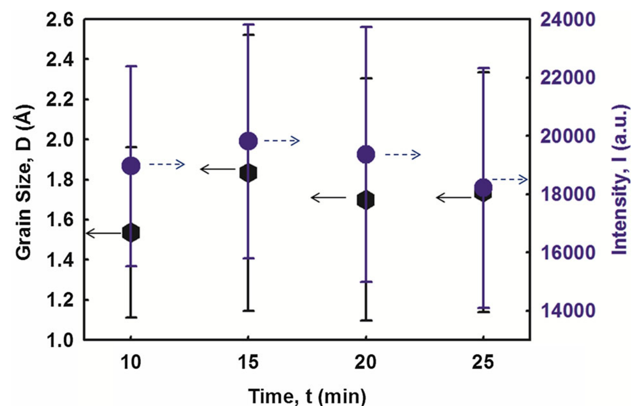


Fig. 2 Grain size and intensity of cubic-Sm_2O_3 at various time (10–25 min)

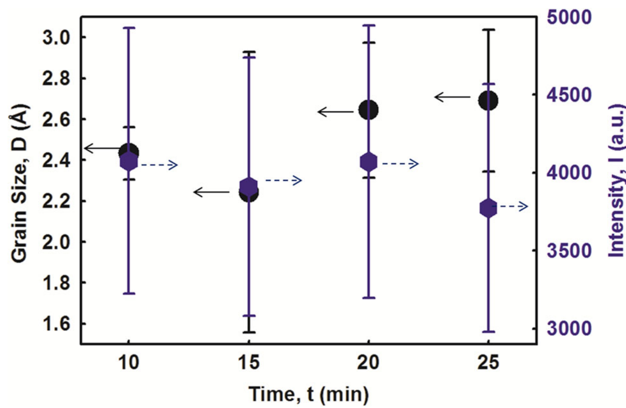


Fig. 3 Grain size and intensity of hexagonal-Sm_2O_3 (2θ = 47.8°) and monoclinic-Sm_2O_3 (2θ = 54.5°) at various time (10–25 min)

the time of anodisation and with the highest mean peak intensity of 10 min anodisation (I ≈ 19637.9 a.u.). Besides that, Sm_2O_3 thin film anodised for 10 min exhibited the smallest grain size (1.55 Å), which would have more grain boundaries thus contributed to electromigration effects and resulted in decreasing current density [24].

Moreover, the intensity profile of Fig. 3 showed almost similar trend as Fig. 2, as Sm_2O_3 thin film anodised for 10 min has the highest intensity of mixture hexagonal-cubic-Sm_2O_3 and monoclinic-cubic-Sm_2O_3 peaks (4080.69 a.u.) and the lowest peaks intensity was 25 min anodisation (3778.41 a.u.). However, the grain size of 10 min Sm_2O_3 anodisation (2.40 Å) was slightly higher than 15 min anodisation (2.28 Å), this might be due to lower monoclinic concentration present in 15 min anodisation Sm_2O_3 as the peak of 2θ = 54.5° were hardly observed in Fig. 1. Theoretically, monoclinic crystal structure was less closely packed as compared to cubic and hexagonal structure.

Furthermore, the grain size of mixture hexagonal and cubic-Sm_2O_3 (2θ = 47.8°) and monoclinic and cubic-Sm_2O_3 (2θ = 54.5°) were averagely 2.50 Å for four samples as showed in Fig. 3, which was comparably bigger than cubic-Sm_2O_3 (averagely 1.69 Å). Thus, the peaks 2θ = 47.8° and 54.5° were highly possibly mixture of polycrystalline structure.

Paper of Yori and Parera discussed the influence of crystalline structure on the metallic properties. Monoclinic-semiconductor lost its metallic properties while tetragonal-semiconductor would enhanced the metallic properties [25]. Ideally, metallic properties should be minimised to reduce the current density in the MOS system. Hence, monoclinic structure would improve the electrical properties and dielectric constant as showed in 10 min anodisation with the highest peak of 2θ = 54.5° (4074.77 a.u.).

On the other hand, cubic-semiconductor has a narrower bandgap which aided to improve the electrical properties as compared to the hexagonal-semiconductor [26] and Fig. 1 showed the 10 min anodisation has the highest cubic-Sm_2O_3 peaks intensity. Furthermore, cubic-Sm_2O_3 exhibited better properties as compared to monoclinic and hexagonal structure as it was the most stable phase at atmospheric pressure and room temperature [21].

3.2 TEM analysis

Figure 4 showed the TEM images of the MOS layer of Si–Sm_2O_3 which undergo 20 V of anodisation voltage and various anodisation durations: (a) 10 min and (b) 15 min. The t_{ox} of 10 min and 15 min anodisation were 19.8 ± 0.6 and 23.0 ± 0.3 nm respectively. The thickness increased as the anodisation time increased because longer oxidation process was able to carry out at deeper depth to ensure fully oxidation.

The Sm_2O_3 XRD pattern appeared to be sharp peaks, which suggested to be exhibiting crystallinity property and polycrystalline structure of bulk oxide could be observed in TEM images as patches of lattice fringes with interplanar spacing, d range from 0.242 to 0.254 nm was measured using ImageJ software. The measured values were matched with the XRD cubic-Sm_2O_3 peaks. However, the grain size observed in TEM images was bigger than the calculated values according to the XRD peaks, this could be the

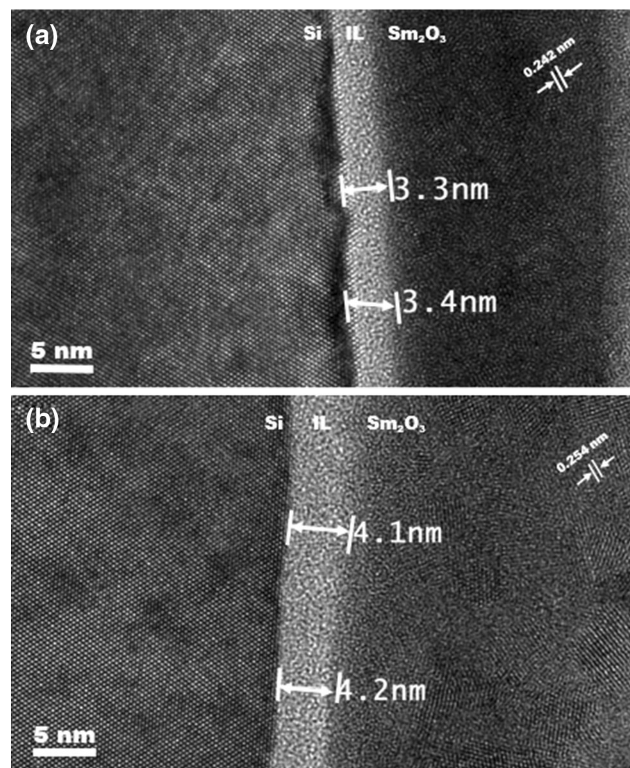


Fig. 4 TEM images of the MOS of Sm_2O_3-Si layer undergo 20 V anodisation voltage and various anodisation durations: **a** 10 min and **b** 15 min

reason due to the crystal alignment. In TEM images were obtained through the side-view, while the XRD measurements were observed through the top view of the samples, which provided dissimilar in grain size values [15].

The existence of SiO_2 IL would limit the gate stack capacitance and reduced the EOT value [27]. However, the region near to the IL with different crystal alignment, was suspected to be $Sm_xSi_yO_z$, which required further verification. For efficient operation of a device, the IL should be minimized during the etching process during RCA-cleaning to lessen the interfacial charge and improved the channel mobility [28]. The presence of IL was observed by TEM analysis as result showed 10 min of anodisation time would provide the smallest IL which ranged from 3.3 to 3.4 nm and as resulted it exhibited better electrical properties as shown in C–V measurement as compared to 15 min anodisation.

3.3 Electrical properties

3.3.1 C–V measurements

C–V measurement was introduced by Frankl in 1961 for MOS characterization. High frequency (1 MHz) C–V curves measured at room temperature were shown in the Fig. 5 at various anodisation duration from 10 to 25 min. The gate bias sweep was done forward and backward cycle ranging from −5 to +1 V.

Figure 5 showed hysteresis curve of 10 min and 20 min anodisation have less positively charge accumulated in the Sm_2O_3 thin film, while 20 min of anodisation displayed the highest capacitance of 4444.36 pF. However, 10 min of anodisation exhibited the smallest different between the forward bias and reverse bias, $\Delta V = 0.0839$ V.

Figure 6 presented the dielectric constant of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation. Dielectric constant of Sm_2O_3 thin film in Fig. 6 was obtained from the formula

$$C_{OX} = \frac{\kappa \varepsilon_0 A}{t_{ox}} \quad (2)$$

where, C_{ox} represented the capacitance of Sm_2O_3 in different MOS sample, ε_o was the permittivity of free space (8.85×10^{-12} F/m), A was the area of Al metal gate (0.07069 cm^2) and t_{ox} was the average of thickness between IL and Sm_2O_3 (21.4 nm), obtained from TEM image measured using ImageJ software from the TEM images.

The dielectric constant of Sm_2O_3 thin layer was highest in 20 min anodisation duration sample, κ-value ≈ 1.52. The low κ-value (0.93–1.52) displayed in Fig. 6 might due to the κ-value of $Sm_xSi_yO_z$ governed the bulk κ-value of Sm_2O_3, instead of obtaining the theoretical κ-value of 9–13.

Figure 7 showed the Q_{eff} of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation. The V_{FB} was shifted negatively which indicated the present of positive Q_{eff}. Q_{eff} was the summation of oxide fixed charge (Q_f), mobile ionic charge (Q_m) and oxide trapped charge (Q_{ot}) [29].

$$Q_{eff} = Q_f + Q_m + Q_{ot} \quad (3)$$

Q_f was the charges accumulated near the SiO_2/Si interface, and Q_{ot} was due to charges trapped in the oxide, while Q_m was negligible as ionic impurities was removed during RCA-cleaning to eliminate the mobile charges [30]. The Q_{eff} of Sm_2O_3 thin film in Fig. 7 was calculated from the formula

$$Q_{eff} = \frac{(\Delta V_{FB})C_{ox}}{qA} \quad (4)$$

where, q was the electric charge, approximately equal to 1.602×10^{-19} C [15].

Figure 8 displayed the STD of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation. The STD was the charges trapped in Sm_2O_3 thin film and was plotted from the formula [15].

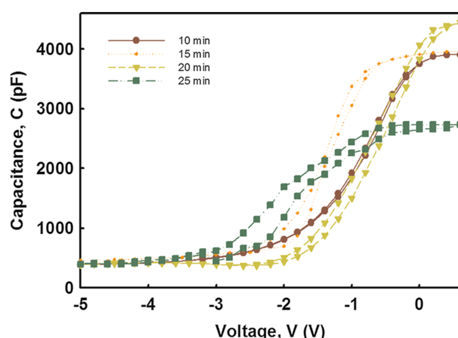


Fig. 5 C–V characteristics of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation

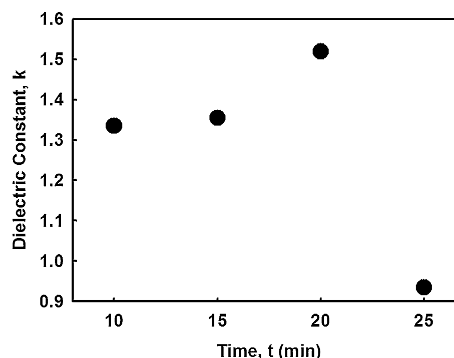


Fig. 6 Dielectric constant of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation

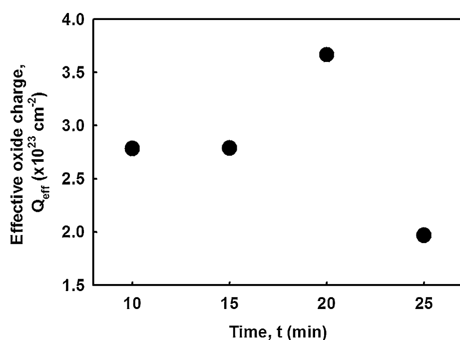


Fig. 7 Effective oxide charge of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation

$$STD = \frac{(\Delta V)C_{ox}}{qA} \quad (5)$$

25 min anodisation achieved the lowest Q_{eff} (1.97×10^{23} cm^{-2}) but highest STD value (7.56×10^{22} cm^{-2}). STD occurred at the oxide of MOS which was the governing factor, should be kept as low as possible. Figure 8 showed 10 min anodisation had the lowest STD (2.91×10^{22} cm^{-2}) as it had the smallest ΔV (0.0839 V) as shown in Fig. 5.

Figure 9 was the plot of average D_{it} of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation and the formula was given as

$$D_{it} = \frac{\Delta V_g C_{ox}}{\varphi_s qA} \quad (6)$$

where ϕ_s was the surface potential of Si at specific gate voltage, V_g [15]. The value of D_{it} obtained in this work was $\sim 10^{24}$ eV^{-1}/cm^2 at ϕ_s in the range of 0.039–0.273 eV. Interface traps were distributed randomly in the energy across the band gap. D_{it} in a device should be maintained at low quantity to avoid the electron carriers accumulated at the interface and reduced the conduction current [31].

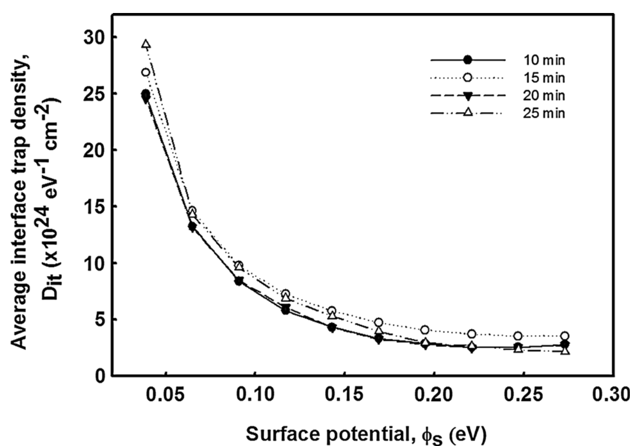


Fig. 9 Average interface–trap density of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation

Figure 10 was the total interface–trap density, D_{total} of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation. D_{total} was calculated from the area under the D_{it} curve in Fig. 9. D_{total} sometimes also known as structural imperfection, Si–Si were stably bonded in tetrahedral structure, but oxidation of Si would reduce the closely packed structure at IL due to bonding between Si and oxygen was tangled out at the surface and also lattice mismatched of the Sm–Si bond, which increased the IL thickness [30].

Smaller D_{total} value indicated the thinner IL and allowed more charges/carriers transferred in the MOS system, this property was exhibited by 10 and 20 min anodisation duration of Sm_2O_3-Si MOS, which were 1.98 and 1.97×10^{24} cm^{-2} respectively.

3.3.2 J–E measurement

Figure 11 was the J–E measurement of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation. The J–

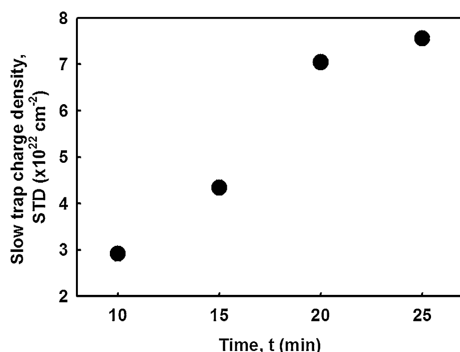


Fig. 8 Slow trap density of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation

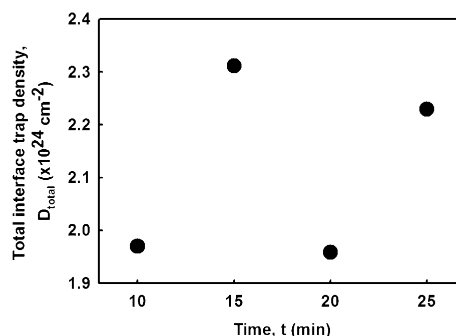


Fig. 10 Total interface–trap density of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation

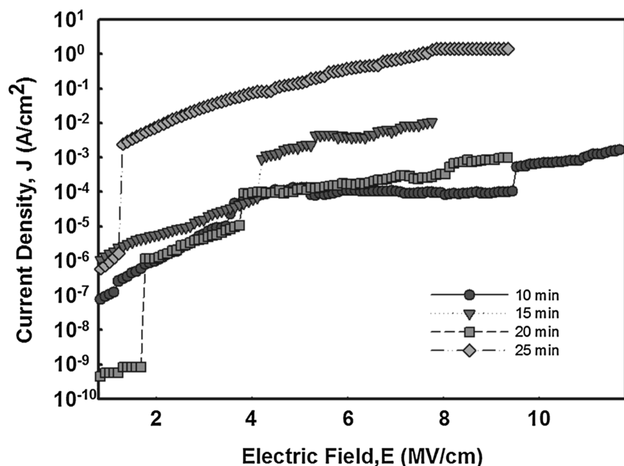


Fig. 11 J–E measurement of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation

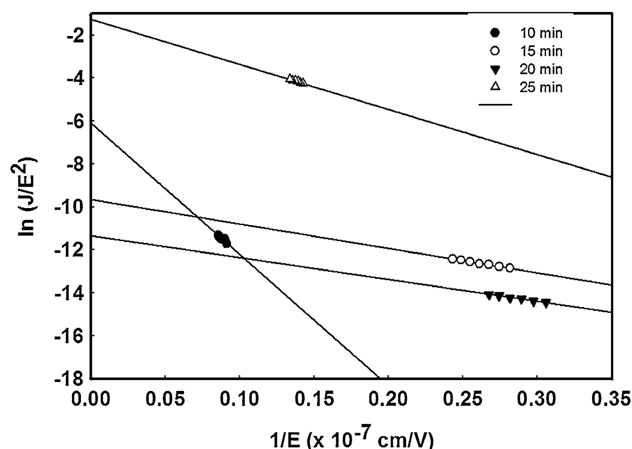


Fig. 12 FN tunneling linear regression plot [ln(J/E^2)–1/E] of Sm_2O_3–Si MOS at various time (10–25 min) with 20 V of anodisation

E measurement in Fig. 4.11 was derivate from the I–V measurement. Electric field (E) was defined as first determining the V_{FB} from the V_g and divided by the summation of Sm_2O_3 and IL thicknesses (t_{ox}) measured by TEM [32].

$$E = \frac{V_g - V_{FB}}{t_{ox}} \tag{7}$$

Dielectric breakdown was occurred in insulating material becoming electrically conducting when exposed to a strong electric field or voltage applied. The material lost its insulator properties when exceeded its breakdown voltage, resulting in sudden increased or “jump” in current density, showed in Fig. 11. The breakdown might be due to surface flashover and semiconductor bulk breakdown, which was contributed by the defect distribution and contact between the IL.

The existence of two-steps breakdown was due to the presence of IL and Sm_2O_3, where the first breakdown at the lower field was contributed by IL between Si and Sm_2O_3, followed by second breakdown due to Sm_2O_3 [32]. The

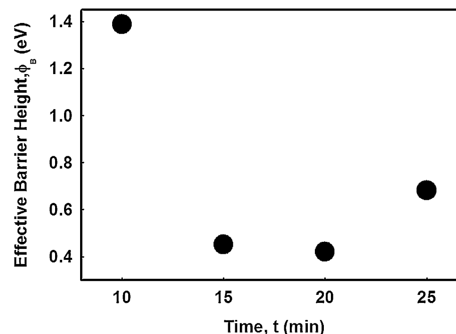


Fig. 13 Barrier height values as function of anodisation duration

concentration of the carrier increased until the layer was electrically broken down at higher electric field. Besides that, first breakdown of 10 and 20 min anodisation duration were having larger instantaneous increment of current density compared to the second breakdown, also known as hard breakdown and was governed by IL. However, 10 min of anodisation duration broken down at first breakdown was 3.48 MV/cm at 10^{-5} A/cm^2 and the second breakdown, also the highest breakdown electric field among four samples, which was 9.39 MV/cm at 10^{-4} A/cm^2.

Barrier height (ϕ_B) of conduction band edge between Si and the IL was extracted from Fowler–Nordheim (FN) tunneling model. FN tunneling was referred to the flow of electron through a triangular potential barrier into conduction band of an insulator. The J attributed to FN tunneling (J_{FN}) can be defined as follow:

$$J_{FN} = AE^2 \exp\left(-\frac{B}{E}\right) \tag{8}$$

$$A = 1.54 \times 10^{-6}\left(\frac{m}{m_{ox}\phi_B}\right) \tag{9}$$

$$B = 6.83 \times 10^7 \left(\frac{m_{ox}\phi_B^3}{m}\right)^{1/2} \tag{10}$$

Figure 12 showed a linear FN plot of ln (J_{FN}/E^2) versus 1/E, and thus ϕ_B was obtained from the intercept of the plot yields A and gradient of the slope yields B. m* was the effective electron mass in the oxide, where, $m^* = 0.3\ m_o$, in which, m_o was the free electron mass [12]. The calculated ϕ_B values for the samples as a function of measured anodisation duration was presented in Fig. 13. The highest barrier height was exhibited by 20 min anodisation samples (0.255 eV).

4 Conclusion

Sm thin films were successfully deposited on the Si substrates by RF magnetron sputtering and oxidised to Sm_2O_3 with various anodisation duration (10–25 min) and voltage

(10–25 V). The Si–Sm_2O_3 MOS was then underwent chemical and electrical characterisation to determine the phase analysis and best electrical properties for capacitor. The average cubic-Sm_2O_3 of XRD peak intensity of Sm_2O_3 sample anodised at 20 V was the highest (16564.8 a.u.) with all the cubic-Sm_2O_3 could be observed distinctively in Fig. 1. Besides that, Sm_2O_3 thin film anodised for 10 min exhibited the smallest grain size (1.55 Å). On the other hand, Sm_2O_3 thin film anodised for 10 min has the highest XRD peaks intensity of mixture hexagonal-cubic-Sm_2O_3 and monoclinic-cubic-Sm_2O_3 peaks at $2\theta = 47.8°$ and 54.5° (4080.69 a.u.) and with the grain size of 10 min Sm_2O_3 anodisation (2.40 Å). TEM images showed the polycrystalline structure of Sm_2O_3 with lattice fringes of interplanar spacing range from 0.242 to 0.254 nm and average t_{ox} of 21.4 nm.

The low κ-value (0.93–1.52) exhibited by anodised Sm_2O_3 thin film instead of obtaining the theoretical κ-value of 9–13 was due to high concentration of charges was trapped at the IL, which can be overcome by introducing nitration process during sputtering or anodisation. As the vacant in IL is filled by nitrogen atom and hence reduced the Q_{eff}, STD and D_{it}.

As conclusion, 10 min of anodisation duration was preferable as obtained the highest breakdown current density (9.39 MV/cm at 10^{-4} A/cm^2) in J–E characteristic. From the C–V characteristic analysis, 10 min anodisation duration also showed the smallest ΔV (0.0839 V), lowest STD (2.91×10^{22} cm^{-2}) and smallest D_{total} value (1.98×10^{24} cm^{-2}) which was the main governed factors. Although the recorded STD and D_{total} of Sm_2O_3 were higher than that of SiO_2 [2], this type of oxide was able to reduce the leakage current density. Therefore, Sm_2O_3 was suitable was replace SiO_2 as it was able to overcome parasitic capacitance delays, crosstalk noise across layers, high power consumption and RC delay.

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