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Solid state bonding of silicon chips to copper substrates using silver with cavities

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Abstract Silicon (Si) chips were bonded to copper (Cu) substrates using 10 μm silver (Ag) layer as the bonding medium. Neither solder nor flux was used. The bonding was achieved by solid state bonding mechanism. The Ag layer was first plated onto Si chips coated with chromium and gold. The Si chips were then bonded to Cu substrates at 300 °C with a static pressure of 600–1000 psi (6.9 MPa) for 5 min in 0.1 torr vacuum. To assist deformation and flow of the Ag layer during bonding, array of cavities was fabricated in the Ag layer. Because of the cavities, the bonding pressure could be reduced to 600 psi (4.1 MPa). Despite significant coefficient of thermal expansion (CTE) mismatch between Si and Ag, no sample broke. Cross-section SEM images show that Ag layer on Si chips was well bonded to Cu substrates without voids. Shear test was performed on six samples. The breaking force of five samples passes MIL-STD-883H requirement. Fracture analyses reveal that only 6.2–7.5 % of the Ag layer surface was actually bonded to the Cu substrate. There is still room to improve to increase the breaking force.

1 Introduction

A wide variety of bonding media are available on the market to attach device chips to substrates or packages. The most popular media include conductive adhesives, lead-free tin-based solders, eutectic gold-tin solders, and sintered silver (Ag) nano-pastes [1–4].

In this research, pure Ag was selected as the bonding medium because of its superior physical properties, high ductility, and high melting temperature. The substrates are made of copper (Cu) as it is the most common electrode and package bond pad material. The bonding process is a solid-state process without molten phase involved. Successful solid state bonding requires the Ag surface to deform and conform to the Cu surface within atomic distance. To assist the deformation and plastic flow of Ag during bonding, an array of cavities is first produced on the Ag layer. These cavities provide space for the extra Ag to flow into. Thus, the Ag flow distance is reduced from half of the chip size to half of the pitch of the array. In other words, the flow requirement is changed from global movement to local movement that is determined by the pitch of the cavity array.

In what follows, bonding mechanism is first presented. Experiment designs and procedures are described. Experimental results are reported and discussed, followed by a summary.

2 Quantum mechanics bonding mechanism

Our fundamental concept of solid-state bonding refers to the situation when the spacing between A atoms and B atoms is brought within atomic distance so that there is interaction between them. On the atomic interface, if A atoms and B atoms can share outer electrons, bonding between materials A and B will occur. The ability of materials A and B to share outer electrons depends on their electronic configurations. The bonding theory based on quantum mechanics was recently reported [5]. According

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to this theory, the distance between Ag and Cu atoms on the interface has to be brought within 1 nm to achieve bonding strength of practical use. This provides a guideline on the maximum atomic distance required to achieve bonding. Therefore, the bonding medium needs to deform easily in order to achieve atomic contact with the object to be bonded.

3 Experimental design and procedures

In experiments, the solid-state bonding process of the Cu-Ag interface is performed at 300 °C with 1000, 800 and 600 psi of applied pressure, respectively. In the design, 2-dimensional array of cavities are provided in the Ag layer for the bonding medium to flow into so that intimate interfacial contact can be achieved at low bonding pressure. The 300 °C bonding temperature assists the Ag layer to deform to conform to the Cu surface profile. Figure 1 illustrates the process flow of photolithography and solid state bonding of Ag joint with cavities. The 10 mm × 12 mm Cu substrates are cut from a 0.8 mm thick Cu sheet having 99.9 % purity with mirror finish on one side. They are slightly polished with 0.5 µm diamond-suspended solution and rinsed with acetone and deionized water right before bonding to remove contaminations and oxides. To fabricate Si chips, 2-in. Si wafers are deposited with 30 nm Cr and 100 nm Au thin films by E-beam evaporation in one high vacuum cycle at 1×10^{-5} torr. The Cr serves as the adhesion layer and Au is the seed layer for electroplating. AZ P4620® photoresist (PR) of 10 µm in thickness is coated uniformly on Si wafers by spinning at 2000 rpm for 40 s. Using photolithographic process, arrays of 25 × 25 photoresist columns with 100 µm in diameter and 200 µm in pitch are produced on the Si wafer. After photolithographic process, the thickness of photoresist is measured by Dektak 3 Profilometer. The Si wafers are diced into 6 mm × 6 mm chips for electroplating and solid state bonding experiments.

Ag layer of 10 µm in thickness is electroplated on the Si chip with arrays of photoresist columns. The Ag plating bath is a cyanide-free, mild alkaline plating solution at pH of 10.5 containing 5–8 % potassium hydroxide (KOH) and 2–3 % silver oxide. The Ag plating is conducted with current density 13 mA/cm^2 at room temperature. The current, voltage, temperature, and time are monitored closely during the plating processes. Afterwards, the arrays of photoresist columns are removed by soaking in acetone at room temperature. The Si wafers are then ultrasonically cleaned in isopropyl alcohol (IPA) bath. The Cu substrates and the resulting Si chips are ready for bonding.

To achieve solid-state bonding, the Si chip with Ag patterned layer is placed over the Cu substrate. They are held together by a fixture with static pressure of 1000 psi (6.9 MPa) to ensure intimate contact. The assembly is loaded on a graphite stage in a vacuum oven, which is then pumped to 0.1 torr [6]. The graphite stage is heated to 300 °C for 5 min. The heater is then shut off and the assembly cools naturally in 50 millitorrs vacuum. It takes about 90 min to cool to room temperature. The purpose of vacuum environment is to suppress Cu oxidation. Several samples are cut in cross section along one complete row of cavities in the Ag joint and polished. Scanning electron microscopy (SEM) and optical microscopy (OM) are used

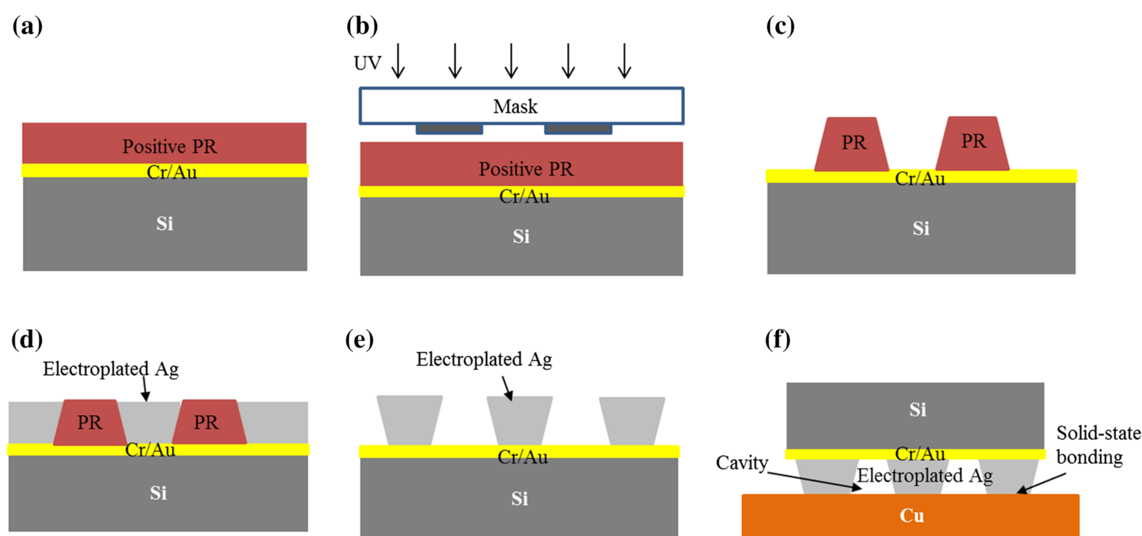

Fig. 1 Photolithographic and solid state bonding process flow of the Si chip with Ag layer having array of 100 µm cavities bonded to a Cu substrate, here PR stands for photoresist. **a** Spin coating, **b** soft baking and UV exposure, **c** developing and hard baking, **d** Ag plating, **e** photoresist removal and **f** solid-state bonding

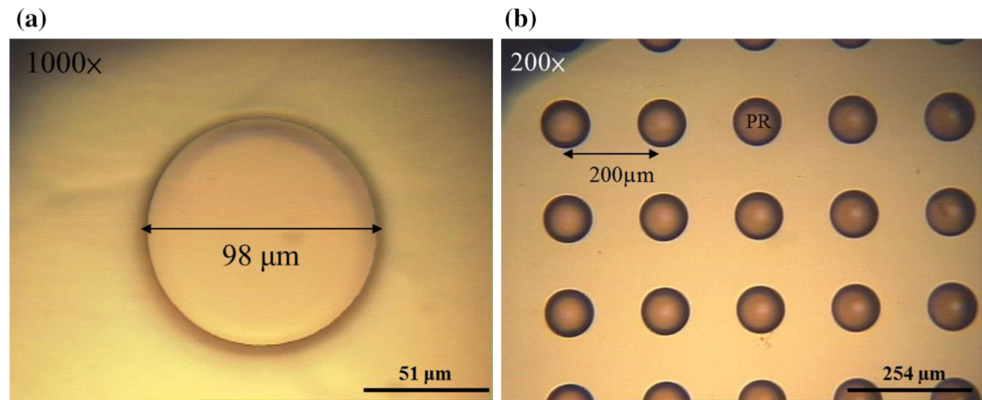

Fig. 2 Optical microscopy images of photoresist column array having 100 μm in diameter and 200 μm in pitch on Si chip: **a** ×1000, and **b** ×200

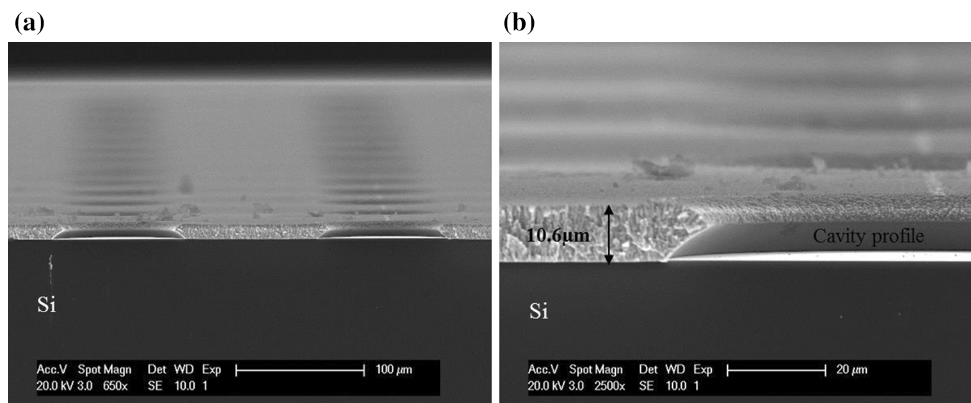

Fig. 3 Secondary electron images on the cross section of a sample showing cavity profile and Ag layer thickness: **a** ×650, and **b** ×2500

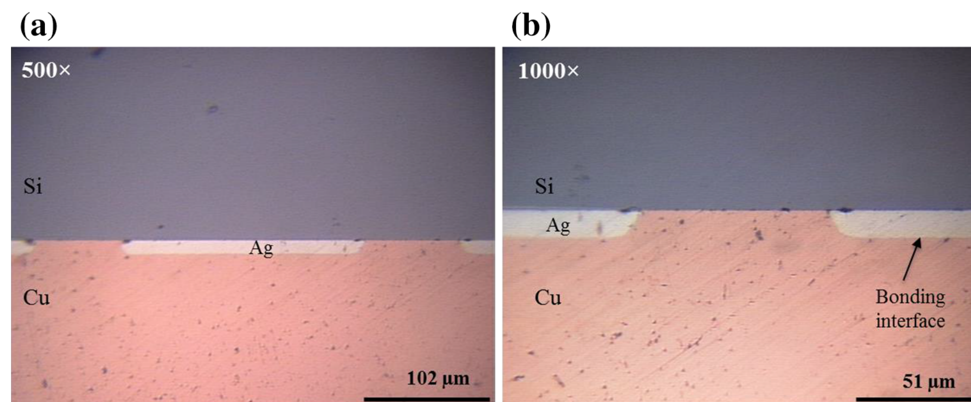

Fig. 4 Cross section OM images of a sample bonded between Si chip and Cu substrate 1000 psi pressure: **a** ×500, and **b** ×1000

to study the morphologies and quality of interfaces. Shear test is performed to measure the strength of Ag joints. The fracture modes are evaluated and analyzed.

4 Experimental results and discussion

Using photolithographic process, photoresist columns were fabricated on silicon chips. Ag layer was electroplated on the Si chips and the photoresist columns were stripped. On each Si chip, an array of 25 × 25 cavities with diameter of 100 μm and pitch of 200 μm was produced on the Ag layer. Figure 2a shows the OM image of photoresist columns with 100 μm in diameter. The pitch of photoresist column is 200 μm, as shown in Fig. 2b. A sample plated with Ag having cavities was cut in cross section to display the cavity profile and the Ag thickness, as shown in Fig. 3. The SEM image exhibits that the thickness of Ag layer is well controlled in range 10–11 μm. The cavity profile indicates lager diameter at the bottom, which helps

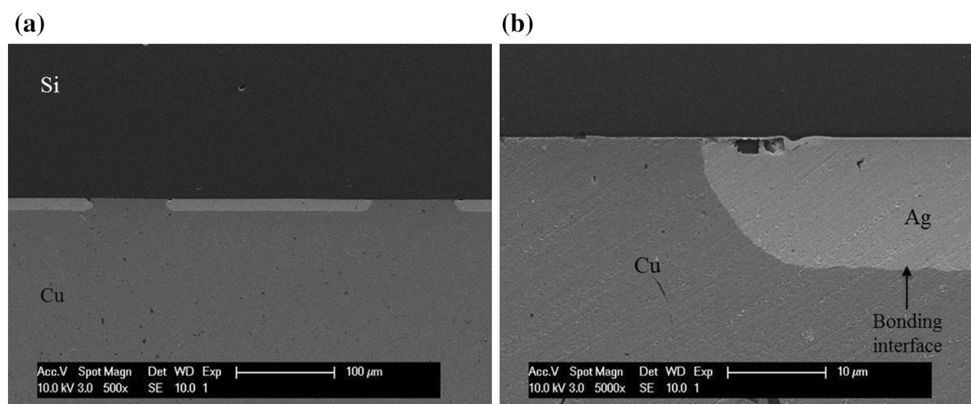

Fig. 5 Cross section SE SEM images of a bonded sample of Fig. 4: **a** ×500, and **b** ×5000

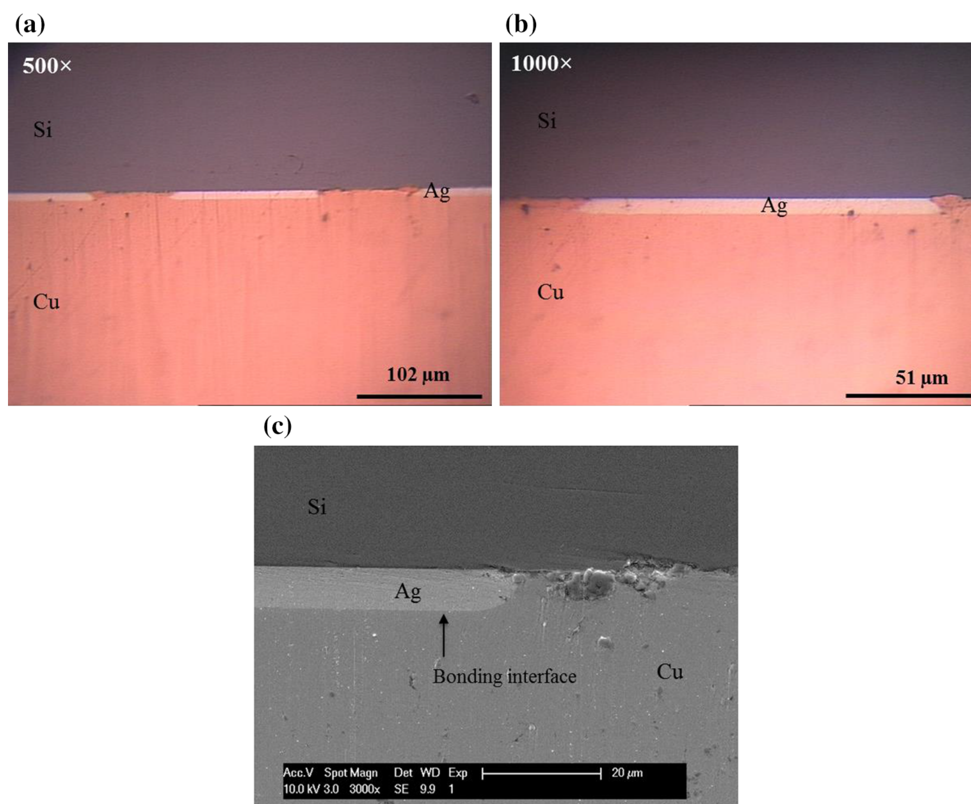

Fig. 6 Cross section OM and SE SEM images of a sample bonded with 800 psi pressure: **a** low magnification OM image, **b** high magnification OM image, and **c** SE SEM image

deformation of Ag layer during the bonding process. The Si chip with patterned Ag layer was flipped over and bonded to Cu substrate by solid-state bonding at 300 °C for 5 min with 1000 psi pressure in 0.1 torr vacuum. Neither underfill nor flux was used.

After bonding, samples were cut along one complete row, polished and examined under optical microscope and SEM. Figure 4 displays the cross section OM images of a typical bonded sample. It is seen that the Si chip and the Cu substrate are well bonded despite significant mismatch in coefficient of thermal expansion (CTE) between Si and Cu. It is interesting to observe that Cu has flowed in and filled the cavities completely. In Fig. 5, the secondary electron (SE) SEM images show sharp bonding interface without voids or gaps. Since Cu filled up the cavities, 1000 psi of bonding pressure is

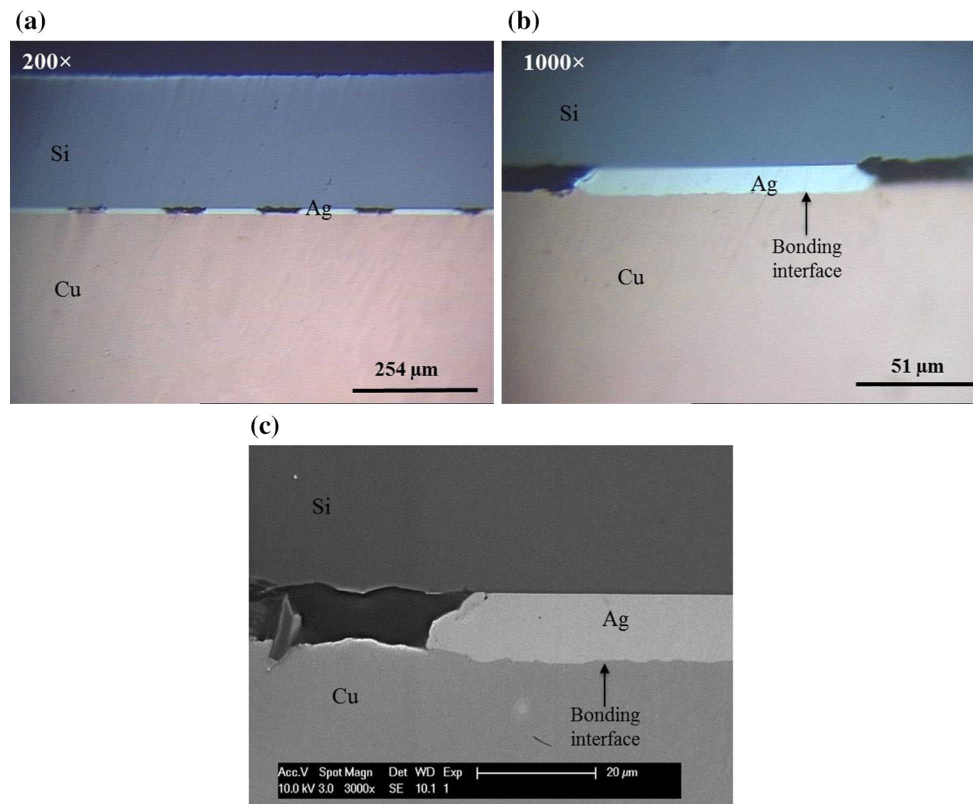

Fig. 7 Cross section OM and SE SEM images of a sample bonded with 600 psi pressure: **a** low magnification OM image, **b** high magnification OM image, and **c** BSE SEM image

more than enough. Thus, the pressure is reduced to 800 psi (5.5 MPa). Figure 6 displays the cross section OM and SE SEM images of bonding results. It is clearly seen that the cavities are still filled by Cu completely. From SE SEM image in Fig. 6c, the Si chip and the Cu substrate are still bonded with pressure of 800 psi. Subsequently, the pressure was reduced down to 600 psi (4.1 MPa). Figure 7 displays the cross section OM and BSE SEM images of a typical bonded sample. Figure 7a shows that the cavities are empty without Cu. The SE SEM image indicates that the Si chip is well bonded to the Cu substrate without visible voids or gaps. The bonding interface is very sharp, showing that both Ag and Cu deform to achieve intimate contact.

Despite the large CTE mismatch between Si and Cu, of all samples made with bonding pressure ranging from 600 to 1000 psi, the Ag joints or Si chips did not break. This indicates that all the interfaces including the Ag–Cu bonding interface of the bonded structure are strong enough to withstand the stresses developed due to the CTE mismatch. A commonly used indicator for evaluating the severity of CTE mismatch is the maximum shear strain without stress. It is the strain calculated assuming that both bonded objects are free to contract during cooling down. It is the maximum possible shear strain on the resulting joint and is given by [7],

$$\gamma = (\alpha_1 - \alpha_2)(T_2 - T_1)L/2h \qquad (1)$$

where α_1 and α_2 are the CTE of Si and Cu, respectively, T_2 is the bonding temperature for solid state bonding, T_1 is the room temperature, L is diagonal length of Si ship, and h is the joint thickness. For this bonding structure design, the maximum shear strain without stress is calculated to be 1.24. This is a relatively large value compared to typical solder joints [8]. Moreover, the samples did not break. To find out how strong it is, shear test was performed.

Six samples bonded at 300 °C with 600 psi bonding pressure were fabricated for shear test. Before bonding, each Cu substrate was slightly polished and rinsed with acetone and deionized water to remove contaminations and oxides. Si chips were coated with Cr and Au by E-beam evaporation, followed by photolithographic processes to fabricate an array of photoresist columns. Ag was plated on the resulting Si chips with 10–11 µm in thickness. After removing the photoresist with acetone, cavities were formed in the Ag layer on the Si chips. During the test, the sample was mounted on the stage. A tool wedge pushed on one 5 mm-wide edge of the Si chip of the sample at a

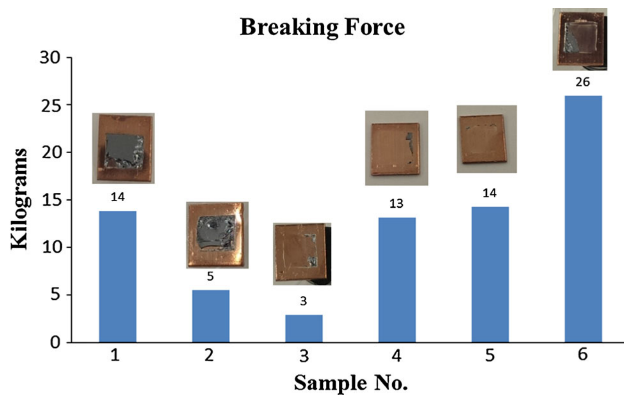

Fig. 8 Breaking force *bar chart* of six samples shear tested with the breakage force of each sample indicated. For sample nos. 1 and 2, the Si chip broke first. For the rest of samples, the Si chip was sheared off

constant speed of 350 μm/s. Figure 8 presents the shear test results of six samples with sample photos. There are two fracture modes. One is Si chip breakage and the other is joint fracture. For sample nos. 1 and 2, the Si chip broke first. Thus, the breaking force measured is not the real breaking force of the joint. It simply indicates that the Ag joint is stronger than the Si chip. For the other four samples, the Si chip was sheared off. The breaking force is 3, 13, 14, and 26 kg, respectively. According to military standards MIL-STD-883H method 2019.8 [9], a force higher than 5 kg is considered passing the die shear test. All samples pass the requirement specified in MIL-STD-883H standard (5 kg) except sample no. 3. To find out the reason of low and high breaking forces, test samples nos. 3 and 6 that have the lowest and highest breaking force, respectively, were examined.

Figure 9 presents the OM and SE SEM images of the fracture surface on Cu and Si sides, respectively, of sample no. 3. Based on OM image on the Cu side, the fracture occurs inside the Ag joint. It shows that the Ag joint was bonded onto the Cu substrate. However, bonding was not achieved across the entire bonding interface. On Fig. 9b Ag traces remained bonded to the Cu substrate can be clearly seen. The amount of Ag traces decreases from the left-hand side to the right-hand side on the Cu substrate. It shows that only a small percentage of the bonding interface achieved bonding and the bonding locations are not uniform over the area. On Fig. 9d, it is seen that the diameter of cavity shrank from 100 to 75 μm during bonding. This shows that some Ag did deform and flow into the cavities. For sample no. 6, Fig. 10a, b show that the Ag traces are more uniformly distributed than that of sample no. 3. On Fig. 10d, diameter of cavity shrank to 76 μm during bonding. The Ag traces are the Ag that remained bonded

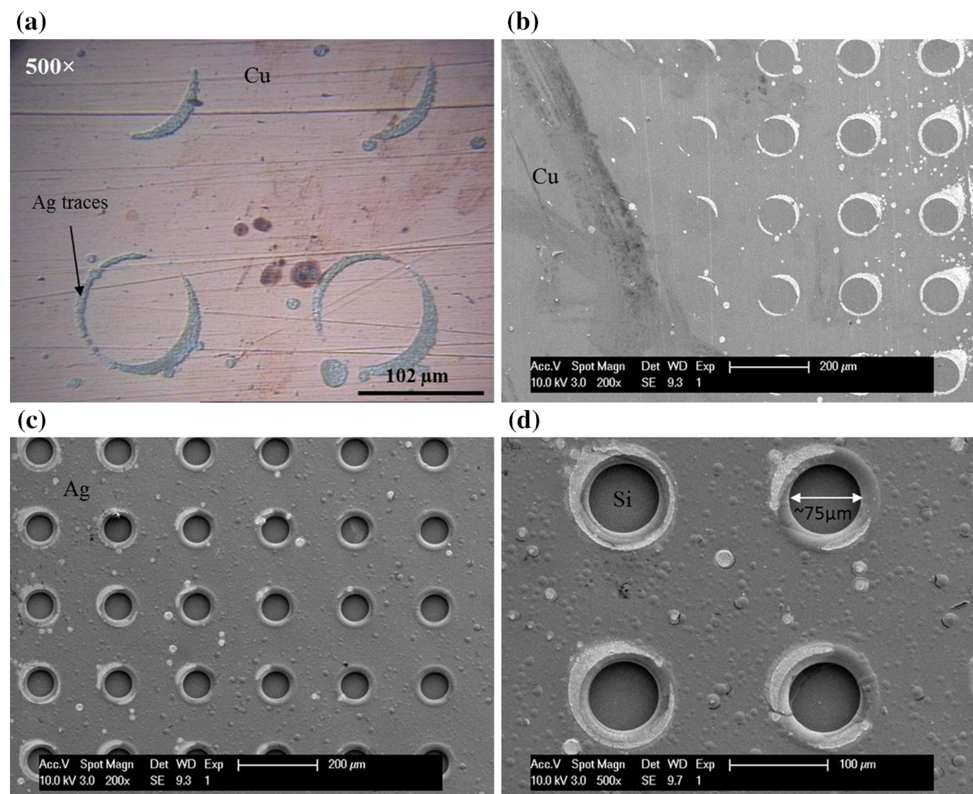

Fig. 9 OM and SE SEM images of the fracture surface of sample no. 3 after shear test: **a** OM image on Cu side, **b** SE SEM image on Cu side, **c** low magnification SE SEM image on Si side, and **d** higher magnification SE SEM image on Si side

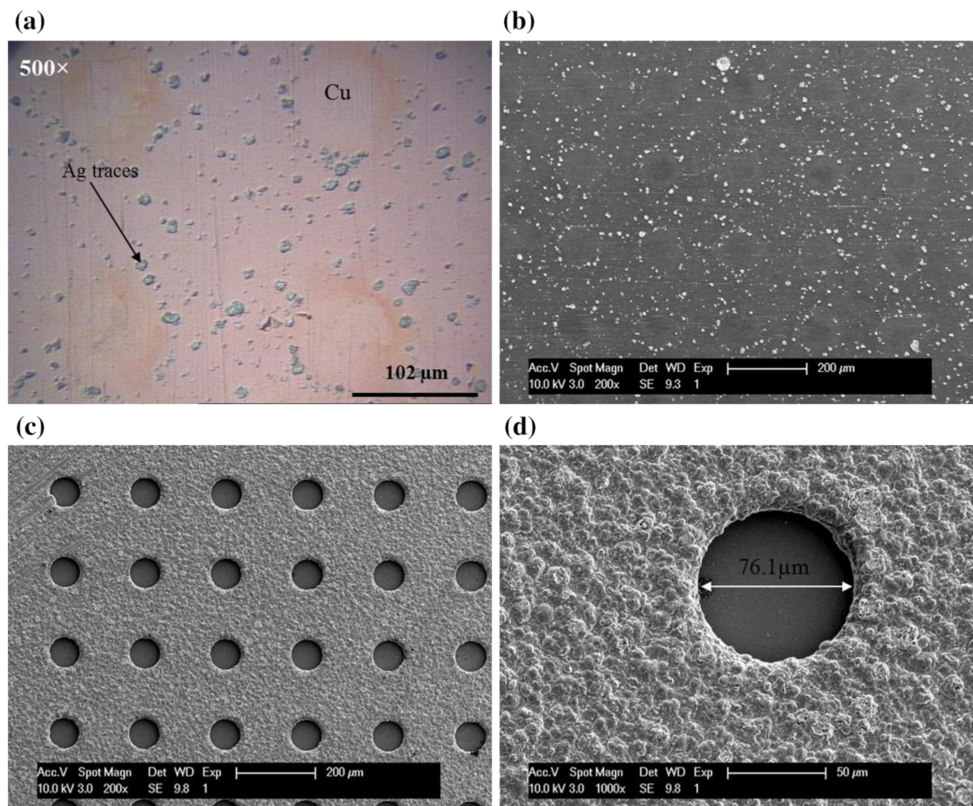

Fig. 10 OM and SE SEM images of the fracture surface of sample no. 6 after shear test: **a** OM image on Cu side, **b** SE SEM image on Cu side, **c** low magnification SE SEM image on Si side, and **d** higher magnification SE SEM image on Si side

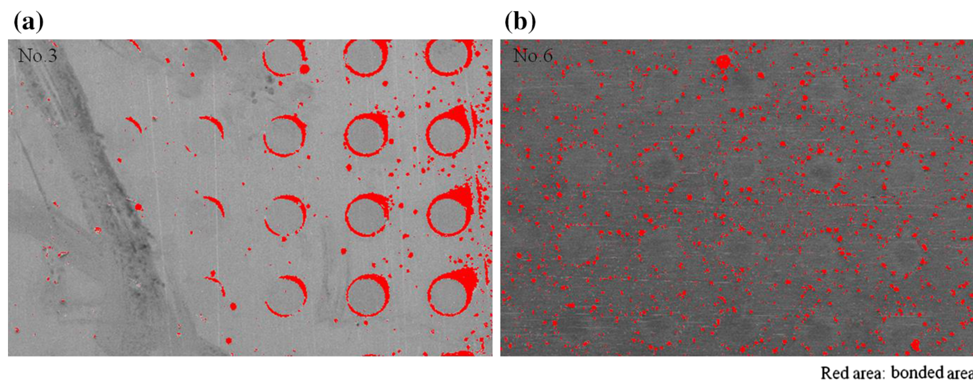

Fig. 11 The Ag traces on the Cu substrate: **a** sample no. 3, and **b** sample no. 6. The percentage of bonded area is 7.5 and 6.2 %, respectively

on the Cu chip after shear test. On these traces, the breakage occurs inside the Ag joint rather than on the Cu/Ag bonding interface.

The percentage of Ag traces on the entire area was estimated using image processing software, shown in Fig. 11. It is 7.5 % for sample no. 3 and 6.2 % for sample no. 6. Even though sample no. 6 has lower percentage of bonding area than sample no. 3, no. 6 sample achieved higher breaking force. This is probably because sample no. 6 has more uniform bonding distribution. Since the actual bonding area percentage is low, there is still room to improve to increase the bonding area percentage and thus increase the breaking force. The percentage of bonding area indicated in Fig. 11 is quite different from what could be expected by observing the very sharp bonding interface on the cross section images exhibited in Fig. 7. It seems that sharp bonding interfaces do not guarantee strong bonding for two reasons: (a) Small cracks and voids at the interface can be filled up by smearing effect during the polishing process, and (b) according to the quantum bonding theory, the interfacial gap needs to be reduced down to 1 nm in order for solid state

bonding to take place [5], which is what our SEM system cannot resolve.

5 Summary

In this research, Ag layers with array of cavities were produced on Si chips with Cr and Au layers and then bonded to Cu substrates. The bonding process is a solid state bonding performed at 300 °C with 1000 psi (6.9 MPa) static pressure for 5 min in 0.1 torr vacuum. The bonding time is limited by our bonding apparatus. In theory, it should take seconds to achieve bonding. With the help of the cavities, the bonding pressure was reduced to 600 psi (4.1 MPa). Neither molten phase nor flux was involved. The function of the cavities on the Ag layers is to provide space for the bonding medium, Ag, to deform and to flow into during the bonding process. The flow distance is thus reduced from half of chip size to half of the pitch of the cavity array, i.e., from global to local. Accordingly, the chip size can be increased without increasing the bonding pressure. The shear test results show that Ag joints are strongly bonded and pass the military standard MIL-STD-883H, except one sample. Fracture analyses reveal that only 6.2–7.5 % of the Ag layer surface was actually bonded to the Cu substrates. Thus, there is room to improve to increase the breaking force. The bonding structure can withstand high operating temperatures that are only constrained by the 780 °C eutectic temperature of the Cu-Ag binary system. Compared to current die-attachment methods, this novel bonding process can be applied to packaging devices with low thermal resistance for high temperature operations.

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