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Effects of post deposition annealing, interface states and series resistance on electrical characteristics of HfO_2 MOS capacitors

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Abstract The purposes of this paper are to investigate the post deposition annealing (PDA) effect on structural and electrical characterizations of HfO_2 MOS capacitor and the frequency dependency of series resistance and interface states in this device. PDA processes on the HfO_2 films deposited using RF magnetron sputtering system were performed in N_2 ambient at 350, 550, 650, and 750 °C. The phase identifications and crystallization degrees of the HfO_2 films were determined by using X-ray diffractometry. The grain size of the films was varied from 4.5 to 15.23 with increasing in PDA temperature. The HfO_2 MOS capacitors were fabricated using the as-deposited and annealed films for electrical characterization. C–V and G/ω–V measurements were performed at 1 MHz frequency. The C–V characteristics of the MOS capacitor fabricated with film annealed at 550 °C show a better behaviour in terms of the high dielectric constant and low effective oxide charge compared to others. For this device, C–V and G/ω–V measurements were performed in different frequencies ranging from 10 kHz to 1 MHz at room temperature. Obtained results show that series resistance and interface states strongly influence the C–V and G/ω–V behaviour of the MOS capacitor.

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1 Introduction

Metal oxide–semiconductor (MOS) capacitors and relevant devices have been intensively investigated due to their common applications [1, 2]. The usability of a MOS capacitor in technological applications depends on especially its electrical characteristics, related to gate insulator properties and its compatibility with semiconductor material. As the size of gate insulator thickness have showed a continuously scale down, the traditional SiO_2 have reached to its physical and electrical limits. It has been reported that the SiO_2 film thickness less than 1.2 nm lead to serious leakage current due to the direct tunneling of electrons [3–6]. During recent years, the studies on the investigation of the electrical properties of the high-k dielectric materials as gate insulator such as ZrO_2 [7], Al_2O_3 [8], HfO_2 [9, 10] have been extensively increased with the aim of designing the high performance. Among the high-k dielectrics, HfO_2 has been reported as the most promising candidate due to their attractive properties such as high dielectric constant [11], large band gap [12], and good thermodynamic stability [4].

The most important parameters affecting the gate dielectric properties are growth method of the films and post-deposition annealing (PDA) treatments. Several methods such as atomic layer deposition (ALD), molecular beam epitaxy (MBE), and chemical vapour deposition (CVD) have been used to deposit the thin films. RF sputtering is an important technique in terms of providing thin film deposition at low temperature. PDA is generally applied after deposition to reduce the number of defects and impurities present in the film. But, it is difficult to form a perfect HfO_2/Si interface compared to the SiO_2/Si because Hf-silicate/Hf–O–Si formation and SiO_2 layer generally occurs during the initial stage of the dielectric deposition or after PDA process

[6, 13–16]. Moreover, the phase transition of the HfO_2 film, from amorphous to crystalline, occurs with the increasing in annealing temperature and so, the electrical properties of MOS capacitor such as leakage current, capacitance values, flat band voltage are influenced [9, 13]. For these reasons, the determination of the optimum PDA conditions is quite important to fabricate high quality devices.

The effect of nitrogen (N_2) ambient in PDA process on structural characteristic of HfO_2 film has been investigated by several researches [11, 13, 16]. The results of these studies show that the crystallization temperature of HfO_2 gate dielectric is improved by the nitrogen ambient during PDA process. Moreover, A few studies on the investigation of capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristic curves of MOS capacitor with HfO_2 annealed at different temperature were reported and, the obtained results show that the PDA temperature strongly influences the behaviours of C–V and G/ω–V curves [4, 9, 13, 17, 18]. However, C–V curve behaviours of devices annealed at similar temperature range are not consistent with each other. Besides, there is very little information about the electrical parameters of MOS capacitor with HfO_2 film annealed at different temperature such as diffusion potential (V_D), carrier concentration (N_D), and barrier height (Φ_B) in the literature.

In this study, RF magnetron sputtering system was used to grow the HfO_2 films. The structural properties of the HfO_2 films annealed at different temperatures between 350 and 750 °C and nitrogen ambient were examined by using X-ray diffraction (XRD). C–V and G/ω–V measurements were performed with the aim of evaluating the PDA dependences of electrical characteristics of HfO_2 MOS capacitors and frequency dependency of series resistance and interface states in this capacitor. Interface states density (D_{it}), effective oxide charge ($Q_{f,eff}$), series resistance (R_s), image force barrier lowering ($\Delta\Phi_B$), V_D N_D Φ_B values were calculated by using obtained experimental results.

2 Experiments

The hafnium dioxide films were deposited on p-type (100) Si substrate using a 4-inch HfO_2 target with purity of 99.99 % by RF-Sputtering technique. The 4 inch Si substrates were cleaned using standard RCA cleaning process. Cleaned substrates loaded into the sputtering chamber for deposition of HfO_2 layers. Before commencing sputtering, the base pressure of the chamber was below 5.0×10^{-4} Pa and the sputtering gas pressure was 1.0 Pa. The pre-sputtering was performed for 30 min at 350 W to remove the possible contamination of target surface. The HfO_2 deposition were performed in the room temperature using argon with the flow rate of 16 sccm and the process parameters, operating pressure, distance between the target and Si substrate, sputtering time, were 1.0 Pa, 10 cm and 11 min, respectively. Then, the deposited films were annealed in a horizontal tube furnace at 350, 550, 650, and 750 °C for 30 min under N_2 ambient (flowing rate 1000 sccm). The thickness of the as deposited film was measured to be 90 nm by ellipsometer. The ohmic contacts were fabricated by sputtering using Al target with purity of 99.99 %. The front surface electrodes of the MOS capacitors were formed using a shadow mask including circular dots with 1.5 mm diameter.

3 Results and discussion

3.1 X-ray diffraction

The crystal structures of as-deposited and annealed films at different temperatures were investigated by XRD method. The XRD patterns between 20° and 65° for as-deposited and annealed HfO_2 films were given in Fig. 1. It is seen that as-deposited films are almost amorphous phase. However, the film starts to crystalize after 305 °C, and the peak intensities, i.e., crystalline structure, increase with increasing in temperature.

The peak positions, indexed using the International Center for Diffractometry Data (ICDD), are in good agreement with the peaks of HfO_2 monoclinic phase (card no: 34-0104). Therefore, it can be clearly seen from the XRD spectra that HfO_2 films with ($\bar{1}11$) preferred orientation are monoclinic phase and polycrystalline structure.

The grain size of as-deposited and annealed films provide information about crystallization degree and is calculated for the strongest peak ($\bar{1}11$) using a Scherrer's equation [19, 20]:

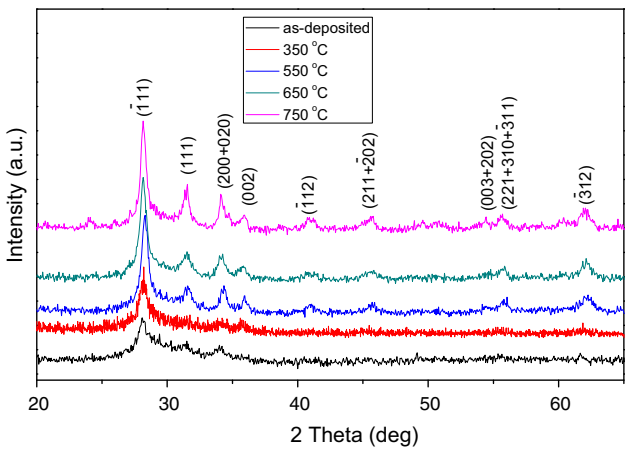

Fig. 1 XRD analyses of HfO_2 films on p-Si wafer, as-deposited and annealed at 350, 550, 650, 750 °C

$$P = \frac{0.9\lambda}{\beta \cos(\theta)} \quad (1)$$

where β is the FWHM of peak, λ is wavelength, and θ is Bragg angle for peak position. The average grain sizes for as-deposited, 350, 550, 650, 750 °C were obtained to be 4.5, 9.73, 12.04, 13.45, 15.23 nm, respectively. These values show that crystallization degree increases with increasing PDA temperature.

3.2 PDA effects on electrical characteristics of MOS capacitors

C–V curves (series resistance correction was taken into account in the C–V measurements as explaining following section) obtained from annealed devices at different temperatures for high frequency (1 MHz) are presented in Fig. 2. The capacitance values in the accumulation regions have not significantly changed between the as-deposited and 550 °C. After 550 °C, reduction in the capacitance values is observed with increasing annealing temperature. But, the reduction in the capacitance of capacitor annealed at 650 °C is quite lower than that of device annealed at 750 °C. The sharp reduction may depend on the increment of the thickness of interfacial layer between the Si and HfO_2. High annealing temperature may leads to the breaking of metastable Hf–Si bonds and the $HfSi_xO_y$ may be observed as dominant components at the interfacial layer [13]. Besides, present of interfacial layer leads to the reduction of effective oxide capacitance of MOS capacitor [9, 17]. In addition to interfacial layer, another reason of the decreasing capacitance may be leakage current. The increment in the crystallization degree leads to larger leakage path and thus leakage current increases and capacitance drops [13, 15, 21]. In addition, the flat band voltage is located to negative values due to positive trapped charges, and approaches to ideal value (−0.50 V) with increasing annealing temperatures up to 550 °C. The amounts of the total charge densities in device structure are main reason of the flat band voltage variations. The total of the oxide charges in the oxide layer is defined as the effective oxide charge ($Q_{f,eff}$). The $Q_{f,eff}$ in the HfO_2 films can be calculated by using following equation [3]:

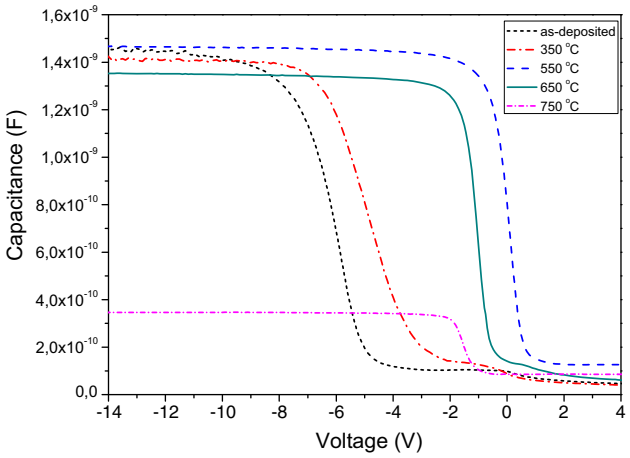

Fig. 2 C–V Curves carried out for high frequency (1 MHz) for MOS capacitors with as-deposited and annealed HfO_2 films

$$V_{FB} = \phi_{MS} \pm \frac{Q_{f,eff}}{C_{ox}} \quad (2)$$

where V_{FB} is flat band voltage, C_{ox} is the oxide capacitance in accumulation region, and $\varnothing_{MS}$, is the work function difference between the Al and Si. Calculated $Q_{f,eff}$ values are shown in Table 1. The negative flat band voltages due to the positive effective charge in HfO_2 layers were observed obviously at the as-deposited, 350, 650, and 750 °C samples. If the positive oxide charge was trapped or a reduction occurred in negative trapped charge due to recombination, depletion would begin earlier with respect to ideal MOS curve. In other word, the less positive gate bias would need to be applied for the transition from the depletion to inversion and MOS curve shifts towards to left side. The flat band voltage shifted towards to right side at the temperature range between the 0 and 550 °C. The reason of these shifts might be the reduction of the effective oxide charge density as given in Table 1, and it can be concluded that the annealing process up to 550 °C enhances the stoichiometry of the insulator and treats the defects. In addition, the flat band voltages for the devices annealed at 650 and 750 °C shift to left side again as seen in Fig. 2. The possible explanation of this behaviour is the formation of new defects with increasing annealing temperature and/or formation of parasitic thin silicate interfacial layer. The Q_{eff} value of MOS capacitor annealed at 550 °C that shows a good behaviour is lower than the value (4.32×10^{12}) reported by Khairniar et al. [9].

One of the most important parameters affecting on C–V characteristics is density of the interface states which can be found using following equation [9, 22]:

$$D_{it} = \frac{2\omega C_{ox}^2 G_{c,\max}}{q.A\left(G_{c,max}^2 + \omega^2\left(C_{ox} - C_{c,m}G_{c,max}\right)^2\right)} \quad (3)$$

where q is the electrical charge, A is the front contact area of the MOS capacitor, $C_{c,m}$ is the capacitance that correspond to $G_{c,max}$, $G_{c,max}$ is the maximum corrected conductance, ω is the angular frequency. Obtained results for the density of interface states are given in Table 1. The interface trapped charge occurs due to the structural defects and oxidation-induced defects. If net positive charge exited at the oxide/silicon interface then less negative gate bias would be needed resulting in a steeper slope for p-type Si.

Table 1 The some electrical parameters of HfO_2 MOS capacitor

T (°C)	$Q_{f,\ eff} \times 10^{12}$ (cm^{-2})	$D_{it} \times 10^{10}$ (eV^{-1} cm^{-2})	V_D (eV)	$N_A \times 10^{14}$ cm^{-3}	E_F (eV)	$\Delta\Phi_B$ (eV)	Φ_B (eV)
As-deposited	11.7	10.9	−1.294	4.28	0.255	0.013	1.052
350	10.1	10.2	−1.313	3.30	0.261	0.012	1.064
550	1.55	13.6	0.244	6.20	0.245	0.009	0.480
650	3.07	11.6	−0.404	6.28	0.245	0.010	0.170
750	3.69	2.42	−1.689	3.05	0.263	0.012	1.438

If net negative charge is trapped then more positive gate bias would be needed resulting in a stretch out of the C–V curve [23]. The C–V characteristics for annealed at 550, 650, and 750 °C devices show that the higher positive interface traps may exist in these structures compared to as-deposited and annealed at 350 °C devices due to the wide of the curves.

Linear regions of $1/C^2$–V characteristics (Fig. 3a) of HfO_2 MOS capacitors for 1 MHz were obtained with the aim of the calculating some electrical parameters of as-deposited and annealed devices such as diffusion potential/

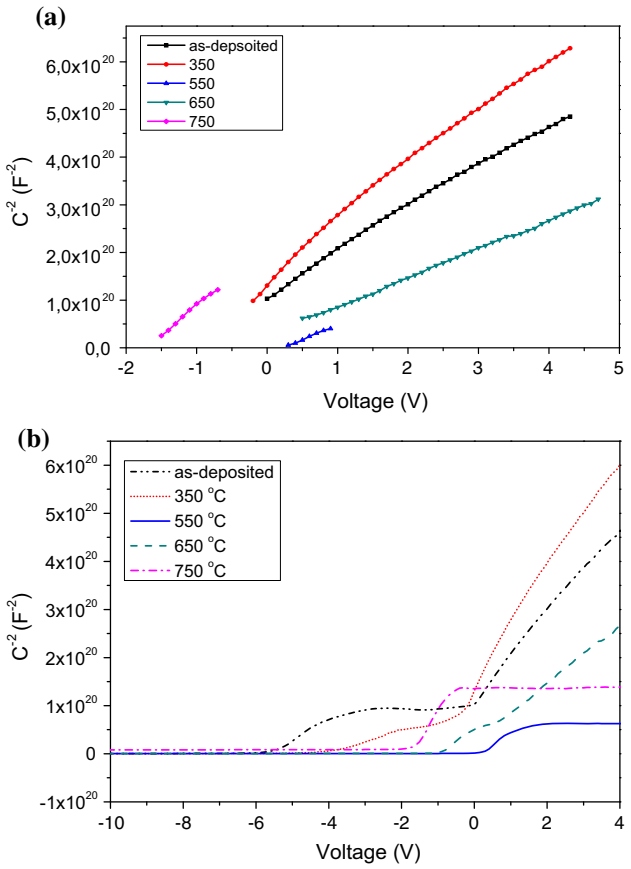

Fig. 3 **a** C^{-2}–V plots of the linear regions of the MOS capacitors with as-deposited and annealed HfO_2 films at 1 MHz , **b** C^{-2}–V plots of the MOS capacitors with as-deposited and annealed HfO_2 films at 1 MHz

built-in voltage (V_D), barrier height (Φ_B). The linear regions of obtained curves fitted using the linear lines and for the high frequency measurements (≥500 kHz), depletion layer capacitance can be given as [10, 24–27]

$$C_c^{-2} = \frac{2(V_o + V)}{\varepsilon_s \varepsilon_o q A^2 N_A} \tag{4}$$

$$\frac{d\left(C_c^{-2}\right)}{dV} = \frac{2}{\varepsilon_s \varepsilon_o q A^2 N_A} \tag{5}$$

where A is the area of the MOS capacitor (1.76625×10^{-4} cm^{-2}), ε_s is the semiconductor dielectric constant (11.9 for Si), q is the electronic charge, V is applied voltage, N_A is carrier (acceptor) concentration. V_0 is the intersection of lines with voltage axis and given as

$$V_o = V_D - \frac{k_B T}{q} \tag{6}$$

where V_D the diffusion potential, T is the absolute temperature and k_B is the Boltzmann constant. The value of barrier height (Φ_B) can be calculated by the following expression [28]:

$$\Phi_{B(C-V)} = V_D + E_F - \Delta\Phi_B \tag{7}$$

where E_F is the energy difference between the bulk Fermi level and conduction band edge, and is given by [28]

$$E_F = \frac{k_B T}{q} \ln\left(\frac{N_c}{N_A}\right) \tag{8}$$

N_c is the effective density of states in Si conduction band and given as [27, 28]:

$$N_C = 2\left[\frac{2\pi m_e^* m_o k_B T}{h^2}\right]^{\frac{3}{2}} \tag{9}$$

$me^* = 0.55\, m_0$ is the effective mass of electron and m_o is the rest mass of the electron. $\Delta\Phi_B$ is the image force barrier lowering and can be calculated from [27, 28]

$$\Delta\Phi_B = \left[\frac{qE_m}{4\pi\varepsilon_s\varepsilon_o}\right]^{\frac{1}{2}} \tag{10}$$

where E_m is the maximum electric field and calculated by [29]

$$E_m = \left[\frac{2qN_A V_o}{\varepsilon_s \varepsilon_o}\right]^{\frac{1}{2}} \quad (11)$$

Obtained V_D, N_A, E_F, $\Delta\Phi_B$, and Φ_B values are given in Table 1. The linear behaviour of C^{-2}–V plots can be explained with possible two events. The interface traps cannot follow the AC signal at high frequency (explained in detail in following section) and as depending on this, these states cannot contribute to the capacitance of MOS. The other possible reason is uniform or constant acceptor concentration (N_A) throughout the depletion region [25, 27, 30]. It is expected that MOS capacitor C–V curve should show a flat slope at the accumulation and inversion regions (for equilibrium condition). The fluctuations in these regions can be fairly observed from the C^{-2}–V curves as seen in Fig. 3b). Our results show that only MOS capacitors annealed at 550 and 750 °C show the flat slope at the inversion region and accumulation while the C–V curves of all annealed devices have flat slope at the accumulation region. The increment of the C^{-2} values in the inversion region shows the reduction in the capacitance values. The possible reason of this reduction is deep depletion. In this case, the collection of inversion charge occurs in longer time as depending on the recombination velocity of minority carriers when the voltage rapidly changes at high frequency measurements. In the result of this event, the capacitance values below the minimum capacitance (C_{min}) are observed in the C–V curve. Therefore, increment in C^{-2} values from depletion to inversion may occur in a wide voltage range [31]. The relatively higher barrier height (Φ_B) values are attributed to high V_D values. The lowest barrier height value was observed in the MOS capacitor with HfO_2 gate dielectric annealed at 650 °C. The high barrier height provides the low charge injection, and thus the tunnelling probability of the charges decreases with increasing barrier height [24, 32].

3.3 Frequency dependency of series resistance and interface states in HfO_2 MOS capacitor

The effect of frequency on electrical characteristics of MOS devices can be investigated by the analyses of capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements. C–V and G/ω–V profiles measured at different frequencies and room temperature are only presented for annealed device at 550 °C in Figs. 4 and 5 due to its high dielectric constant and low flat band voltage (−0.510 V) compared to others. It can be clearly seen from Fig. 4 that the capacitance values decrease with increasing voltage frequency. The possible reason of this behaviour is time dependent surface states, especially interface states. The measured capacitance can be explained by equivalent circuit as seen in Fig. 6 [33, 34]. In the circuit, C_{ox}, C_{sc}, C_{it}, and R_s are the oxide capacitance, space charge capacitance,

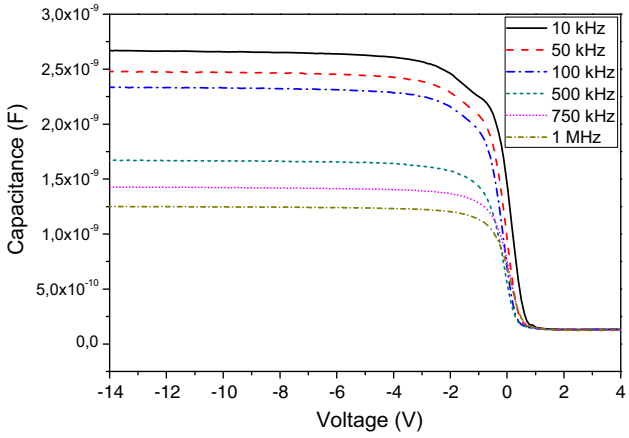

Fig. 4 C–V curve for device at annealed at 550 °C for different frequencies

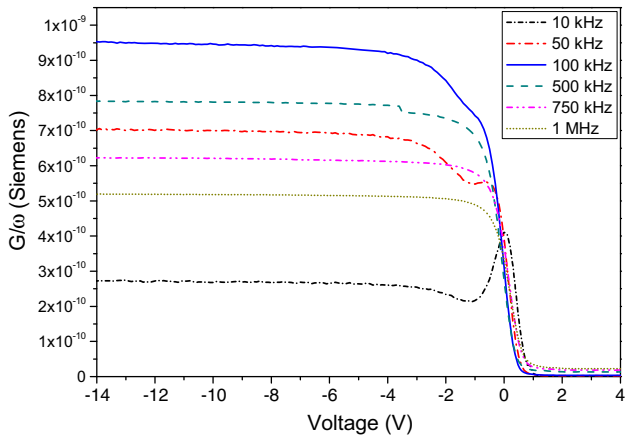

Fig. 5 G/ω–V curve for device at annealed at 550 °C for different frequencies

interface states capacitance and series resistance, respectively. For the low frequencies (<100 kHz), the effective capacitance C_{LF} can be expressed as [33]

$$\frac{1}{C_{LF}} = \frac{1}{C_{OX}} + \frac{1}{C_{SC} + (C_{it}/(1+\omega^2\tau^2))} \quad (12)$$

where ω (ω = 2π*f*) is angular frequency. The interface-trap lifetime (τ) is defined as $C_{it}R_s$ term that determines the variation of interface traps with frequency. The studies in the literature show that τ is on the order of 10^{-6}–10^{-7} s [35]. Therefore, ωτ is quite small for the low frequency, especially lower than 50 kHz. The $\omega^2\tau^2$ term is negligible in Eq. (12). In other words, interface trapped charges may easily follow the AC signal and leads to excess capacitance at low frequency measurements. Consequently, the oxide capacitance is in series with a parallel combination of space charge capacitance and interface states capacitance at low frequencies, and C_{it} can be calculated from following expression [33]:

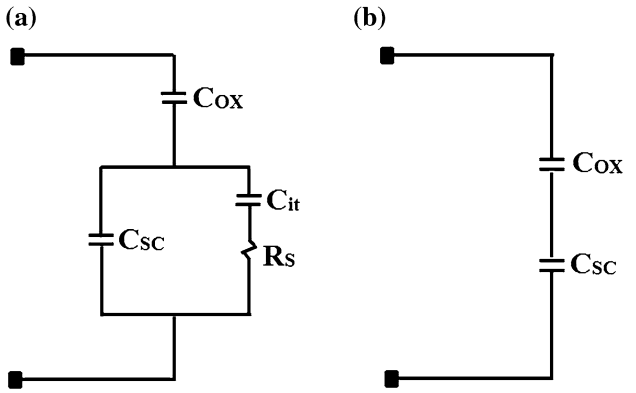

Fig. 6 Equivalent circuits including series resistance R_s and the capacitance induced interface traps C_{it}; **a** low frequency, **b** high frequency limit

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{OX}}\right)^{-1} - C_{SC} \tag{13}$$

The contribution of the interface states to total capacitance is negligible level at high frequencies level (f ≥ 500 kHz) because they cannot follow the AC signal [33]. Therefore, the effective capacitance is the series combination of oxide and space charge capacitances. In this case, the effective capacitance represented by C_{HF} is expressed by

$$\frac{1}{C_{HF}} = \frac{1}{C_{OX}} + \frac{1}{C_{SC}} \tag{14}$$

Although interface states influence the C–V characteristic of MOS capacitor, The C–V curves for all of the frequencies have three characteristic regions defined as accumulation, depletion, and inversion, verifying a typical MOS behaviour. Besides, it was not observed any kinks at the C–V curves above the voltage frequency of 10 kHz. But, the kink in the C–V curve is clearly seen in transition from the accumulation to depletion for 10 kHz. The reason of this behaviour may be some defects and poor interface properties between the HfO_2 and p-Si [36]. Moreover, the C–V curves shift towards to right side with increasing voltage frequency. The frequency dependent surface states such as interface states and series resistance may lead to this variation in the C–V curve [29, 33, 37].

When a small AC signal is applied to the metal–oxide–semiconductor (MOS) capacitor, the exchange of majority carriers between the interface states and majority carrier band of semiconductor inducing the conductance losses occurs. The conductance measurement is based on this event. The Fermi level moves up or down with respect to the interface trap states due to applied a small AC signal. The interface traps near the band edges can rapidly capture and release carriers under different gate bias. This case influences the charge and field distributions and alters the ideal MOS curve [33, 37]. Consequently, investigation of the conductance variation as depending on gate voltage is a quite important to evaluate the electrical characteristic of MOS capacitor. The G/ω–V measurements (Fig. 5) show that the obtained curves are not as expected due to the number of parameters such as series resistance, interface states density and frequency dependency of these states as stated above [38]. However, high frequency G/ω–V measurements (≥500 kHz) show a similar behaviour with the low frequency G/ω–V measurements. This result may show that R_s is more important parameter compared to interface states because the effect of these states on G/ω–V curve can be eliminated or decreased at high frequencies. The interface traps change depending on measurement frequency were investigated and the results were shown in Fig. 7. It can be obviously shown that the density of interface states decreases with increasing frequency as expected.

Series resistance (R_s) is an important error parameter in the C–V and G/ω–V measurements as explained above. Therefore, series resistance effect should be taken into account in the measured conductance and capacitance curves. We used the Nicollian and Goetzberger method to eliminate the series resistance effect at the C–V and G/ω–V curves [39]. The strong accumulation admittance (Y_{ma}) of the capacitor is calculated from the Eq. 15 including the measured capacitance in strong accumulation, C_m, and parallel conductance G_m (measured conductance in strong accumulation) [39].

$$Y_m = G_m + j\omega C_m \tag{15}$$

Series resistance is the real part of the impedance ($Z_m = 1/Y_m$) and given by [39]

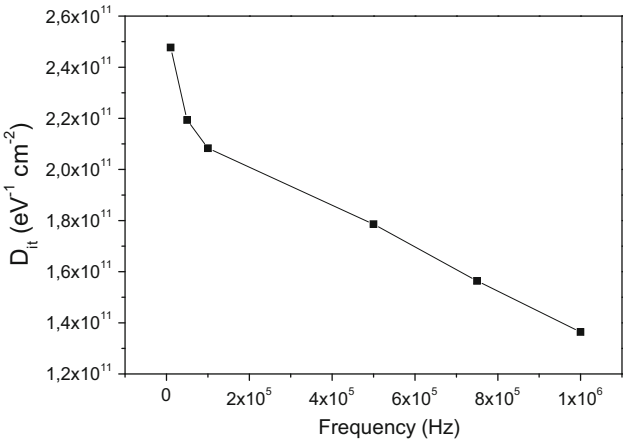

Fig. 7 The densities of interface states at different frequencies for MOS capacitor with HfO_2 annealed at 550 °C

$$R_s = \frac{G_m}{(G_m)^2+(\omega C_m)^2} \tag{16}$$

where ω is the angular frequency. The series resistance values were calculated from Eq. (16), and the curves of voltage-dependent variation for different frequencies from 10 kHz to 1 MHz were shown in Fig. 8. It can be clearly seen that the location of the peak of the R_s-voltage curves varies with applied voltage frequency. This behaviour of R_s peak can be explained with the voltage dependent charges such as fixed oxide charge, interface charge, oxide trapped charge, and mobile oxide charge [33, 34]. Moreover, R_s values take the values close to each other at high frequencies ($f \geq 500$ kHz) due to the trapped charges, which gain enough energy to escape from the traps located to the Si band between metal and semiconductor interface [34]. The calculated R_s values are used to correct the C–V and G/ω–V curves. The corrected C–V and G/ω–V curves were obtained by using the following equations:

$$C_c = \frac{\left[(G_m)^2+(\omega C_m)^2\right]C_m}{a^2+(\omega C_m)^2} \tag{17}$$

$$G_c = \frac{\left[(G_m)^2+(\omega C_m)^2\right]a}{a^2+(\omega C_m)^2} \tag{18}$$

where $a = (G_m) - \left[(G_m)^2+(\omega C_m)^2\right]R_s$. The corrected C–V and G/ω–V curves of MOS capacitor measured in the range from −14 to 4 V are shown in Figs. 9 and 10, respectively. The comparison between the uncorrected and corrected C–V curves shows that capacitance values have higher values after series resistance correction. The behaviour of C–V curves after correction is similar with uncorrected C–V curves. But, corrected G/ω–V curves are quite different from the uncorrected G/ω–V results. Corrected G/ω values decreases with increasing frequency while the uncorrected G/ω values increases with increasing frequency up to 100 kHz and after this value, these values decreases with increasing frequency. Besides, conductance peak position shifted towards to left side from the 10 to 500 kHz. After this frequency value, the peak position varied towards to right side with increasing value and reached to ideal case at 1 MHz.

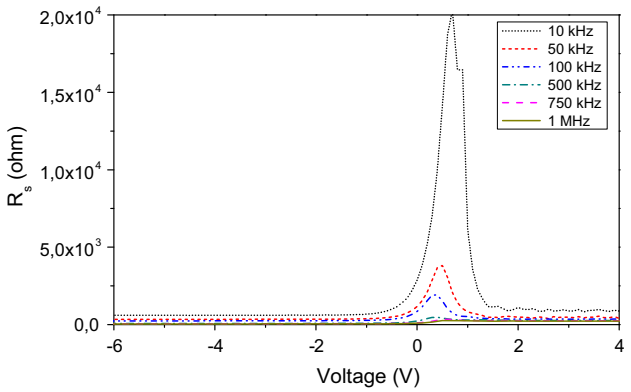

Fig. 8 The series resistance curves of the HfO_2 MOS capacitor at different frequencies

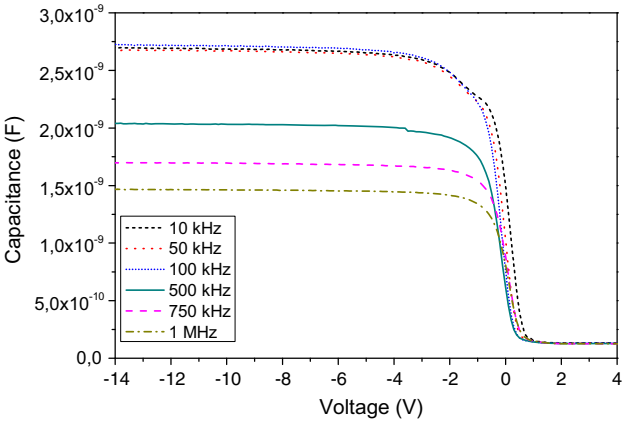

Fig. 9 Corrected C–V curves for HfO_2 MOS capacitor for different frequencies

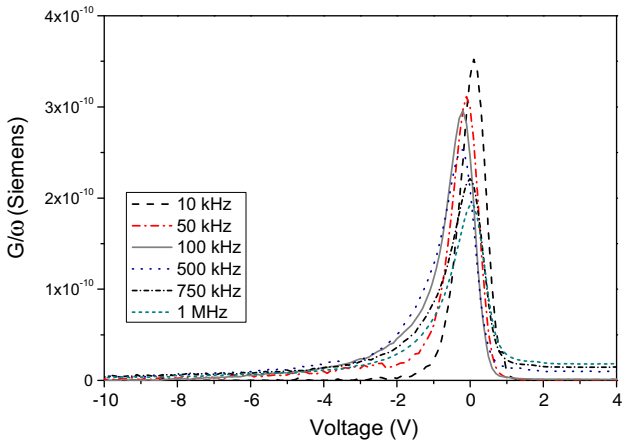

Fig. 10 Corrected G/ω–V curves for HfO_2 MOS capacitor for different frequencies

4 Conclusion

In the present study, the effects of PDA in nitrogen ambient on crystallization degree of HfO_2 films and C–V characteristics obtained from HfO_2 MOS capacitors were investigated. Moreover, the frequency dependencies of the series resistance and interface states were investigated using the C–V and G/ω–V curves of MOS capacitor with HfO_2 film annealed at 550 °C. The capacitance values for the MOS capacitors with HfO_2 films as-deposited and annealed at 350 and 550 °C slightly changed. However, the C–V

curves shifted towards to zero voltage up to 550 °C due to the treatment of defects or effective oxide charges with PDA process. After 550 °C, the capacitance values decrease with increasing PDA temperature due to the possible formation of interfacial layer and increasing leakage current. A continuous reduction in capacitance values in inversion regions except MOS capacitors with HfO_2 layer annealed at 550 and 750 °C was observed due to deep depletion. Series resistance and interface states influence the measured C–V and G/ω–V curves. Especially, series resistance effect is more dominant parameter than the effect of interface states at high frequency measurements. Therefore, necessary correction about series resistance effect should be performed in the C–V and G/ω–V curves. It can be concluded that the Both C–V and G/ω–V curves are close to the approximately ideal case at the 1 MHz.

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