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Growth of gold nanoparticles using aluminum template via low-temperature hydrothermal method for memory applications

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Abstract Gold nanoparticles (AuNPs) were grown on a Si(100) substrate using a sacrificial hydrothermal method on Al template prepared by direct current (DC) sputtering, followed by thermal annealing. The effect of annealing temperature on the Al template was investigated. The morphology and phases of the grown AuNPs were observed by field-emission scanning electron microscopy (FESEM) and X-ray diffraction (XRD), respectively. FESEM and XRD results revealed the uniform face-centered cubic structure of AuNPs with isolated 83 nm particle size and 1.48×10^{13} m^{-2} area density; these properties were considered optimum for AuNPs formed on the non-annealed sputtered Al template. The electrical properties of AuNPs embedded in polymethylsilsesquioxane (PMSSQ) as an organic dielectric layer were studied using a semiconductor characterization system. A metal–insulator-semiconductor device with embedded AuNPs was proven to exhibit memory effects. Optimum memory properties of AuNPs embedded in PMSSQ were obtained for AuNPs grown on the non-annealed sputtered Al template with the lowest threshold voltage of 2.4 V in I–V characteristics and 34 electrons stored per AuNP in C–V measurement.

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1 Introduction

Noble metallic nanoparticles (NPs), such as gold (Au), silver (Ag), and platinum (Pt), have received considerable research interest because of their excellent electronic, optical, and thermal properties [1–4]. Among various types of materials, gold nanoparticles (AuNPs) are the most promising because they contain good trap sites as electron acceptors when electrons from an electrode are injected. Moreover, AuNPs are characterized with a wide range work function ($\sim$5.0 eV) to provide a small barrier for programming/erasing mode and high confinement barrier for retention mode [3, 5].

In electronic applications, non-volatile memory devices, which are embedded with AuNPs as a charge-trapping source, are of great interest because these devices exhibit high current density, large on/off current ratio, and excellent storage properties [3, 5]. To obtain excellent electrical properties of memory devices, AuNP distribution is crucial. Therefore, efficient approaches of AuNP formation on substrates are necessary to achieve excellent NP distribution. For instance, self-assembled monolayers (SAMs), physical vapor deposition, and Langmuir–Blodgett method [6–12] have been developed to produce AuNPs on substrates.

SAMs have been used to modify substrate surfaces for good adhesion of AuNPs on a substrate. SAMs provide unique advantages of highly oriented self-organization and can incorporate a wide range of groups in alkyl chains and at chain terminals [6–9]. For example, Hurst et al. [7] obtained a monolayer of self-assembled particles by attaching a functionalized p-aminophenyl trimethoxysilane and 3-mercaptopropyl trimethoxysilane polymer on a substrate and then dipping it in AuNP solution. NPs attached to the substrate via covalent bonds to immobilize AuNPs. This

deposition technique produced uniform AuNP thin films. However, AuNP/SAM films are limited by thermal stability issues associated with organic SAMs [7]. Furthermore, Liu et al. [13] investigated the fabrication of self-assembled AuNPs attached to 3-aminopropyltrimethoxysilane-modified fused silica substrates by the spin coating method. This method produced high packing density of AuNPs on the Si substrate. However, the spin speed and rate should be controlled to avoid the formation of liquid droplets caused by the centrifugal effect [14].

Physical vapor deposition can be used to produce AuNPs by depositing a layer of gold thin films followed by post-deposition annealing to acquire agglomerated AuNPs via the Ostwald ripening method [11]. However, diffusion of metals to form an interface layer and stacking of structures may degrade the memory properties of devices. The Langmuir–Blodgett method has also been studied to deposit AuNPs on a substrate. Ultrathin films can be obtained by transferring a monolayer of amphiphilic molecules from the air water interface to a substrate through evaporation of the underlying water layer. Although this simple process can be performed to prepare ordered arrays of metallic NPs, the homogeneity of NP arrays is difficult to control [12].

In previous studies, AuNPs were directly formed on a substrate using a novel sacrificial template hydrothermal method [15, 16]. In those studies, seeded ZnO was used as a template [15, 16]. The effect of annealing temperature of the ZnO template on AuNP formation has also been studied, in which 300 and 350 °C are the optimum annealing temperatures for sputtered and thermally evaporated ZnO templates, respectively. In both studies, the ZnO template was dissolved in hydrothermal solution during AuNP formation. The amphoteric properties of ZnO allow it to dissolve in acids to form salts that contain hydrated zinc(II) cations [15]. This method is simple, cost-effective, and produces uniform distribution of AuNPs. The effects of AuNP distribution embedded in PMSSQ layers in memory applications have also shown promising results compared with those described in other reported studies. However, in both studies, we only used ZnO as a template. Moreover, the underlying mechanism that caused template dissolution has not been explained.

Therefore, in this work, we used Al as a template to investigate whether it can affect the formation of AuNPs using the sacrificial growth hydrothermal method. In this work, a DC-sputtered Al template was used. The effect of annealing temperature of the template on AuNP formation was studied. The mechanisms of AuNP formation and Al template dissolution are discussed in detail in this paper. For the analysis of memory properties, a metal-insulator-semiconductor (MIS) memory device in the form of Au/insulator/AuNP/insulator/n-type Si/Al structure was fabricated. Furthermore,

the possible transport mechanisms via insulator memory devices were proposed.

2 Experimental details

In this study, 1 cm × 1 cm n-type <100> silicon wafers were used as substrates. The substrates were cleaned in accordance with the standard Radio Corporation of America (RCA) cleaning procedures to remove organic and inorganic contaminants. The RCA cleaning procedures involve the following steps. In the first step, organic cleaning was performed with 1:1:5 volume ratio of 37 % hydrogen peroxide: 28 % ammonium hydroxide: DI water. Si substrates were immersed in the solution at 80 °C for 10 min, and rinsed with DI water. In the second step, oxides were removed from the Si substrates by soaking in 1:50 of hydrofluoric acid and DI water in a polypropylene beaker, followed by rinsing with DI water. Si substrates were subjected to ionic cleaning in a 1:1:6 volume ratio of 49 % hydrochloric acid: 37 % hydrogen peroxide: DI water at 80 °C for 10 min and then rinsed with DI water. The substrates were soaked in DI water for 5 min and dried using N_2 gas.

The first layer of 250 nm-thick polymethylsilsesquioxane (PMSSQ 1) was spin-coated at 2000 rpm for 60 s. The substrates were cured at 160 °C for 1 h to crosslink PMSSQ. A 200 nm Al thin film was deposited on the substrates using the DC sputtering method. The substrates were annealed at 200, 300, and 400 °C with a ramp rate and soaking time of 10 °C/min and 1 h, respectively. The substrates were then subjected to hydrothermal reaction in a pre-heated oven at 80 °C for 4 h. The hydrothermal bath contained 0.1 M aluminum nitrate tetrahydrate ($Al(NO_3)_3 \cdot 4H_2O$), 0.1 M hexamethylenetetramine ($C_6H_{12}N_4$), 0.01 M gold (III) chloride trihydrate ($AuCl_4 \cdot 3H_2O$), and 10 mL of acetic acid. After hydrothermal reaction, the samples were removed and rinsed with deionized water. The samples were dried in an oven at 160 °C for 30 s to ensure good adhesion of AuNPs.

The samples were then characterized using a field-emission scanning electron microscope (FESEM) (LEO Gemini) equipped with an energy dispersive X-ray spectrometer (EDX) (ZEISS SUPRA^{TM} 35VP). Phases were analyzed using an X-ray diffractometer (XRD) (Bruker D8). For memory property analysis, a 250 nm second layer of polymethylsilsesquioxane (PMSSQ 2) was spin-coated on the sample and cured at 160 °C for 1 h. Au top and Al bottom contacts were deposited using thermal evaporation with the aid of a shadow mask. The structure of the MIS layer is illustrated in Fig. 1. The electrical characteristics, namely, current–voltage (I–V) and capacitance–voltage (C–V), of the device were measured using a semiconductor characterization system (Keithley Model 4200-SCS).
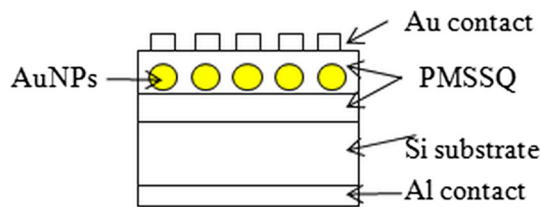
Fig. 1 Structure of AuNPs embedded in the MIS layer

3 Result and discussion

Figure 2 shows the surface morphology of as-sputtered Al and Al template annealed at different temperatures observed using FESEM. The FESEM image in Fig. 2a shows non-uniform surface morphology in the non-annealed sample. Large grains were observed on the template surface because atoms did not have sufficient time to rearrange themselves. For the sample annealed at 200 °C, the atoms rearranged themselves to form smaller grains and a more stable structure. For the sample annealed at 300 °C, the sample was dense and contained large and small grains. For the sample annealed at 400 °C, the small grains became finer. Moreover, the large grains were larger compared with those in the sample annealed at 300 °C. Small grains formed as products of recrystallization, whereas large grains formed by diffusion of small grains during annealing.

The average grain size of each sample was measured from FESEM images by using ImageJ software. Two distinct sizes of Al grains were obtained. The grain size larger than 100 nm was classified as large grains and the grain size less than 100 nm was classified as small grains. The size and ratio of large to small Al grains are tabulated in Table 1. The large grain sizes of the Al template of non-annealed sample and samples annealed at 200, 300, and 400 °C were 112 ± 8, 114 ± 12, 149 ± 12, and 157 ± 23 nm, respectively. The small grain sizes of the Al template of non-annealed sample and samples annealed at 200, 300, and 400 °C were 91 ± 9, 59 ± 6, 41 ± 8, and 27 ± 7 nm, respectively. Besides that, the ratio of large and small grain sizes for Al template of the non-annealed sample and the samples annealed at 200, 300, and 400 °C were 43:131, 61:145, 70:100 and 51:65, respectively. With increasing annealing temperature, the small Al grains became smaller because of the grain disorientation increased the mobility of the boundary and increased the amount of sub-grains. Disorientiation occurred as atoms vibrated at their lattice positions and exchanged energy with neighboring atoms. Therefore, atoms gained sufficient energy and diffused to achieve the lowest strain energy, resulting in small grains. This finding was in agreement with the findings
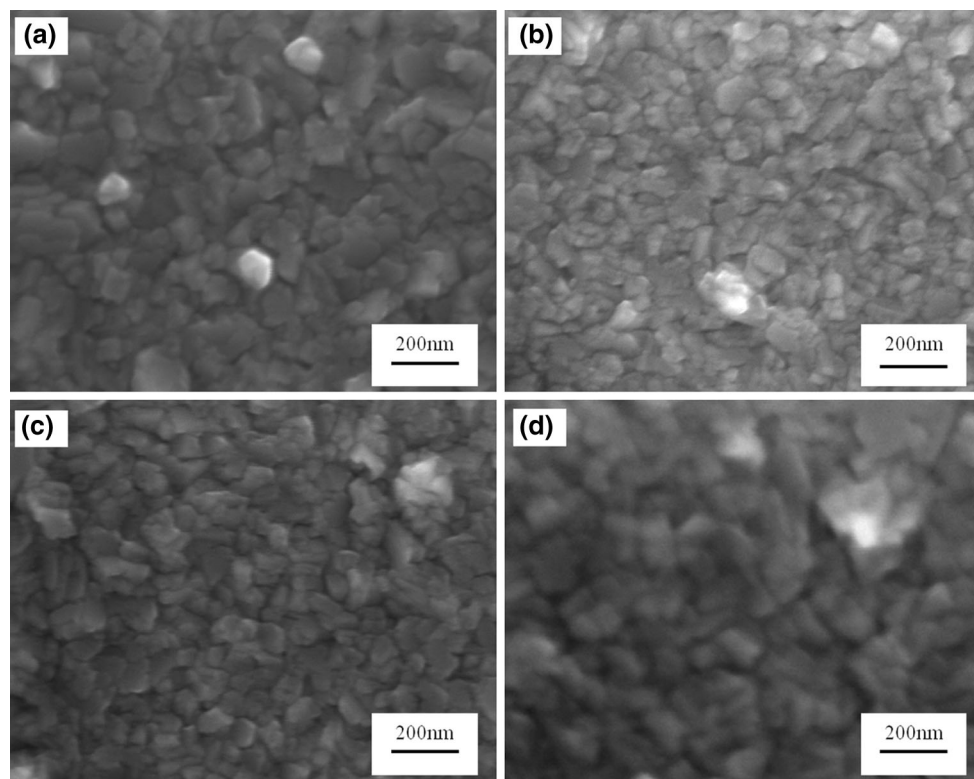

Fig. 2 FESEM images of the sputtered Al template with varying annealing temperatures: **a** non-annealed template, **b** template annealed at 200 °C, **c** template annealed at 300 °C, and **d** template annealed at 400 °C

Table 1 Grain size and ratio of large and small grain size of the Al template with varying annealing temperatures

Samples	Small grains (nm)	Large grains (nm)	Ratio of large and small grain size
Non-annealed	91 ± 9	112 ± 8	43:131
200 °C	59 ± 6	114 ± 12	61:145
300 °C	41 ± 8	149 ± 12	70:100
400 °C	27 ± 7	157 ± 23	51:65

of Mittemeijer [17]. However, some of the large Al grains likely grew because of grain growth during increasing annealing temperature. Thermal annealing induces coalescence of small grains by grain boundary diffusion, which causes grain growth. A similar finding was observed by Stinzianni et al. [18], who reported that grain growth occurs when the temperature increases beyond the recrystallization range; this growth causes small grains to form larger grains. These Al grains are then used as seeds to produce AuNPs during sacrificial hydrothermal reaction.

The crystalline structure and orientation of the Al template were investigated using XRD, and the results are shown in Fig. 3. Three strong diffraction peaks were observed at 38.45°, 44.71°, and 65.09°, which were ascribed to metallic aluminum [JCPDS No. 89-4037], and corresponded to the (111), (200), and (220) planes of the standard Al face-centered cubic (FCC) structure, respectively. In Fig. 3, the intensities of Si peaks are slightly changed among the samples due to PMSSQ layer contains Si was spin coated on the Si substrate before the Al template layer was sputtered. For the samples prepared with 200, 300 and 400 °C, the intensities of Si became higher compared to the non annealed Al template. This is because the crystallinity of PMSSQ increased when the annealing temperature increased. However, the Si intensity for sample which was

annealed at 300 °C decreased slightly,that could be due to the centrifugal effect of spin coating PMSSQ layer. The average crystallite size was calculated using the Scherrer equation [19, 20] (Eq. 1) using the full width at half maximum (FWHM) of the Al orientation.

$$d = \frac{0.89\lambda}{\beta \cos \theta} \tag{1}$$

where λ is the X-ray beam wavelength (1.54 Å for Cu K$_\alpha$), β is the FWHM of the Bragg peak, and θ is the peak position. The crystallite sizes are tabulated in Table 2. The non-annealed Al template sample displayed the crystallite size of 42.4 nm. However, the crystallite sizes of Al annealed at 200 °C decreased to 33.0 nm which is in agreement with grain sizes decrement in FESEM images (Fig. 2b) due to annealing process. The crystallite sizes of Al annealed 300, and 400 °C were 48.6 and 59.0 nm, respectively. The crystallite size increased with increasing annealing temperature of the templates because this temperature is higher than typical recrystallization temperature, which is generally ∼250–350 °C [21, 22]. Above recrystallization temperature, small grains tend to form larger grains. However, the crystallite sizes of samples annealed 300 and 400 °C are larger than particle size as observed in FESEM images. Average grain size in FESEM images was classified into two distinct sizes (small and large grains), but crystallite size in XRD analysis was determined by the line broadening of XRD profiles.

In this work, the effects of the annealing temperature of the Al template on the formation of AuNPs were investigated using the hydrothermal method. Figure 4 shows the FESEM images of AuNPs grown using Al templates with varying annealing temperatures. The average particle size of each sample was calculated from FESEM images using ImageJ software, and the results are tabulated in Table 3. The size distribution of the formation of AuNPs is shown in Fig. 5. The size of AuNPs formed on the non-annealed
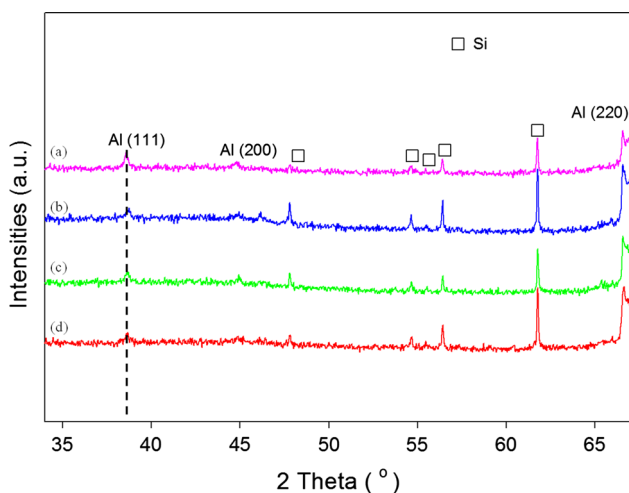
Fig. 3 XRD spectra of sputtered Al templates with varying annealing temperatures: *a* non-annealed template, *b* template annealed at 200 °C, *c* template annealed at 300 °C, and *d* template annealed at 400 °C

Table 2 Crystallite size of Al template

Sample	Average crystallite size (nm)
Non-annealed	42.4
200 °C	33.0
300 °C	48.6
400 °C	59.0

template, templates annealed at 200, 300, and 400 °C are 83, 70, 75, and 113 nm, respectively. AuNPs grown on the non-annealed Al template (Fig. 4a) contained more uniformly distributed compact AuNPs with an area density of 1.48×10^{13} m^{-2} and narrow size distribution (Fig. 5). As the annealing temperature increased to 200 °C, smaller AuNPs formed compared with the sample grown on the non-annealed Al template (Fig. 4b). In addition, AuNPs were far apart from each other with area density of 1.19×10^{13} m^{-2} and broader size distribution. This large distance is due to the template that influences the size, shape, and distribution of NPs [15]. During hydrothermal reaction, AuNPs nucleate on Al grain boundaries with high surface energy sites Al grain boundaries. The increase in annealing temperature increases the grain size of Al templates because of the diffusion of ions [18]. Ion diffusion may lead to the formation of large AuNPs, thereby increasing the distance between AuNPs. The AuNPs grown on the Al template annealed at 300 °C (Fig. 4c) revealed that the distance between AuNPs was far, and the AuNPs increased in size as shown in size distribution (Fig. 5) with area density of 8.01×10^{12} m^{-2}. The AuNPs grown on the Al template annealed at 400 °C (Fig. 4d) showed that the AuNPs become larger and agglomerated because of diffusion, with an area density of 5.93×10^{12} m^{-2} and broad size distribution as in Fig. 5.

The formation of nanomaterials in terms of size, shape, and distribution can be determined by a template [23]. This basic theory is applicable in this study, in which the size and distribution of the AuNPs formed were confined by the template. Au nucleated on a high surface energy site of the grain boundary of the Al template. The grain boundary area between the Al template increased and resulted in the formation of large AuNPs when the Al grain size increased. Therefore, low AuNP area density was observed when larger AuNPs formed. During the hydrothermal reaction, AuNPs formed in a hydrothermal reactive bath because of competitive growth between Au and Al$_2$O$_3$. Two systems are involved in the hydrothermal bath, as shown in Eqs. 2 and 3. The free Gibbs energies (ΔG) of Au and Al$_2$O$_3$ formations were −604.7 and −226.5 kJ/mol, respectively [24–26]. Based on the difference in the ΔG values, the

Table 3 Grain size and area density of AuNPs grown at varying annealing temperatures of Al template

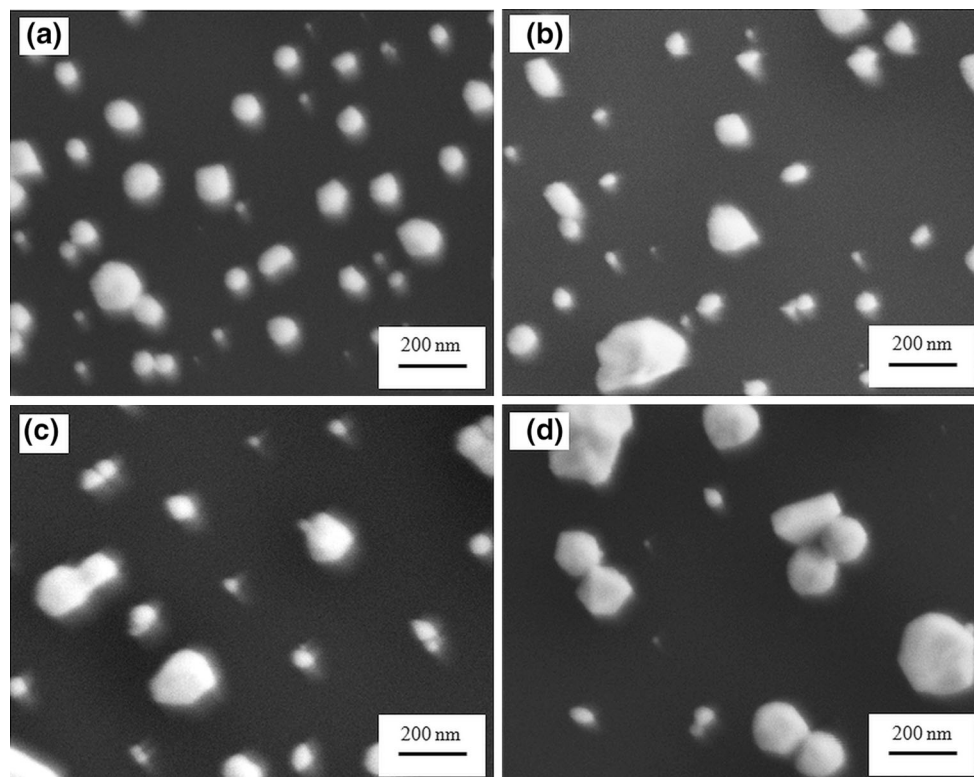| Sample	Size (nm)	Area density (m^{-2})
Non-annealed	83	1.48×10^{13}
200 °C	70	1.19×10^{13}
300 °C	75	8.01×10^{12}
400 °C	113	5.93×10^{12}

Fig. 4 FESEM images for AuNPs grown at varying annealing temperatures of Al template: **a** non-annealed template, **b** template annealed at 200 °C, **c** template annealed at 300 °C, and **d** template annealed at 400 °C
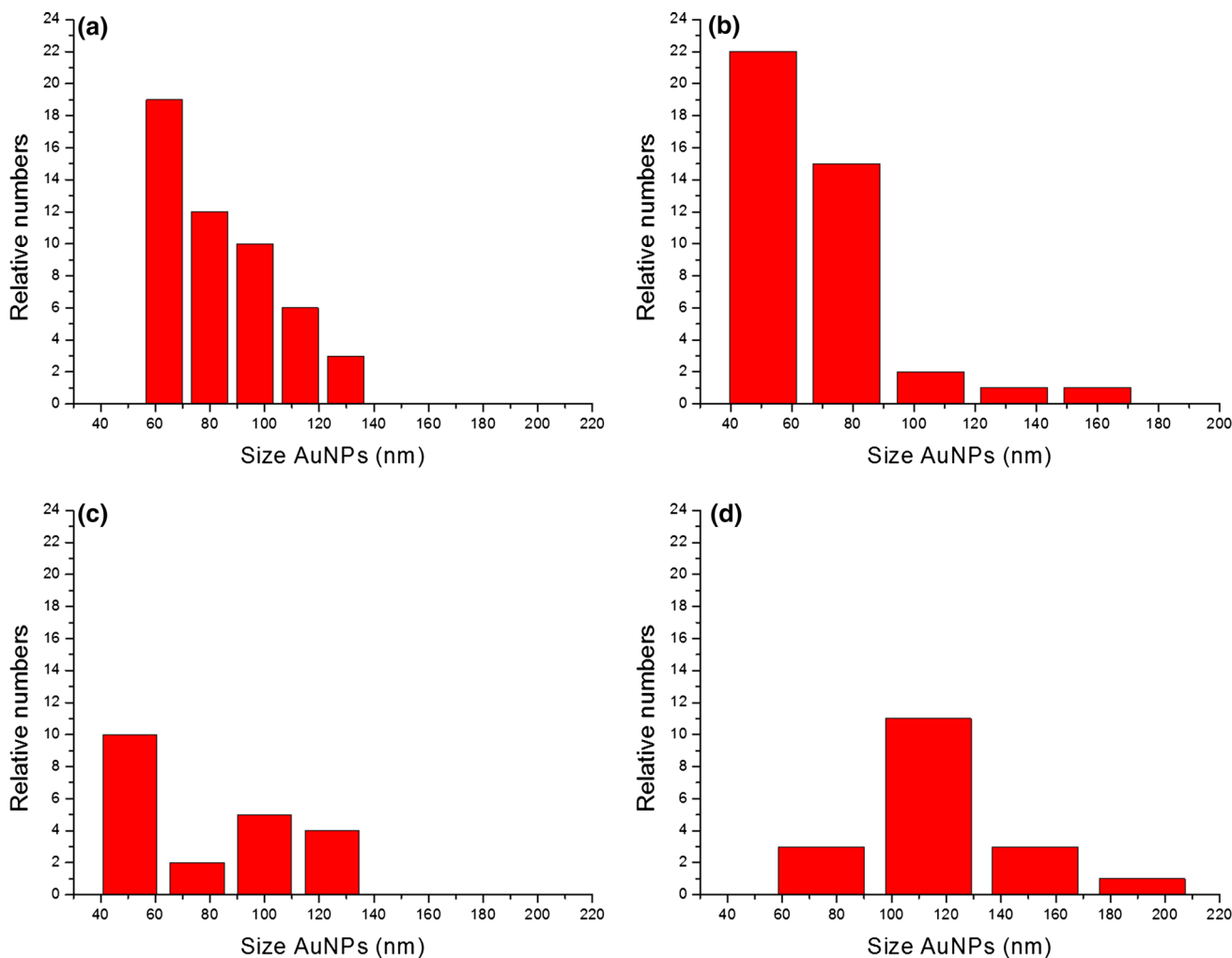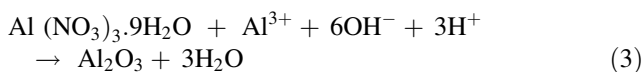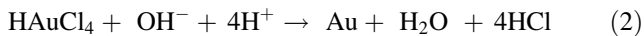
Fig. 5 Size distribution of AuNPs grown at varying annealing temperatures of Al template: **a** non-annealed template, **b** template annealed at 200 °C, **c** template annealed at 300 °C, and **d** template annealed at 400 °C

formation of AuNPs was more favorable because higher negative values result in more spontaneous chemical reactions [24, 25, 27].

$$HAuCl_4 + OH^- + 4H^+ \rightarrow Au + H_2O + 4HCl \qquad (2)$$

$$Al(NO_3)_3 \cdot 9H_2O + Al^{3+} + 6OH^- + 3H^+ \rightarrow Al_2O_3 + 3H_2O \qquad (3)$$

During hydrothermal reaction, the Al template dissolved in the hydrothermal reactive bath because the Al template corrodes under acidic conditions. Al dissolves in acid to form salts that contain aluminum (III) cation, as shown in Eq. 4. The ΔG value is −970.68 kJ/mol, so the chemical reaction proceeds spontaneously in the forward direction [24, 25, 27].

$$2Al + 6H^+ \rightarrow 2Al^{3+} + 3H_2 \qquad (4)$$
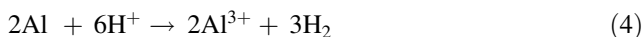
The composition of the AuNP samples in the FESEM image was further confirmed by EDX analysis. The EDX

spectrum in Fig. 6 corresponded to the AuNPs grown on the non-annealed Al template. The results showed the existence of Au, whereas C, Si, and O were from the PMSSQ dielectric layer and Si substrate. This observation proved that the Al template was completely dissolved during the hydrothermal reaction. The same elements were obtained for other samples with different atomic percentages.

The XRD spectra of samples after hydrothermal reaction are shown in Fig. 7. The peaks could be ascribed to FCC gold (JCPDS No.04-0784). The diffraction peaks appeared at 2θ = 38.20°, 44.41°, and 64.54°, which corresponded to the (111), (200), and (220) planes of the standard Au cubic, respectively. The stability of the individual surface planes decreased in the order {111} > {100} > {110} based on the densities and coordination number of the surface atoms [28]. During crystal growth, low-energy [29] planes are more favorable because of high stability [30]. Thus, the intensity of the (111) plane was the highest among the

Fig. 6 EDX analysis of AuNPs after hydrothermal reaction

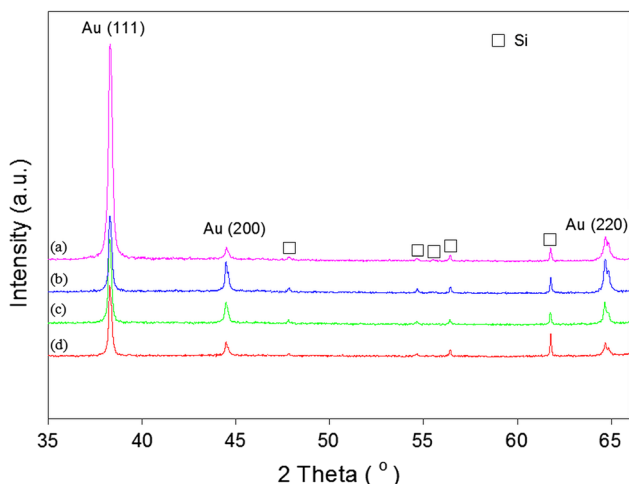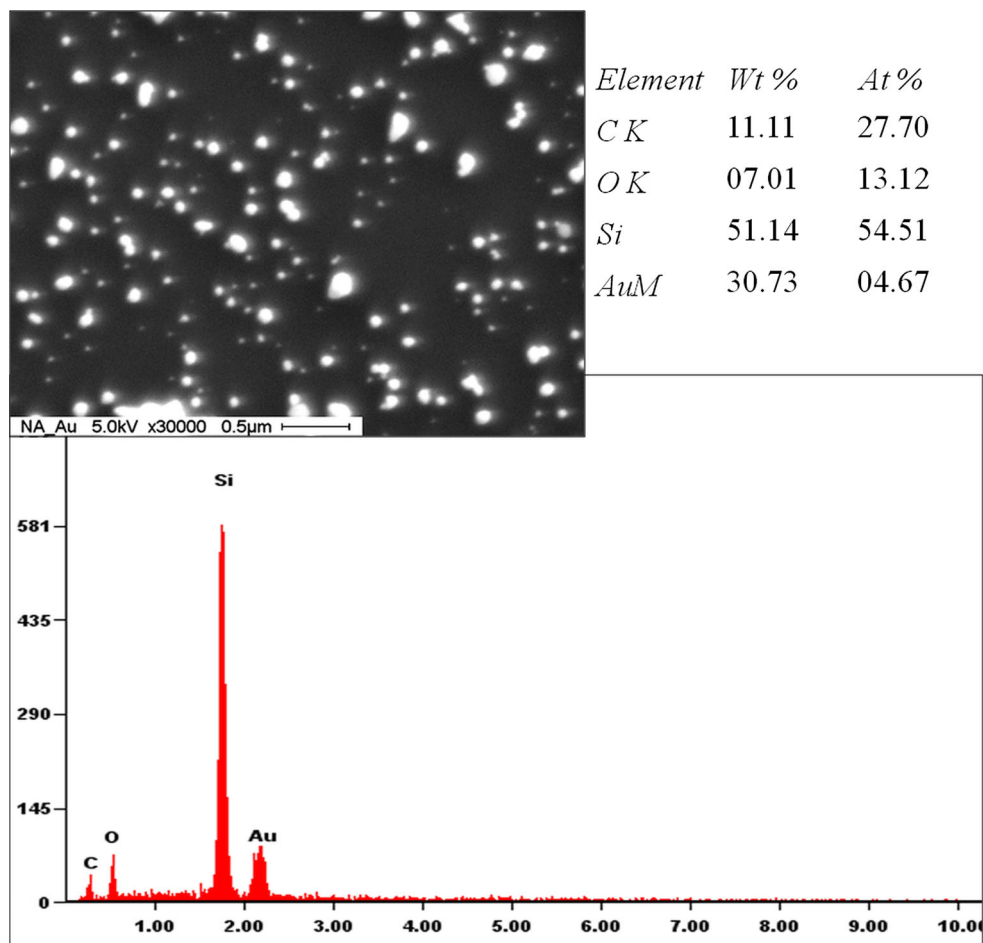| Element	Wt %	At %
$C\,K$	11.11	27.70
$O\,K$	07.01	13.12
Si	51.14	54.51
$Au\,M$	30.73	04.67

Fig. 7 XRD spectra of AuNPs grown on Al template at varying annealing temperatures: *a* template annealed at 400 °C, *b* template annealed at 300 °C, *c* template annealed at 200 °C, and *d* non-annealed template

other planes. Moreover, the intensity of the peak could be affected by several factors such as crystallization, density and thickness of thin film [31]. In this result, the intensity

of the (111) peak increased with increasing annealing temperature that revealed an improvement in crystallinity of the AuNPs with increasing particles size. This finding is in agreement with the FESEM image in Fig. 4a. The Al peak disappeared after the hydrothermal reaction because of the acidic precursor; the pH of the hydrothermal precursor was similar for all sample, that is, the Al thin film dissolved at approximately pH 2, as observed by Hassan et al. [32]. Thus, only AuNPs formed after the hydrothermal reaction.

Among all samples, a strong peak at $2\theta = 38.20°$ indicated a higher population of Au (111), which was the preferred orientation for AuNPs. A similar finding was observed by Chowdhury et al. [33]. Therefore, the average crystallite size was calculated via the Scherrer equation [19, 20] (Eq. 4) using the full width at half maximum (FWHM) of the (111) peak.

The crystallite sizes are tabulated in Table 4. The AuNPs grown on the non-annealed template sample displayed the smallest crystallite size of 41.4 nm, which was in agreement with the grain size observation from FESEM because of the smallest size obtained from the non-annealed template. The crystallite sizes of AuNPs grown at

200, 300, and 400 °C were 49.0, 49.7, and 49.8 nm, respectively. The crystallite size increased with increasing annealing temperature of the templates.

A layer of PMSSQ was spin-coated on the AuNP samples to determine the electrical properties. The Au top and Al bottom contacts were prepared using the thermal evaporation method. The I–V characteristics of PMSSQ-embedded AuNPs at various annealing temperatures of the sputtered Al template are shown in Fig. 8. The I–V characteristics were obtained by sweeping positive voltage from 0 to 10 V and vice versa. In Fig. 8, each of the I–V curves was divided into three distinct regions, namely, Regions 1, 2, and 3, to explain the transport mechanisms of the memory device structure.

The I–V relationship was expressed as I proportional to V^n, and the fitted slope of a double log plot determines the n value of log I proportional to n log V. During the first sweep from 0 V at Region I, the device current increased monotonically with the applied bias, followed by an abrupt current increment in the current flow. In Region 1, the thermionic emission (TE) current conduction occurs at low voltage, which is related to the thermally generated electrons because TE is a process by which heat induces the emission of electrons across a barrier. However, the curve in Region 1 can be fitted by Schottky and Poole–Frenkel emissions because electrons are possibly transported over the Si-PMSSQ interface via Schottky emission and Poole–Frenkel emission in the 250 nm-thick porous silicate PMSSQ. Therefore, electrons from Si are transported across the barrier by thermionic effects via field-assisted lowering at the Si-PMSSQ interface with the combination of the Schottky and Poole–Frenkel emission effect. Similar results were obtained in our previous work using a Zn template [16]. When the bias increased to threshold voltage (V_{th}), the current in Regions 2 and 3 can be described by a space charge limited current (SCLC) model with trapping in the I–V characteristics, as shown in the following expression: $I \propto V^n$. In Region 2, the slopes of the yield $n \gg 2$ indicated that a typical trap-limited SCLC, also known as trapped charge limited current (TCLC), transport mechanism exists. In this region, the trap sites of AuNPs were filled with electrons, and an abrupt increase in current was observed in the I–V measurement. After all traps in the AuNPs were filled, the transport mechanism in Region 3

switched to a trap-free (an ideal SCLC transport mechanism contains $n = 2$; Fig. 8) SCLC. The transport mechanism was in agreement with that reported by Ooi et al. and Lai et al. [34, 35].

During the reverse sweep of bias from 10 to 0 V, current flow was higher than that of the forward sweep because traps were completely filled with electrons. The existence of the memory effect was proven; electrons could be stored when AuNPs with a high range of work function ($\sim$5.0 eV) dispersed randomly in the insulating PMSSQ layer, which captured electrons that were injected from the electrodes. The AuNPs grown using the non-annealed template showed the lowest increment of abrupt current, which was 2.4 V (Table 5). This sample is of particular interest in electrical properties because only low voltage is necessary to turn "on" the memory device.

Counter-clockwise hysteresis was observed in the C–V characteristics (Fig. 9) by sweeping positive voltage from 0 to 10 V and vice versa for the PMSSQ-embedded AuNPs grown using sputtered Al template annealed at varying temperatures. The current increased in all memory devices after forward and reverse sweeps because of the trapped electrons in the AuNP sites [36]. The hysteresis (flat-band voltage shift, ΔV_{FB}) window of the sample prepared on the non-annealed sputtered Al template exhibited the largest hysteresis of 1.2 V, whereas that of the sample prepared on the template annealed at 200 °C was 0.7 V. Hysteresis of 0.6 and 0.9 V were observed in the samples grown on the template annealed at 300 and 400 °C, respectively. To obtain the charge storage capacity per AuNP, ΔV_{FB} was calculated for a single electron ($n = 1$) confined in AuNPs using Eq. 5.

$$\Delta V_{FB} = \frac{nq d_{nanoparticle}}{\varepsilon_{PMSSQ}} \left(t_{gate} + \frac{1}{2} D_{nanoparticle} \right) \quad (5)$$

where n is the number of charges per single AuNP, q is the electron charge magnitude, $d_{nanoparticle}$ is the area density, t_{gate} is the thickness of the control gate (PMSSQ), $D_{nanoparticle}$ is the AuNP diameter, and ε_{PMSSQ} is the dielectric constant of PMSSQ [15, 16]. The data obtained using the C–V characteristics of each sample were also calculated (Table 6). The sample grown on the non-annealed template showed the largest hysteresis among the memory device samples. The sample grown at 400 °C exhibited a higher value of charge stored per AuNP of 60; the FESEM results (Fig. 4) showed that the AuNPs grown on the template annealed at 400 °C had a large size of 113 nm. The result was in agreement with the work by Tseng and Tao, who revealed that large AuNPs (5.5 nm) can store more charges compared with small AuNPs (3 and 1 nm) [37]. However, the existence of agglomerated AuNPs caused inconsistent memory properties that could not be considered as optimum memory. The values of

Table 4 Crystallite size of AuNPs grown at varying annealing temperatures of Al template

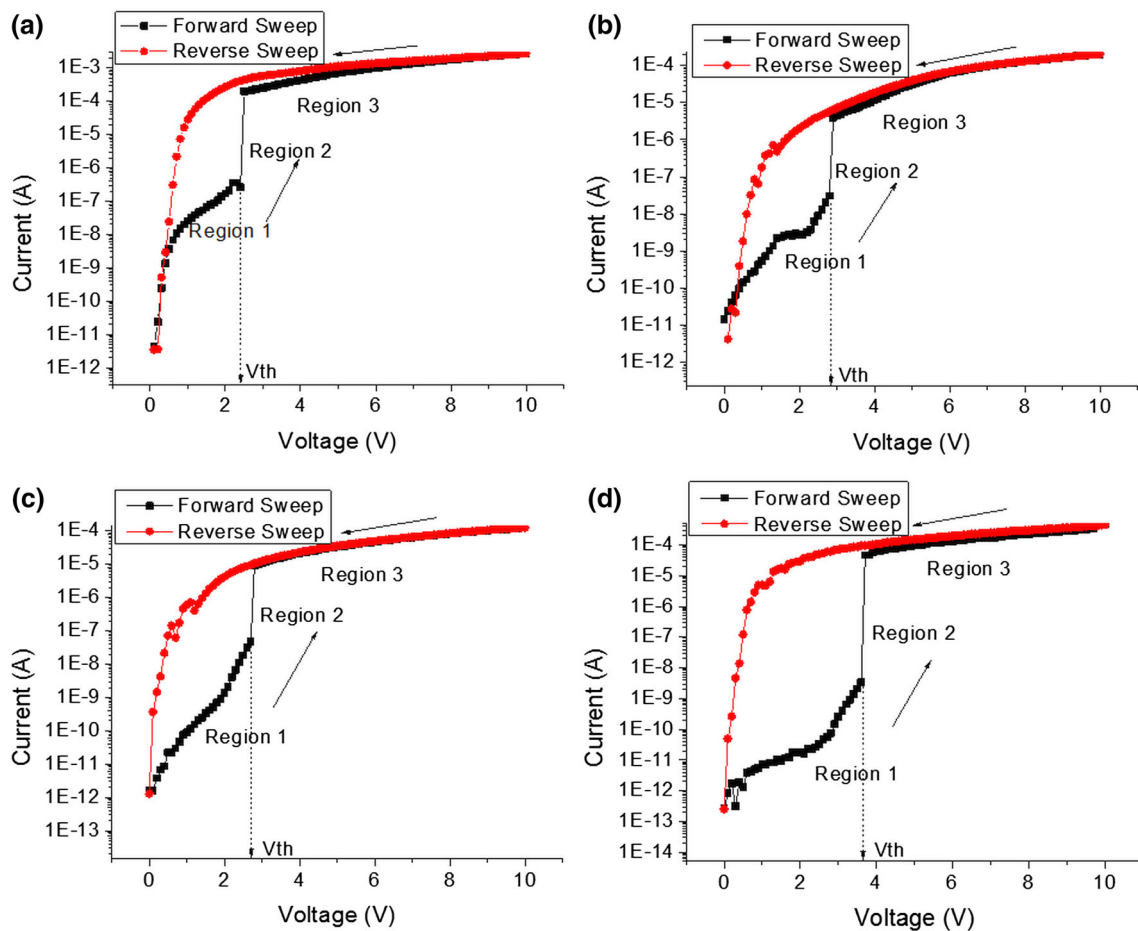| Sample	Crystallite size (nm)
Non-annealed	41.4
200 °C	49.0
300 °C	49.7
400 °C	49.8

Fig. 8 *I–V* characteristics of AuNPs embedded in MIS structure grown at varying annealing temperatures of Al, **a** non-annealed template, **b** template annealed at 200 °C, **c** template annealed at 300 °C, and **d** template annealed at 400 °C

Table 5 Summary of V_{th} of samples at varying annealing temperatures of Al template

Samples	V_{th}
Non-annealed	2.4
200 °C	2.8
300 °C	2.7
400 °C	3.6

charge stored per AuNP of 25 and 32 were observed in the samples grown on the template annealed at 200 and 300 °C, respectively. Therefore, the sample grown on the non-annealed sputtered Al template exhibited optimum memory properties because the charge stored per AuNP was 34. This finding indicated that the presence of isolated and uniform AuNPs was crucial to obtain optimum memory properties.

Our findings indicated that optimum memory properties of AuNPs embedded in PMSSQ were obtained for AuNPs grown on the non-annealed sputtered Al template. This result was due to the lowest turn on voltage (abrupt increased current) of 2.4 V in *I–V* characteristics, although only 34 electrons were stored per AuNP in *C–V* measurement.

Therefore, uniform distribution of size and area density is crucial for excellent memory properties of devices. In a previous study, devices with AuNPs grown on the ZnO seed template annealed at 350 °C can store 49 electrons per AuNP, showing better memory effects than the optimum result in this study, which was 34 electrons per AuNP for devices with AuNPs grown on non-annealed sputtered Al template. However, the use of Al templates could eliminate the requirement of heat treatment, thereby saving time and cost.

4 Conclusion

AuNPs were successfully grown on the Al template followed by the sacrificial hydrothermal process. The size and distribution of AuNPs were dependent on the annealing temperature of the Al template because AuNPs nucleated and grew at Al grain boundaries. Optimum memory properties of AuNPs embedded in PMSSQ were obtained for AuNPs grown on the non-annealed sputtered Al

Fig. 9 *C–V* characteristics of AuNPs embedded in MIS structure grown at varying annealing temperatures of Al, **a** non-annealed template, **b** template annealed at 200 °C, **c** template annealed at 300 °C, and **d** template annealed at 400 °C
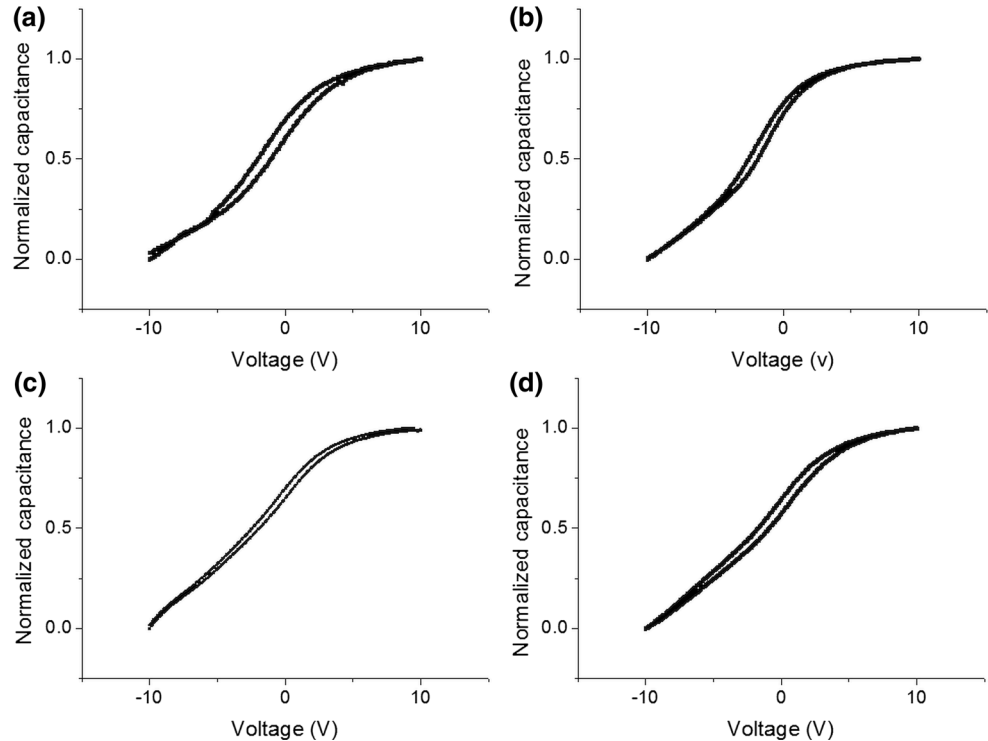

Table 6 Summary of ΔV_{FBO} and number of charge stored per AuNP at varying annealing temperature of Al template

Samples	ΔV_{FB}	No. of stored charge per single AuNP
Non-annealed	1.2	34
200 °C	0.7	25
300 °C	0.6	32
400 °C	0.9	60

template, with the lowest turn on voltage (abrupt increased current) of 2.4 V in *I–V* characteristics and 34 electrons stored per AuNP in *C–V* measurement. These findings proved that uniform AuNPs, in combination with a size of 83 nm and area density of 1.48×10^{13} m^{-2} characterized by FESEM images, contributed to excellent memory effects.

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