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Complex impedance spectroscopy of high-k HfO_2 thin films in Al/HfO_2/Si capacitor for gate oxide applications

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Abstract The dielectric responses of ultrathin (~6.65 nm) HfO_2 films, in the form of Al/HfO_2/Si capacitors were prepared by rf sputtering technique, has been studied in the wide frequency range as a function of deposition temperatures. Deposition temperatures were varied from room temperature (30 °C) to 500 °C. Thickness and the interfacial and surface roughness of heterostructures were extracted by fitting the specular X-ray reflectivity data. The impedance analysis combined with modulus spectroscopy was performed to get insight of the microscopic features like grain, grain boundary and film–electrode interfaces and their effects in the film properties. The films exhibited maximum frequency dispersion in both real and imaginary part of impedance at low frequency range. The frequency analysis of the modulus and impedance studies showed the distribution of the relaxation times due to the presence of grains and grain boundaries in the films. Impedance analysis revealed that the interfacial polarization caused by space charges in the film/electrode interfaces plays an important role in the dielectric behavior of the capacitor. In order to explain effectively that the impedance plots contain one or two arcs due to more than one relaxation contributions, the results are interpreted using the approach proposed by Abrantes (Z' vs. $|Z''|/f$ representation). The dielectric loss (tan δ) curves exhibited the fact that there is possibility of existence of a Schottky barrier at the insulator semiconductor interface, which is due to traps distributed throughout the semiconductor-insulator interface and it is believed to be due to auto doping during deposition process. The ac conductivity, $\sigma_{ac}(\omega)$, varies as $\sigma_{ac}(\omega) = B\omega^n$ with n in the range 0.06–0.71.

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1 Introduction

In last decades tremendous research has been undertaken to replace the conventional SiO_2 gate dielectric in the ultra large scale integrated circuit (ULSIC), by new dielectric materials for the gate stack with permittivity (dielectric constant) higher than that of SiO_2 [1–6]. Attempt to find new suitable gate dielectric materials for future 14 nm node CMOS technologies is because SiO_2 has already been scaled down to its technological and direct tunnelling (<3 nm) limit [5]. Recent research focused mainly on HfO_2, Al_2O_3, ZrO_2, TiO_2, Gd_2O_3, La_2O_3, Y_2O_3, CeO_2, Sm_2O_3 and their silicates [7–14]. HfO_2 and HfO_2-based materials (silicates aluminates and oxynitrides) are being proposed to replace the silicon oxide as they have good dielectric properties with thermal stability on Si substrates [15, 16]. It has been observed that irrespective of deposition methods there are few issues with HfO_2 when the thickness of the film is reduced below 10 nm. The performance of these devices is dependent especially on the formation of an insulator layer, native or deposited, at the MOS interface, interface states (D_{it}) localised at the semi conductor/insulator interface and series resistance R_s. Moreover, the change in bias voltage and frequency has important effect on the electrical and dielectric properties of thin films as a function of deposition temperatures. Therefore a systematic detailed study of effect of deposition temperature on the electrical and dielectric properties of ultrathin film is still a very important research investigation. When a MOS structure is biased in strong accumulation, the frequency-dependent properties of MOS devices can be described via complex impedance. The complex impedance spectroscopy technique is very common for bulk ceramics, has been utilised in case of thin films by many researchers. While a dc measurement

corresponds to the response in time domain, ac measurements pertain to response in frequency domain. It is a powerful and versatile technique to analyze the microstructure property relationship and it also allows distinction between different region intrinsic (bulk) and extrinsic contributions (grain boundary, surface layer and electrode contact problem [17–19]. An equivalent circuit based on the impedance data provides information on the physical processes occurring inside the sample. In this work we present the impedance spectroscopic studies of MOS structure using HfO_2 as gate dielectric on p-type silicon prepared by rf sputtering.

2 Experimental details

Ultra thin hafnium oxide (HfO_2) films (thickness 6.65 nm) were deposited by radio frequency (rf) sputtering technique on 1–20 Ω/cm resistivity p-type silicon substrate. Sputtering was carried out at power of 100 W directly from a high purity HfO_2 target of one inch diameter. Silicon substrates were cleaned by using RCA method. The cleaned substrates were then loaded into the sputtering chamber for deposition of HfO_2 thin films. The base pressure and operating pressure of the sputtering chamber were 5×10^{-5}, 0.180 mbar, respectively. The distance between the target and the substrate was maintained at 4 cm and the deposition was carried out for 45 min. The deposition was done in a reactive gas environment. Argon and oxygen gas was fed into the sputtering chamber in the ratio of 5:1 during sputtering process. Three samples were deposited by varying the deposition temperature from room temperature (30–500 °C) and keeping all other parameters constant. The thickness of film was measured using Grazing incidence X-ray reflectivity GIXRR measurements. Grazing incidence X-ray reflectivity measurements were performed using a Philips X-Pert PRO-MRD diffractometer with CuKα ($\lambda = 0.15418$ nm) radiation operated at 45 kV and 40 mA. The X-ray reflection intensity was collected by a counter with a reception slit of width 0.1 mm. The sample was mounted on a vertical sample stage controlled by a higher-resolution goniometer with a 2θ angular resolution of 0.0002°. For electrical measurements aluminium was deposited as top electrode on HfO_2 thin film through shadow mask using thermal evaporation technique at a base pressure 5×10^{-5} mbar thus making $Al/HfO_2/Si$ MOS capacitors. The area of the top electrodes is 1.8×10^{-3} cm^2. An ohmic contact was also formed on the back side of the silicon substrate by thermally evaporating aluminium metal. The impedance measurements were carried out using keithely 4200 SCS at room temperature in the frequency range 5 kHz–5 MHz.

3 Results and discussion

3.1 Thickness and interfacial roughness

The surface and interface quality HfO_2/Si heterostructures have been investigated through the analysis of X-ray reflectivity. Figure 1 shows the XRR spectrum of the film deposited at substrate temperature 500 °C. The specular reflectivity is plotted as a function of the vertical momentum transfer $q_z = 4\pi\sin\theta/\lambda$ (incidence angle equal to reflection angle), where q_z is the momentum transfer perpendicular to the sample surface, θ is the grazing incidence angle, and λ is the wavelength of the X-rays. The specular reflectivity data has been fitted using the Parratt algorithm [20] in which the surface or interface root-mean-square (rms) roughness, thickness, and density of each constituent layer are the fitting parameters. Almost uniform oscillations in the reflectivity curve, starting from q_z value of 0.05–1.2 are observed. This indicates that the deposited film is smooth with low surface and interface roughnesses. Fitting results revealed that there is a thin top surface layer of slightly different electron density from bulk HfO_2 and thickness of the HfO_2 layer is found to be 6.65 nm from fitting result. However an interfacial layer (SiO_2) of thickness 1.2 nm is obtained from the fitting results. We attributed the SiO_2 layer formation during deposition of the film at elevated temperature (Table 1).

3.2 Impedance analysis

To study the frequency dependent property of the fabricated MOS capacitors the impedance spectroscopy analysis was performed on the three samples. For our convenience the film deposited at room temperature is named as X1, while film deposited at 300 °C and at 500 °C is named as X3 and X5, respectively. The use of impedance

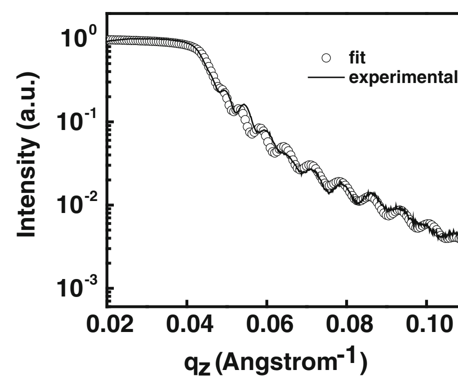

Fig. 1 Specular X-ray reflectivity plotted as a function of $q_z = 4\pi \times \sin\theta/\lambda$, where q_z is the momentum transfer perpendicular to the sample surface, θ the incidence angle and λ the wavelength of X- ray for HfO_2 film deposited at 500 °C

Table 1 Extracted parameters from X-ray reflectivity curve

Parameters	Surface layer	As-deposited HfO_2 (6.65 nm)/Si	SiO_2
d (Å)	7 ± 0.2	66.5 ± 0.8	12.0 ± 0.2
σ (Å)	3.5 ± 0.1	8 ± 0.2	3 ± 0.1
δ	5.205×10^{-5}	3.865×10^{-5}	2.445×10^{-6}
β	4.305×10^{-6}	3.765×10^{-5}	1.465×10^{-7}

The fitting parameters are layer thickness (*d*), interfacial roughness (*σ*) and the real and imaginary parts of the index of refraction *δ* and *β*, respectively

spectroscopy to characterise grain, grain boundary and electrode contributions by exhibiting successive semi circles (often with some distortion) of the impedance (real and imaginary part) in complex plane is well established [21, 22]. In case of Al/HfO_2/p-Si MOS capacitors there is no distinct grain boundary but only bulk and interfaces (HfO_2/p-Si and Al/HfO_2) can contribute to the dielectric relaxation [23]. Figure 2 shows the impedance plane plots for all the three samples at various bias voltages.

The characteristic semicircles could be obtained only in the depletion and accumulation region i.e. under the negative bias condition only. The impedance spectra ($Z^{/}$ vs. $Z^{//}$) are usually analysed in terms of complex formalism for the impedance $Z^{*} = Z^{/} + iZ^{//}$. Figure 2a–c show the impedance spectra of the three samples deposited at RT (X1), 300 °C (X3) and 500 °C (X5). The spectra depicted the characteristic semicircles. The semicircle in the high frequency region corresponds to the dielectric response of the bulk and the semicircles in the low frequency region correspond to the top and bottom interfaces. The impedance spectra of the sample X1 and X5 show two distinct semicircles while the impedance spectrum of the sample X3 also shows trace of a third semi circles in the low frequencies and at low voltages up to −1.5 V. To understand better the contributions from different relaxations with relatively small differences in time constants the alternative $Z^{/}$ versus $|Z^{//}|/f$ representation (at −1.5 V) proposed by Abrantes et al. [24] has been used. Accordingly, in Fig. 2d two well defined regions with different slopes are observed for all three samples. It confirms that there are two distinct regions of frequency response for the three samples originating from two different dielectric responses. It is also observed that frequency at which the two regions separated increased with increase in substrate temperature.

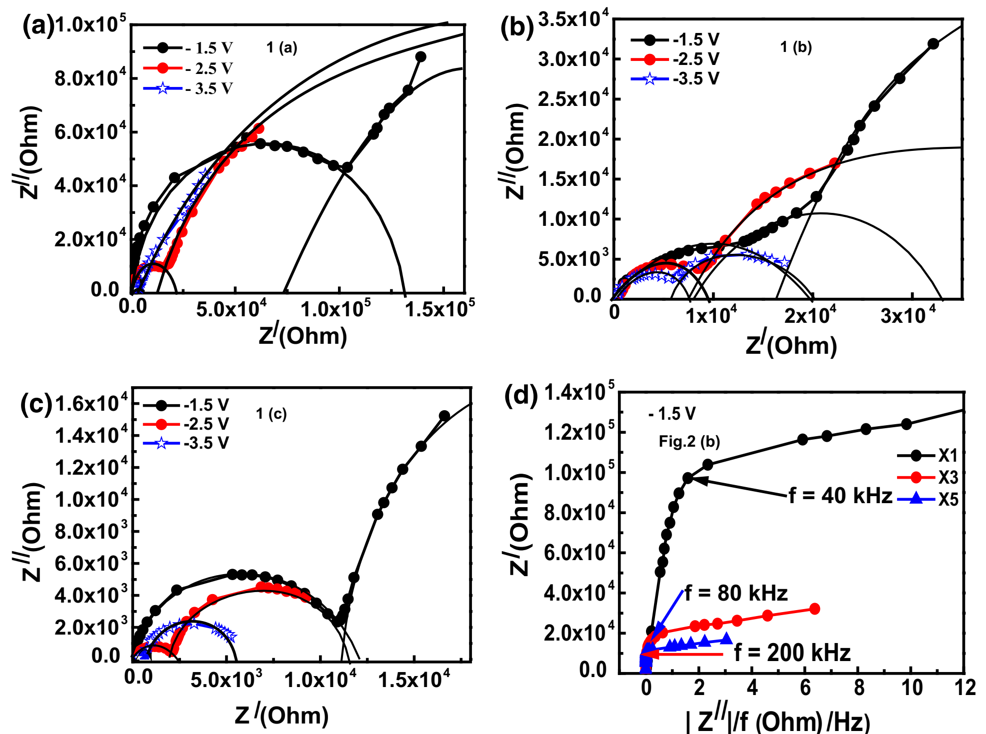

Fig. 2 **a–c** The complex impedance spectra of the samples X1, X3 and X5, respectively. *Solid line* is the fitting results. **d** $Z^{/}$ versus $Z^{//}$/f curves of X1, X3, and X5 at a bias voltage −1.5 V

The ($Z^{/}$ vs. $Z^{//}$) plots show that the semi circles in the low frequency region of X3 overlapped at higher voltages which indicates the very small difference in the relaxation time. The second semicircle of the sample X1 is almost a straight line making an angle $\sim 45°$ with the real axis indicating very high resistance of the interfacial layer correspondingly very low relaxation frequency [25]. At low biasing voltages (<-3.5 V) the interfacial layer impedance dominates in all the samples. But from -3.5 V, the second semicircle in the lower frequency range in X3 and X5 bends indicating that the resistance of the grain-bulk region and the resistance of the interfacial region are comparable and both determine the observed frequency response. For all the samples the grain bulk resistance and the interfacial layer resistance decreased with increase in biasing voltage. The overall comparison of the impedance spectra of the three samples show that the resistance of grain bulk (R_g) and the resistance of interfacial layer (R_{il}) decreased with increase of deposition temperature. An electrical analog circuit representation applicable to our case will be a series combination of grain, interface and electrode elements and is shown in Fig. 3. The grain circuit consists of parallel combination of grain resistance (R_g) and grain capacitance (C_g), the grain boundary circuit i.e. the interfacial layer consists of parallel combination of interface resistance (R_{il}) and interface capacitance (C_{il}) and the electrode circuit (applicable only at -1.5 V for sample X3) consists of parallel combination of electrode resistance (R_e) and electrode capacitance (C_e) [19].

The equivalent electrical equation can be represented by

$$Z^{*} = Z^{/} - iZ^{//} = \frac{1}{R_g^{-1} + j\omega C_g} + \frac{1}{R_{il}^{-1} + j\omega C_{il}} + \frac{1}{R_e^{-1} + j\omega C_e} \quad (1)$$

From the intercepts of the semicircular arcs on the $Z^{/}$ axis, R_g, R_{il} and R_e, can be evaluated. The R_e values of X3 are very high beyond the range of our instrument. The R_{il} values for lower voltages also could not be calculated for the same reason. The value of capacitance C can be calculated from the relation ω_{max} RC = 1 where $\omega_{max} = 2\pi f_{max}$, where f_{max} is the frequency that corresponds to maximum peak of the semicircles. It is also known that the mean relaxation time (τ) can be calculated from the equation [19] $\omega_{max}\tau = 1$ (Table 2).

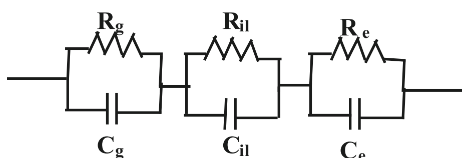

Fig. 3 Analog electrical circuit model for Al/HfO_2/p-Si MOS capacitors

The R_{il} value of the samples X1 X3 and X5 estimated from the impedance spectra at -3.5 V are 48, 15 and 5 kΩ, respectively. The τ values are calculated to be 1.7×10^{-5}, 1.13×10^{-5} and 7.9×10^{-6} s, for X1, X3 and X5, respectively. The capacitance values are as follows 3.68×10^{-10}, 7.58×10^{-10}, 1.59×10^{-9} F. Hence, at higher voltages the relaxation time of the bulk grain varies from 10^{-6} to 10^{-8} s, while that of the interfacial layer varies from 10^{-5} to 10^{-6} s. The capacitance values for the bulk are in the range of 10^{-11} F while the capacitance of the interfacial layer is in the range of 10^{-9}–10^{-10} F.

3.3 Dielectric permittivity

The dielectric properties of a structure can be obtained from complex permittivity defined as [26]

$$\varepsilon^{*} = \varepsilon^{/} - i\varepsilon^{//}, \quad (2)$$

where $\varepsilon^{/}$ and $\varepsilon^{//}$ are the real and imaginary parts of complex permittivity and can be expressed by the following equations.

$$\varepsilon^{/} = \frac{-Z^{//}}{(2\pi f \varepsilon_0)(Z^{/2} + Z^{//2})} \cdot \frac{d}{A}, \quad (3)$$

$$\varepsilon^{//} = \frac{Z^{/}}{(2\pi f \varepsilon_0)(Z^{/2} + Z^{//2})} \cdot \frac{d}{A}, \quad (4)$$

where d, A and ε_o are the thickness of HfO_2 film, area of electrode and permittivity of free space (8.85×10^{-12} F/m), respectively.

Figure 4a–f illustrates the frequency dependence of the $\varepsilon^{/}$ (real) and $\varepsilon^{//}$ (imaginary) parts of dielectric constant of all the three MOS capacitors. It is observed that the values of real part of complex permittivity ($\varepsilon^{/}$) and imaginary part of complex permittivity ($\varepsilon^{//}$) increases with decrease of frequency and is found to be high in the low frequency region. This can be attributed to the Maxwell–Wagner type of interface polarisation [27]. This may be due to the fact that the interfaces between HfO_2 and p-Si have different conductivities; this causes an additional polarisation which boosts the dielectric constant. The high values of $\varepsilon^{/}$ and $\varepsilon^{//}$ at low frequencies and small values at high frequencies suggests that strong dielectric relaxation occurs in the capacitors at low frequencies. This increase of $\varepsilon^{/}$ values at low frequencies and decrease with increasing frequency is observed in many MOS systems [28, 29]. A simple way to explain this is to assume the presence of interfacial traps states. The lower the frequency, the more the interface traps can follow the alternate current variation and thus the larger the interface trap capacitance which leads to the anomalous frequency dispersion contributing to the total capacitance. The values of dielectric constant of HfO_2 thin

Table 2 Calculated values of grain resistance (R_g), grain capacitance (C_g), relaxation time (τ) at various bias voltages for all three samples obtained from $Z^{//}$ versus $Z^{/}$ plots as shown in Fig. 2

Bias voltage	Sample deposited at RT X1			Sample deposited at 300 °C X3			Sample deposited at 500 °C X5		
(V)	R_g (kΩ)	τ (s)	C_g(F)	R_g (kΩ)	τ (s)	C_g(F)	R_g (kΩ)	τ (s)	C_g(F)
−1.5	120	1.8×10^{-6}	1.56×10^{-11}	20	3.98×10^{-7}	1.99×10^{-11}	12	1.76×10^{-7}	1.47×10^{-11}
−2.5	20	3.18×10^{-7}	1.59×10^{-11}	12	3.18×10^{-7}	2.65×10^{-11}	2.2	3.98×10^{-7}	1.8×10^{-11}
−3.5	5	6.4×10^{-8}	1.27×10^{-11}	7.5	2.89×10^{-7}	4.02×10^{-11}	0.8	2.65×10^{-8}	3.31×10^{-11}

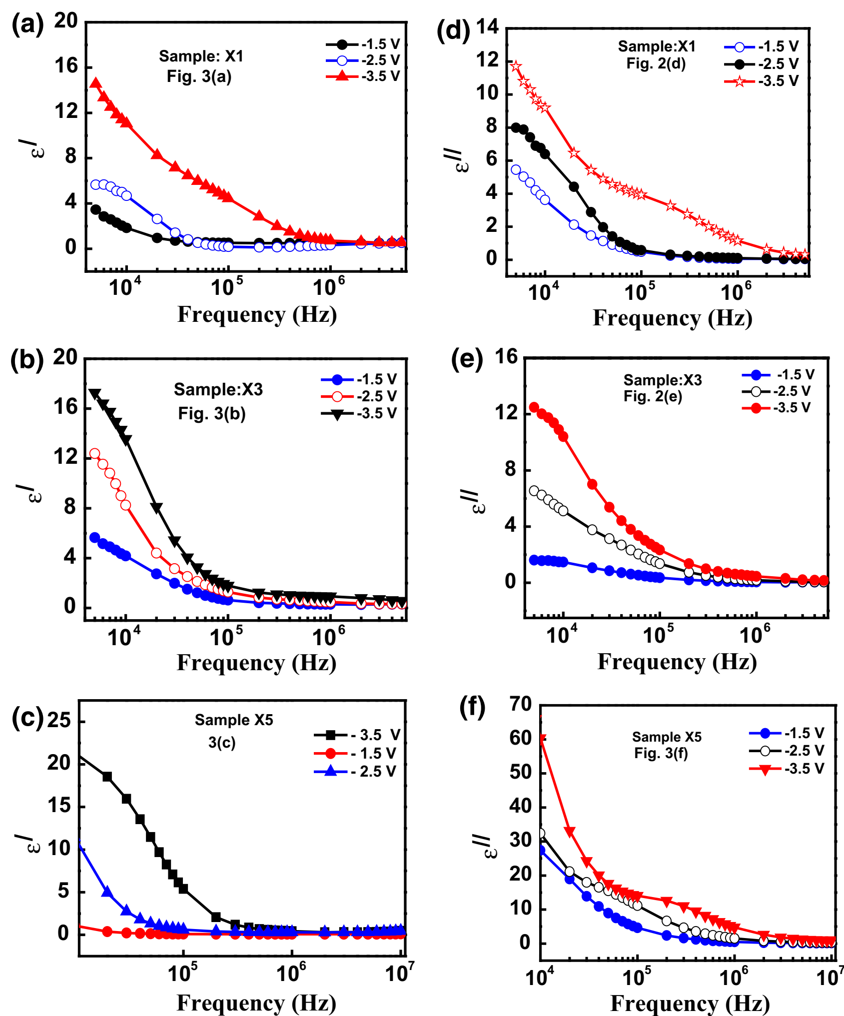

Fig. 4 **a–c** The real part of complex permittivity ($\varepsilon^{/}$) as a function of frequency for sample X1, X3 and X5, respectively and **d–f** imaginary part of complex permittivity ($\varepsilon^{//}$) as a function of frequency for samples X1, X3 and X5

film obtained from our study are comparable with those of reported values [4]. The $\varepsilon^{/}$ value increased with increase in biasing voltage in all the capacitors and its value is highest for the X5 capacitor. Figure 4d–f show the variation of dielectric loss ($\varepsilon^{//}$) of the films with frequency at different voltages. It is observed that in the lower frequency region, dielectric loss is linearly decreases with the increase of frequency. The $\varepsilon^{//}$ values are highest in the capacitor X5 indicating its values increased with substrate temperature.

3.4 Dielectric loss (tan δ)

The dielectric loss (tan δ) of the thin films are calculated from the following equation

$$\tan \delta = -\frac{Z^{/}}{Z^{//}}, \quad (5)$$

where $Z^{/}$ and $Z^{//}$ are the real and imaginary parts of complex impedance.

Figure 5a–c shows the dielectric loss (tan δ) as a function of frequency of the $Al/HfO_2/p\text{-}Si$ MOS capacitors.

The tan δ is found to increase with frequency at different bias voltage, pass through a maximum value (tan δ) max, and thereafter decreases. As the bias voltage is increased, the frequency at which (tan δ) maximum occurred shifted to higher frequencies. This type of behaviour of tan δ has been reported by other researcher's also [30]. It is similar to that reported by Simmons et al. [31] for thin films, having parallel resistance (*R*) and capacitance (*C*) of the materials in series with a parallel combination of Schottky barriers capacitances. The dielectric loss tangent peak in case of X1 and X5 shifted towards higher frequency with increase in the bias voltage. For X3 the peak value shift was less but the peak height decreased with increase in bias voltage. The X5 capacitor showed the highest dielectric loss among all three capacitors.

3.5 Impedance and modulus spectroscopy

Sinclair and West [15] suggested the combined use of impedance and modulus spectroscopy plots. The data regarding complex modulus can be expressed by the following equations.

$$M^{*} = \frac{1}{\varepsilon^{*}} = M^{/} + iM^{//}, \quad (6)$$

$M^{/}$ is the real part of M^{*} and $M^{//}$ is the imaginary part of M^{*}, where $M^{/} = \frac{\varepsilon^{//}}{(\varepsilon^{/2} + \varepsilon^{//2})}$ and $M^{//} = \frac{\varepsilon^{/}}{(\varepsilon^{/2} + \varepsilon^{//2})}$

The advantage of using impedance and modulus spectroscopy plots together is that $Z^{//}$ plots highlights the phenomena with largest resistance and $M^{//}$ plots picks up those with the smallest capacitance. The imaginary part of impedance $Z^{//}$ and modulus $M^{//}$ was plotted with frequency as shown in the Figs. 6a, b, 7a, b and 8a, b for different bias voltages. In an ideal Debye type relaxation the peaks in $Z^{//}$ and $M^{//}$ curves coincide and further the FWHM of these peaks should be less than 1.14 decades. Both these conditions are not satisfied by the curves of the fabricated MOS capacitors. Hence the relaxation observed is non Debye type relaxation [9]. This happens due to intrinsically dispersive nature of the thin films. The variation of $Z^{//}$ with frequency (f) at different voltages shows magnitude of $Z^{//}$ decreases with increase in frequency and bias voltage. At a low voltages (−1.5 V), a peak is observed. The peak height is least for the sample X3. The peak height for the three samples decreases with increase in bias voltage and finally they merge in the high frequency domain indicating presence of space charge polarisation at lower frequencies and its disappearance at higher frequencies. At high voltages two peaks are observed for X3 and X5 which confirms presence of two relaxation times in the system. The peaks of $M^{//}$ curves represents the conductivity relaxation peak. The peaks shift towards higher frequency with increase in biasing voltages revealed that the relaxation time decreases as the conductivity increases.

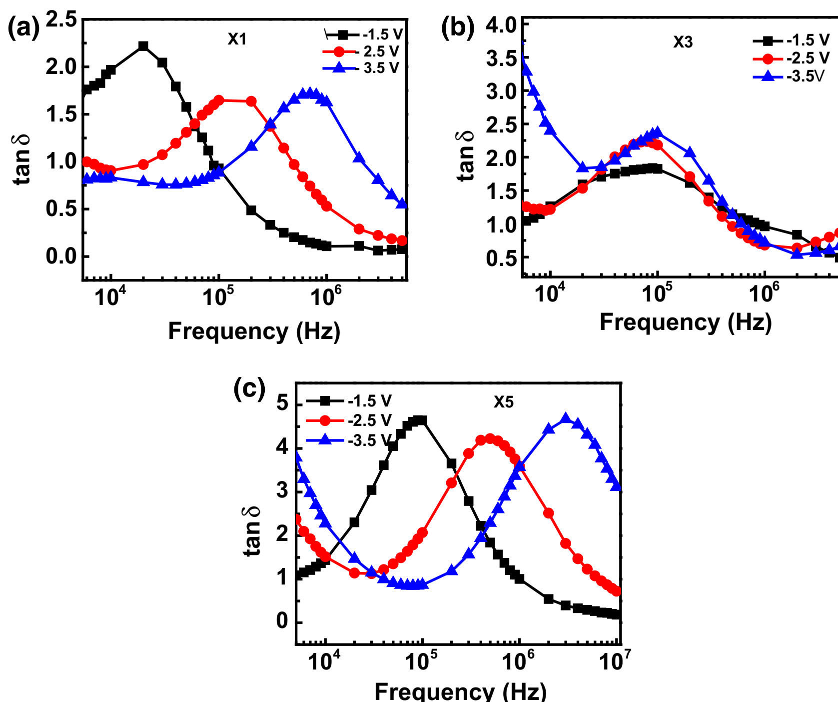

Fig. 5 a–c The variation of tan δ with frequency for the sample X1, X3 and X5, respectively

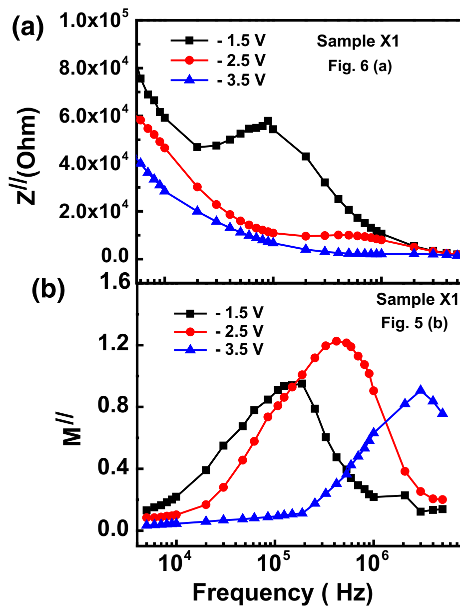

Fig. 6 **a**, **b** The imaginary impedance ($z^{//}$) versus frequency and imaginary modulus ($M^{//}$) versus frequency curves of X1

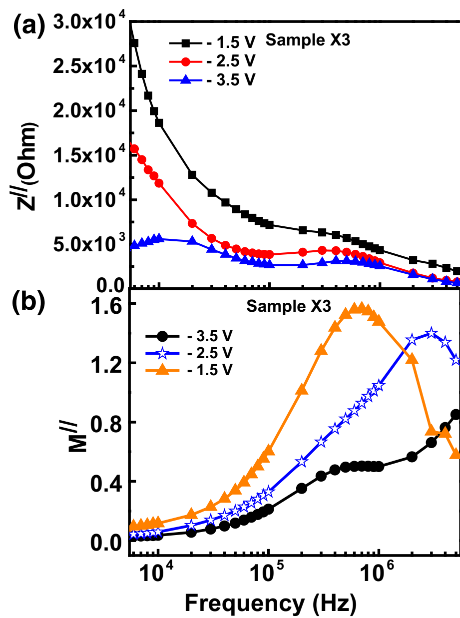

Fig. 7 **a**, **b** The imaginary impedance ($z^{//}$) versus frequency and imaginary modulus ($M^{//}$) versus frequency curves of X3

The conductivity relaxation time can be calculated from the relation as given below.

$$2\pi f_{max} = \frac{1}{\tau_\sigma}, \tag{7}$$

where τ_σ is the conductivity relaxation time and f_{max} is the frequency corresponding to $M^{//}$ maximum.

Figure 9 shows that at a particular biasing voltage the conductivity relaxation time decreases with increase in substrate temperature.

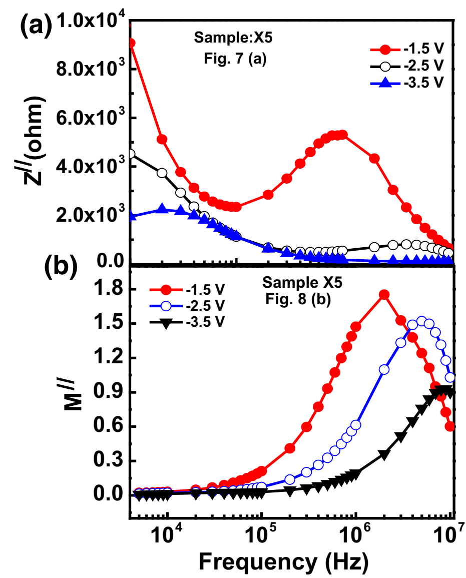

Fig. 8 **a**, **b** The imaginary impedance ($z^{//}$) versus frequency and imaginary modulus ($M^{//}$) versus frequency curves of X5

3.6 ac conductance

The ac electrical conductivity σ_{ac} of the dielectric MOS capacitors was obtained by the following equation

$$\sigma_{ac} = \varepsilon^{//}\omega\varepsilon_0 \tag{8}$$

Figure 10a–c shows the frequency dependence of ac conductivity (σ_{ac}) of X1, X3 and X5, respectively at different bias voltages. The curves show that ac conductivity is frequency independent in the lower frequency region and then increases rapidly with increase of frequency, which is representative of dc leakage current throughout the sample. The σ_{ac} value also increased with increase of biasing voltage. The increase of conductivity with frequency could be due to release of trapped charges in the system. The

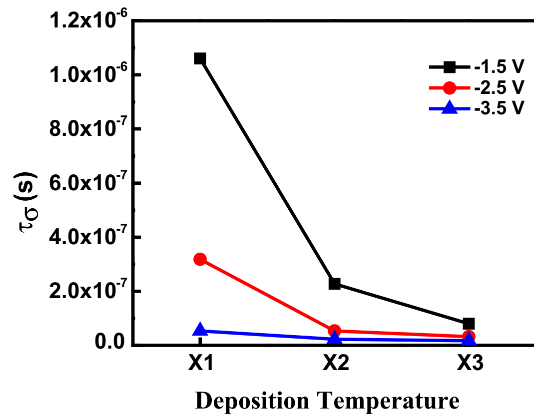

Fig. 9 Variation of conductivity relaxation time with deposition temperature

onset (switch from frequency-independent region to frequency dependent region) varied with deposition temperature.

The variation of conductivity with angular frequency at different voltages can be investigated by applying Jonscher [32] law as given below

$$\sigma_{ac} = \sigma_{dc} + B\omega^{n}, \quad (0 < n < 1) \tag{9}$$

where B is a constant with voltage dependence σ_{dc} is the dc conductivity, ω is the angular frequency. The term $B\omega^{n}$ includes the ac dependence and represents all dispersion phenomena. The n value has been calculated from the linear part of σ_{ac} versus ln ω curve at higher frequencies [9, 33]. The n values were found to vary between 0.06 and 0.708 for the film deposited at room temperatures (X1), and n values for the film deposited at 300 °C (X3) were almost equal to that of X1, however, it decreases with rise in deposition temperature to 500 °C (X5). So, it is evident the present observed ac conductivity with frequency obeys universal power law. The n values of the three capacitors increases with the increase in biasing voltage, however remains less than unity in all the cases (Table 3).

The table shows that the n value is highest in X5 in lower voltages but with increase in bias voltage the n value increase was less in X5 compared to X1 and X3.

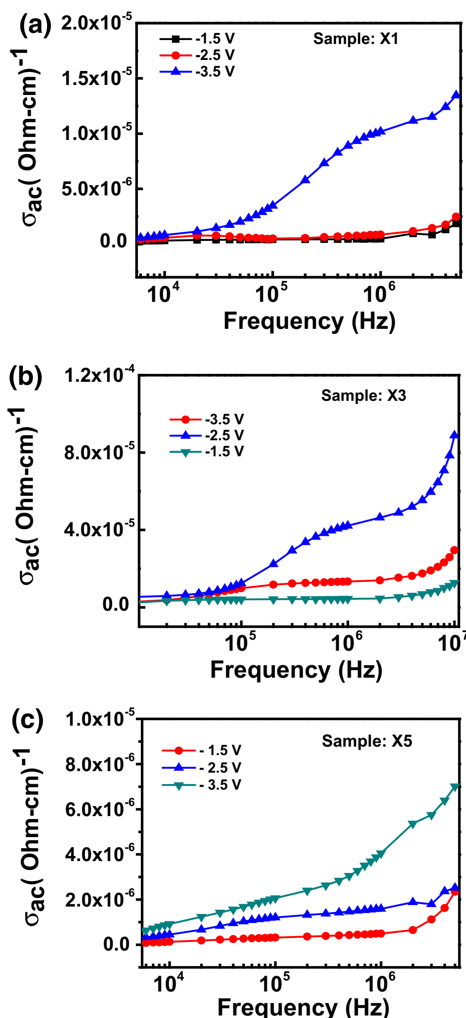

Fig. 10 a–c The frequency dependence of ac conductivity (σ_{ac}) for X1, X2 and X5, respectively

4 Conclusions

We have fabricated MOS heterostructures with HfO_2 as gate dielectric layer. Interfacial and surface roughnesses were extracted by fitting the specular X-ray reflectivity data using parrat simulation software. The frequency dependent dielectric properties and ac electrical conductivity of three Al/HfO_2/p-Si (MOS) structures fabricated at different deposition temperature has been studied in detail in frequency range (5 kHz–5 MHz). The (Z' vs. Z'') curves showed that the resistance of the interfacial layer is very high for the sample deposited at RT (X1) for all biasing voltages but in case of samples deposited at 300 and 500 °C (X3 and X5) the resistance of interfacial layer decreased and was compatible with the bulk resistance. The ε' and ε'' values were found to be very high in the low frequency region which may be attributed to the increase in mobility of the charge carrier at interface state. The tan δ curves indicated to the fact that there is possibility of existence of a Schottky barrier at the insulator semiconductor interface. Such barriers are possible if there are traps throughout the insulator band gap or insulator is auto doped during deposition process. The study of Z'' and M'' curves showed that the relaxation observed in the curves is non Debye type relaxation. The conductivity relaxation time decreased with increase in substrate temperature. The ac conductance increased with biasing voltage in all the capacitors. The study of variation of conductivity with angular frequency at different voltages using Jonscher law shows that the variation was least for the film obtained at deposition temperature 500 °C (X5). The dielectric constant varied between 8 and 14 for the films deposited at room temperature, 300 and 500 °C, respectively, at a frequency 50 kHz at a bias voltage of −3.5 V. An overall analysis of experimental results exhibited that the interfacial layer

Table 3 Variation of n for X1, X3 and X5 at bias voltages 1.5, 2.5 and 3.5 V, calculated from slope of the graph (σ_{ac} vs. ln ω)

Biasing voltage (V)	Sample X1	Sample X3	Sample X5
1.5	0.060	0.120	0.217
2.5	0.609	0.616	0.292
3.5	0.708	0.710	0.301

influences greatly the dielectric property of the fabricated (Al/HfO_2/p-Si) MOS capacitors. The study revealed that the values of ε' and ε'', tanδ, Z'' and M'' and σ_{ac} are strongly dependent on both the applied voltage and frequency especially at depletion and accumulation regions.

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