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# Schottky barrier characteristics of Pt contacts to all sputtering-made *n*-type GaN and MOS diodes

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**Abstract** All sputtering-made Pt/*n*-GaN [metal–semiconductor (MS)] and Pt/$SiO_2$/*n*-GaN [metal–oxide–semiconductor (MOS)] diodes were investigated before and after annealing at 500 °C. *n*-GaN, Pt, and $SiO_2$ films were all fabricated by the cost-effective radio-frequency sputtering technique. A cermet target was used for depositing GaN. The Schottky barrier heights (SBHs) of both MS and MOS Schottky diodes have been investigated by the current–voltage (*I–V*) measurements. The results showed that SBHs increased after annealing at 500 °C for 20 min in $N_2$ ambient, compared to the as-deposited at 400 °C. By using Cheung's and Norde methods, the highest SBHs of MOS Schottky diodes were respectively found to be 0.79 and 0.91 eV for the as-deposited and had reached to 0.81 and 0.94 eV after annealing. The annealed Schottky diode had showed the higher SBH, lower leakage current, smaller ideality factor, and denser microstructure.

## 1 Introduction

High thermal conductivity, high electron mobility, high electron saturation velocity, and large band gap of nitride-based materials have attracted many research interests in recently years. The nitride-based materials have brought promising future for the application of electronic devices such as metal–oxide–semiconductor field effect transistor (MOSFET) and hetero junction field-effect transistor (HJ-FET), Schottky diode, laser, light emitting diode (LED) etc. [1, 2]. The wide range of practical applications of GaN and its related alloys make them receive much attention in many studies. In addition, metal–oxide–semiconductor structures are very important for studying electronic devices. The development of a thin insulator with high–quality for the catalytic metal–insulator–GaN Schottky diode has become a key issue [3–5].

Metal–semiconductor (MS) and metal–oxide–semiconductor (MOS) GaN Schottky diodes have been used and considered as the important and crucial materials. To improve the leakage current through the Schottky contacts to III–V nitride-based semiconductors, *n*-GaN epitaxial layers with low dislocation density are preferred [2]. The drawback of large leakage current has the effects on operation, power consumption, noise, and reliability of the electronic devices. Therefore, ultra-low leakage current is one of the challenges for HJ Schottky contacts to their applications in electronic devices and optoelectronics. To reduce the leakage current and to improve the breakdown voltage in Schottky barrier diodes, it can be achieved with a high Schottky barrier at the MS interface. High-quality Schottky contacts to *n*-GaN for both MS and MOS diodes with a high barrier and good thermal stability have been the important factors for improving electrical properties of diodes [2, 6]. Metals (Au, Pt, Ni, W, Pd, Ru, Ir etc.) with a high work function have been used as contacts to GaN for forming the Schottky contacts.

For the MS Schottky diodes, Rajagopal Reddy et al. [1] studied the effect of annealing temperature on electrical characteristics of Cu/Au alloy Schottky contacts to *n*-GaN by means of current–voltage (*I–V*) and capacitance–voltage (*C–V*) techniques. They concluded that Schottky barrier heights (SBHs) of the as-deposited *n*-GaN Schottky diode were 0.6 eV (*I–V*) and 0.77 eV (*C–V*). Upon annealing at 300 °C, the maximum SBHs of 0.77 and 1.18 eV were

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achieved from *I–V* and *C–V* tests, respectively. In the other paper, they also investigated the effect of rapid thermal annealing on electrical and structural properties of Pd/Ru Schottky contacts to *n*-GaN [7]. They determined that the as-deposited Ru/Pd/*n*-GaN diode yielded SBHs of 0.67 eV (*I–V*) and 0.79 eV (*C–V*), respectively. Furthermore, it was observed that higher SBHs were found to be 0.80 eV (*I–V*) and 0.96 eV (*C–V*) after annealing at 300 °C. Jun Wang et al. investigated the as-deposited Pt/*n*-GaN Schottky diode and calculated the SBH of 0.82 eV from *I–V* measurement. They found that there was a slight increase in SBH of Pt/*n*-GaN contacts after annealing at 500 °C, meanwhile the SBH decreased greatly after annealing above 600 °C [8]. Ramesh et al. also measured the SBH of Mo/*n*-GaN for the as-deposited and was found to be 0.81 eV (*I–V*) [9]. Upon annealing at 400 and 600 °C, SBHs were determined to be 0.74 and 0.56 eV, respectively. Siva Pratap Reddy et al. [10] studied the effect of annealing temperature on interface properties of Ni/Ru/*n*-GaN. They found that SBHs for the as-deposited Schottky diode were 0.66 eV (*I–V*) and 0.79 eV (*C–V*). Furthermore, when the contact was annealed at 600 °C, the SBH maxima of 0.79 eV (*I–V*) and 0.98 eV (*C–V*) were achieved.

For the MOS Schottky diodes, Bulbul et al. studied electrical and dielectric properties of Al/$HfO_2$/*p*-Si MOS device at different temperatures [11]. By the *C–V* measurement, the SBHs changed from 0.172 to 0.982 eV in the temperature range of 300–400 K. Liu et al. [12] studied hydrogen sensing properties of both Pd/AlGaN and Pd/$SiO_2$/AlGaN-based MOS Schottky diodes. They determined that SBHs of MOS Schottky diode were higher than those of MS Schottky diodes. Moreover, the SBHs of the MOS (MS) diode decreased from 0.98 (0.88) to 0.75 (0.68) eV upon exposing to a 9,660 ppm $H_2$/air gas. Cheng et al. [13] also showed the SBH of Pt–oxide–$Al_{0.3}Ga_{0.7}As$ MOS diodes versus hydrogen concentration. Based on the thermionic-field emission, the SBH was decreased from 1.03 to 0.86 eV after annealing in hydrogen atmosphere.

The metal organic chemical vapor deposition (MOCVD) system has been used for all the reported GaN-based MS and MOS Schottky diodes. The present study, radio-frequency (RF) reactive sputtering technique was chosen as the method to grow all sputtering-made Schottky diode devices because of its advantages such as lower deposition temperature than MOCVD, low equipment cost, and secure working atmosphere (Ar and $N_2$) [14]. Pt for Schottky contact has been selected for its high work function of 5.65 eV [8]. In order to investigate the thermal stability, our MS and MOS Schottky diodes were deposited with RF sputtering followed by annealing at high temperature of 500 °C. The electrical characteristics of Pt Schottky contacts to *n*-GaN MS and MOS diode were calculated by thermionic emission (TE) mode.

## 2 Experimental details

For the MS Schottky diodes, *n*-GaN film was deposited on 200 nm thickness of Pt/$TiO_2$/Si substrate at 400 °C for 40 min by reactive sputtering. The RF power inputted into the GaN cermet target was kept at 100 W under the mixture of Ar and $N_2$ gases at a flow rate of 5 sccm for each. The working pressure during sputtering was kept at $9 \times 10^{-3}$ torr. The detailed experimental procedure for depositing GaN films can be referred to our previous work [14].

For fabricating MOS Schottky diodes, $SiO_2$ was used as the insulator layer at the interface between the Pt metal and *n*-GaN semiconductor. This layer was deposited at 100 °C for 10 min by RF magnetron sputtering with a quartz target under the argon atmosphere. The target was operated at RF power of 80 W. After depositing *n*-GaN films, a blanket layer of Al on the top as the Ohmic contact was sputtered at 200 °C for 30 min with an Al target and the working pressure was also $9 \times 10^{-3}$ torr. For depositing Al, only argon gas was used at a flow rate of 5 sccm meanwhile the RF power was kept at 80 W.

In order to study the thermal annealing effect on Schottky diodes, both MS and MOS Schottky diodes were annealed at 500 °C for 20 min in $N_2$ ambient. The electrical characteristics (*I–V*) of all sputtering-made Schottky diodes were evaluated by using Semiconductor Device Analyzer (Agilent, B1500A) at the room temperature.

## 3 Results and discussion

### 3.1 Structural and surface morphological characteristics

Hall effect measurement (HMS-2000, Ecopia) was conducted for the electron concentration ($N_d$) and carrier mobility (μ) of *n*-GaN films. As a result, they were found to be $N_d = 8.8 \times 10^{16}$ cm$^{-3}$ and $\mu = 42$ cm$^2$ V$^{-1}$ s$^{-1}$ at the room temperature.

By scanning electron microscopy (SEM, JSM-6500F, JEOL), the thickness of $SiO_2$ layer in MOS was measured to be ~70 nm. For Schottky contacts, the Pt layer of 200 nm in thickness was fabricated and the Al layer of 200 nm was used for Ohmic contact. The surface condition of the GaN semiconductor contact to metal layer is the key issue in determining of electrical properties. Figure 1 shows SEM surface morphologies of the *n*-GaN films (a) deposited at 400 °C and (b) annealed at 500 °C. All cross-sectional images were shown as insets in individual image and showed the film thickness of ~1 μm. The microstructure of the as-deposited *n*-GaN film (Fig. 1a) showed smaller grains, much smoother surface, and

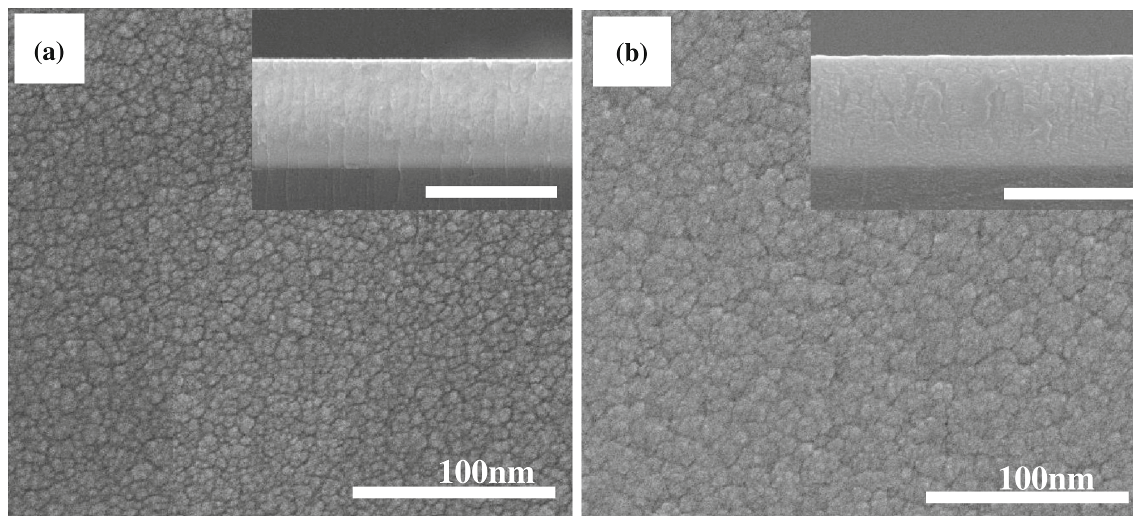


**Fig. 1** SEM surface morphologies of **a** the as-deposited and **b** the 500 °C-annealed *n*-GaN films. The *insets* are the corresponding cross-sectional images

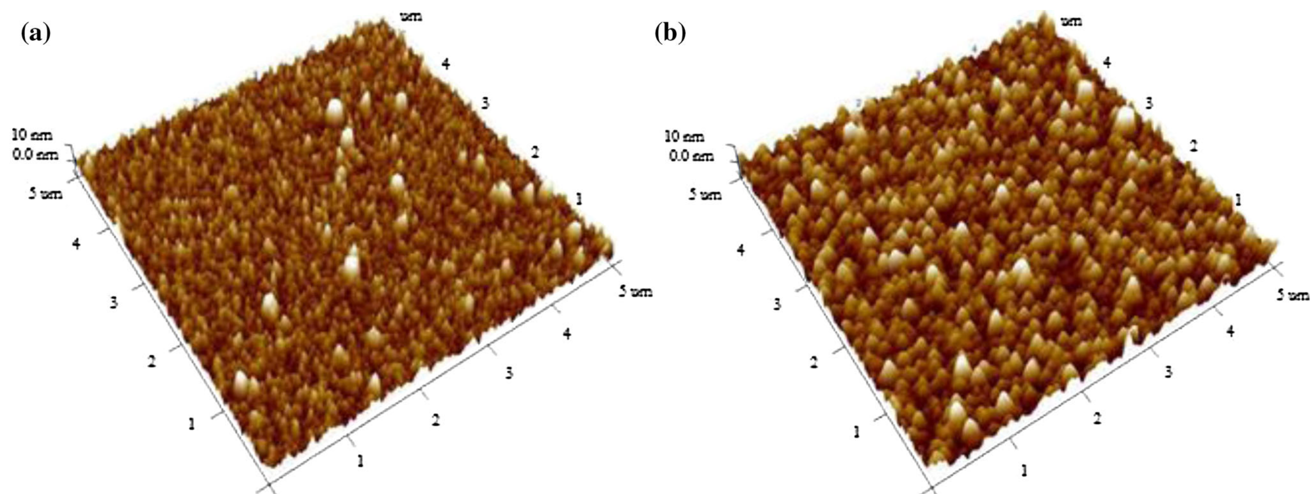


**Fig. 2** AFM topographies of **a** the as-deposited and **b** the 500 °C-annealed *n*-GaN films

columnar growth behavior, as compared with that of the 500 °C-annealed one. From the cross-sectional images, the as-deposited GaN showed the cleavage plane propagating from the substrate to GaN film, which indicated the much oriented growth for the GaN with the columnar growth behavior. Meanwhile, the oriented growth with the columnar microstructure disappeared after annealing at 500 °C (Fig. 1b).

Surface topographies of *n*-GaN films before and after annealing were determined by AFM measurement to find the root-mean-square (rms) values of surface roughness (Fig. 2). The surface morphology of the as-deposited was fairly smooth with the rms roughness of 2.12 nm (Fig. 2a). After the Schottky contact was annealed at 500 °C, the GaN film had the increased rms roughness of 2.65 nm (Fig. 2b). AFM results show that the grains become bigger and surface morphology has been significantly altered after annealing at 500 °C. Therefore, there are suppositions that grain growth and the chemical reactions between metal and semiconductor can have effects on the electrical properties for MS and MOS Schottky diode after annealing.

### 3.2 Current–voltage (I–V) characteristics

The forward and reverse *I–V* characteristics of Pt/*n*-GaN (MS) and Pt/$SiO_2$/*n*-GaN (MOS) Schottky diodes were measured for the as-deposited and the 500 °C-annealed at room temperature. The semilogarithmic *I–V* characteristics are shown in Fig. 3 for (a) MS and (b) MOS Schottky diodes.

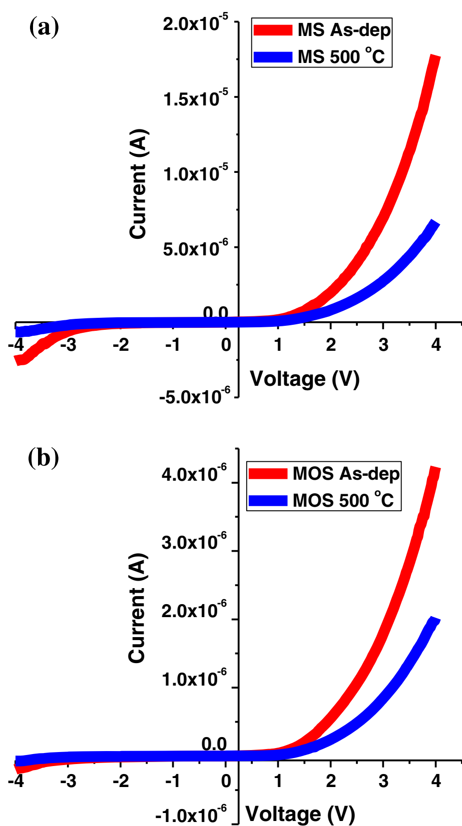


**Fig. 3** The reverse and forward *I*–*V* characteristics for the as-deposited and the 500 °C-annealed. **a** MS and **b** MOS Schottky diodes

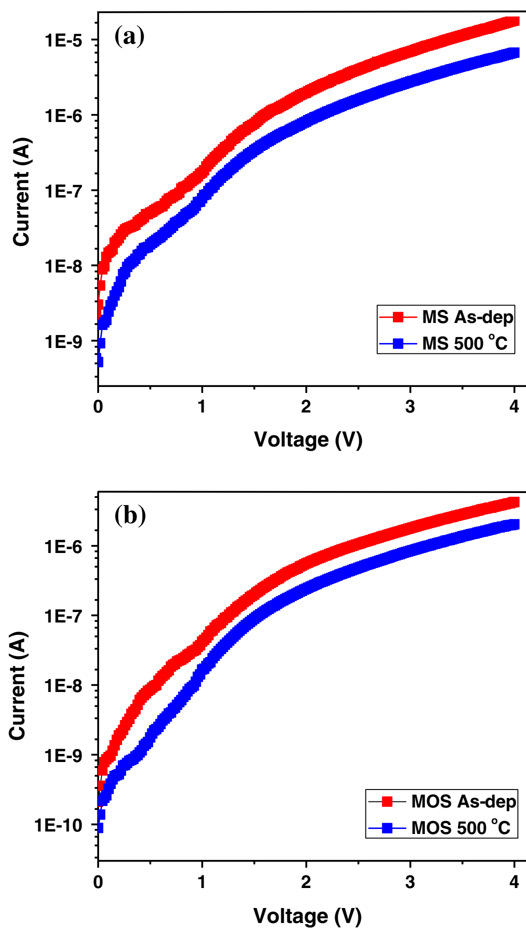


**Fig. 4** Plot of ln(*I*) versus *V* for the as-deposited and the 500 °C-annealed. **a** MS and **b** MOS Schottky diodes

As can be seen from Fig. 3a, the leakage current of MS Schottky diodes decreased after annealing. They were $1.75 \times 10^{-8}$ A for the as-deposited and $1.02 \times 10^{-8}$ A for the annealed under the reverse bias of $-1$ V. For MOS Schottky diodes shown in Fig. 3b, the observed reverse leakage current of MOS Schottky diode is $5.25 \times 10^{-9}$ A at $-1$ V for as-deposited, while it is $1.86 \times 10^{-9}$ A at $-1$ V for the 500 °C-annealed. The *I*–*V* data indicate that the leakage currents of both MS and MOS Schottky diodes are improved after annealing at 500 °C. It has been known that the as-deposited films made by sputtering have a faster growth rate and the attached atoms or adatoms on substrate to form thin film do not have good packing. The annealing process can provide the kinetic energy for the unsettled atoms to pack well and become stable. Therefore, our annealed GaN diodes showed lower leakage current than the as-deposited devices.

The electrical characteristics of Schottky diodes can be generally explained by using the *I*–*V* equation on a standard thermionic emission (TE) mode relation for electron transport from a metal–semiconductor contact (for qV > 3kT). It can be given as below [1, 10, 15, 16]

$$I = I_0\left[exp\frac{q}{nkT}(V - IR_s)\right] \quad (1)$$

where $V$ is applied voltage, $R_s$ series resistance, $n$ ideality factor, and $I_0$ saturation current. $I_0$ can be expressed as below [1, 10]

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \quad (2)$$

where $A^*$ is the effective Richardson constant and $A$ is the diode area. In this study, the electrode of our diode has a square shape and its area was measured to be 1 mm$^2$. $T$ is the experiment temperature in Kelvin, $q$ is electronic charge, $k$ is the Boltzmann constant, and $\phi_B$ is the Schottky barrier height gained from metal–semiconductor contact [10].

The value of $\phi_B$ can be deduced directly from *I*–*V* curves if the effective Richardson constant $A^*$ is known. In this calculation, the theoretical value of $A^*$ was calculated to be 26.4 A cm$^{-2}$ K$^{-2}$, based on the effective electron mass ($m^* = 0.\ 22m_e$) for *n*-GaN Schottky diodes [1, 9].

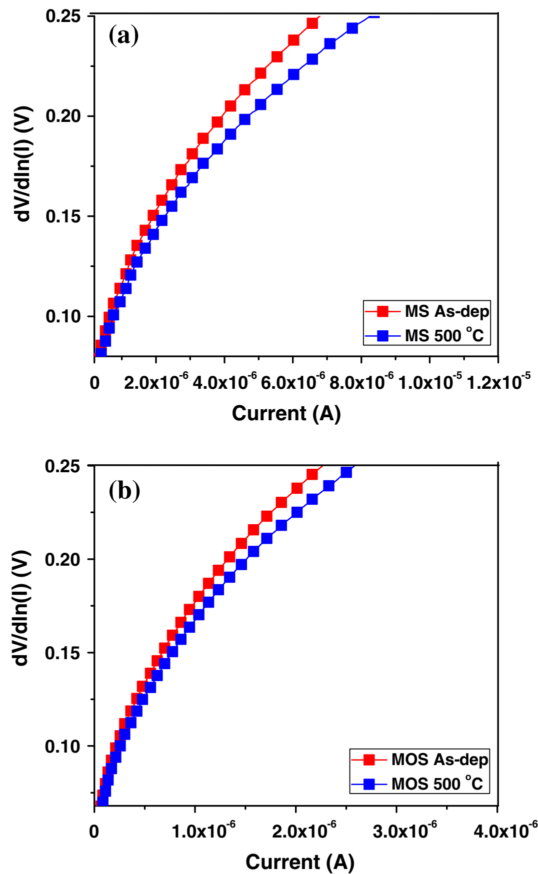


**Fig. 5** Plot of dV/dln($I$) versus $I$ for the as-deposited and the 500 °C-annealed. **a** MS and **b** MOS Schottky diodes

The ideality factor $n$ can be obtained from the slope of the linear region of the forward $I$–$V$ characteristics through the relation:

$$n = \frac{q}{kT}\left(\frac{dV}{dlnI}\right) \quad (3)$$

The plot of ln$I$ versus V, based upon Eq. (1), can be used to derive the saturation current $I_0$, which can be obtained by intersecting the interpolated straight lines of the linear region with the current axis [11, 15–17]. In addition, the value of saturation current $I_0$ is substituted into the Eq. (4) below to calculate the SBH value:

$$\phi_B = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_0}\right) \quad (4)$$

SBHs were 0.76 and 0.78 eV for the as-deposited and the 500 °C-annealed MS Schottky diodes, respectively (Fig. 4a). The SBH values for the as-deposited and the 500 °C-annealed MOS diodes were found to be 0.79 and 0.81 eV, respectively (Fig. 4b). The SBH value of MOS Schottky diode determined was significantly higher than that of MS Schottky diodes.

**Table 1** The parameters and the electrical characteristics of MS and MOS Schottky diodes for the as-deposited and annealing temperatures

| Sample | Leakage current (A) at −1(V) | Schottky barrier height (SBH) (eV) | | From $I$–$V$ | Cheung's function dV/dln($I$) versus $I$ | |
|---|---|---|---|---|---|---|
| | | Cheung's | Norde | $n$ | $R_s$ (kΩ) | $n$ |
| *MS diode* | | | | | | |
| As-dep. | $1.75 \times 10^{-8}$ | 0.76 | 0.85 | 3.12 | 27.9 | 3.19 |
| 500 °C | $1.02 \times 10^{-8}$ | 0.78 | 0.89 | 3.01 | 23.7 | 3.08 |
| *MOS diode* | | | | | | |
| As-dep. | $5.25 \times 10^{-9}$ | 0.79 | 0.91 | 2.83 | 84.4 | 2.96 |
| 500 °C | $1.86 \times 10^{-9}$ | 0.81 | 0.94 | 2.74 | 76.1 | 2.82 |

### 3.3 Calculations the series resistance $R_s$ and ideality factor $n$

Generally, $I$–$V$ characteristics of Schottky diode at low forward bias voltage are linear in a semilogarithmic scale. However, $I$–$V$ characteristics deviate considerably from the ideality factor due to the effect of series resistance $R_s$. The ideality factor $n$ and the series resistance $R_s$ are very important parameters which impact the electrical characteristics of the Schottky diode. Interestingly, $R_s$ and $n$ can be determined from forward bias $I$–$V$ data by Cheung's method [11, 15], which is defined as below:

$$\frac{dV}{d(lnI)} = \frac{nkT}{q} + IR_S \quad (5)$$

Figure 5 shows the $\frac{dV}{d(lnI)}$ versus $I$ plots for the as-deposited and the 500 °C-annealed (a) MS and (b) MOS diodes. The linear region is fitted with the linear curve ($y = A + Bx$) and the series resistance $R_s$ and the ideality factor $n$ can be obtained from the intercept and the slope of the straight line [10, 15–17]. Table 1 provides the results obtained from a detailed calculation of the series resistances $R_s$ and ideality factor $n$ for both MS and MOS Schottky diodes. The as-deposited MS devices had 27.9 kΩ and 3.19 for $R_s$ and $n$, respectively, but dropped to 23.7 kΩ and 3.08 after annealing. The as-deposited MOS devices had 84.4 kΩ and 2.96 for $R_s$ and $n$, respectively, but dropped to 76.1 kΩ and 2.82 after annealing. The MOS device always had a high series resistance due to a thin layer of insulating $SiO_2$.

### 3.4 Norde method

Along with Cheung's method, the Norde method also has been frequently used to calculate the effective SBHs of Pt

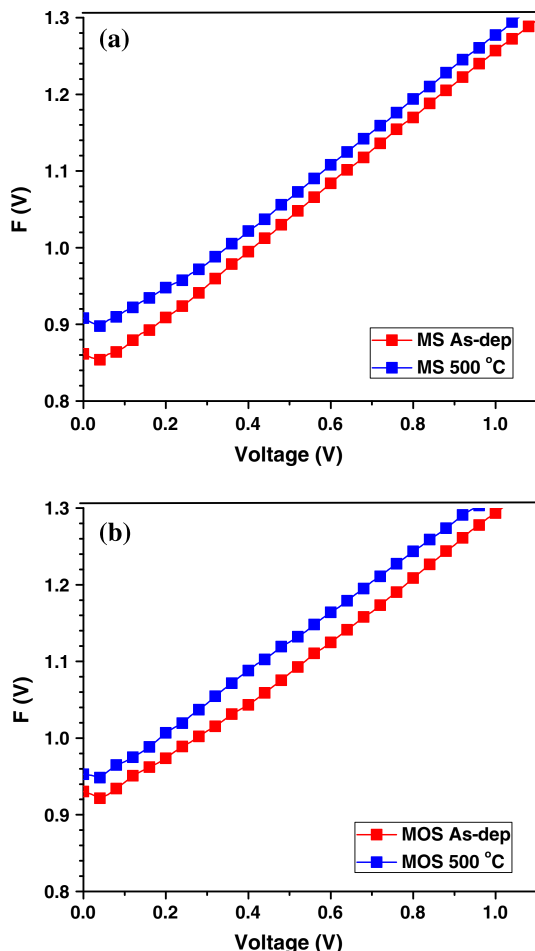


**Fig. 6** Plot of the $F(V)$ versus $V$ for the as-deposited and the 500 °C-annealed. **a** MS and **b** MOS Schottky diodes

Schottky contacts for a comparison purpose [1, 18, 19]. This method involves a Norde function, F($V$, $I$), plotted against $V$. The F($V$, $I$) function is given by

$$F(V,I) = \frac{V}{2} - \frac{kT}{q}\ln\left(\frac{I}{AA^{*}T^{2}}\right) \quad (6)$$

The effective SBH $\phi_B$ is calculated by the following equation:

$$\phi_B = F(V_{min}) + \frac{V_{min}}{2} - \frac{kT}{q} \quad (7)$$

where F($V_{min}$) is the minimum value of F($V$) and $V_{min}$ is the corresponding voltage [2].

Figure 6 shows the F($V$,$I$) versus $V$ curves of the as-deposited and the 500 °C-annealed (a) MS and (b) MOS Schottky diodes. The SBHs, based upon Eqs. (6) and (7), were 0.85 and 0.89 eV for the as-deposited and the annealed MS diodes, respectively. They were 0.91 and 0.94 eV for MOS diodes before and after annealing.

## 4 Discussion

Table 1 shows a comparison for the derived data from MS and MOS Schottky diodes. A positive correlation is explored between the leakage current and the SBHs, i.e. the higher SBH the lower leakage current. It is noted that the SBH values calculated by the Cheung's method are lower than those by the Norde method. These findings indicate that both MS and MOS Schottky diodes display improved electrical properties after annealing at high temperature of 500 °C. Our SBH of 0.76 eV obtained by the Cheung's method is consistent with the reported values of 0.66–0.82 eV for GaN-based MS Schottky diodes with the $n$-GaN made by MOCVD [1, 8–10]. As other's SBHs had shown a big change after annealing at and above 300 °C, our SBH was relatively stable after annealing at 500 °C.

Noticeably, there is a slight increase in the SBHs of MOS Schottky diodes comparing with MS Schottky diode for both Cheung's and Norde methods. The development of a high-quality thin insulator layer of $SiO_2$ for the MOS Schottky diode has become an important issue [3], because the amount of the polarized $SiO_2$ layer also causes a considerable change of the electrical field across the depletion region near the GaN surface. With the change in the insulation oxide layer, SBHs, leakage current, and breakdown voltage will be totally changed [3, 4, 11].

The SBH enhancement after annealing at 500 °C for both MS and MOS Schottky diodes is explained. The increase of the SBHs after annealing can be correlated with the change of nonstoichiometric defects in the metallurgical interface [2, 8]. Based upon the disappearance of the propagation streaks of cleavage planes after annealing (the inset in Fig. 1b), it is possible that high density of defects occur at our GaN/Pt interface due to the formation of Ga–Pt intermetallic phases after annealing at 500 °C or the sharp $n$-GaN/Pt interface has become disordered. High density of defects and disordered interface will lead to the enhancement in the recombination of electrons and holes via deep-level traps in the space-charge region and cause the Schottky contact to exhibit a strong deviation from its ideal behavior.

In addition, structural and surface morphological characteristics of $n$-GaN films can play an important role in the electrical properties of metal–semiconductor contact, as shown by SEM and AFM analyses. The microstructure of $n$-GaN films is much rougher and has lost its oriented growth pattern after annealing at 500 °C. From AFM analysis, the rms roughness of $n$-GaN films for the annealed contacts is higher than those as-deposited contacts. The rougher surface can be caused by interfacial reactions between metals and $n$-GaN films, which also explains the increase in SBH after annealing. Similar results were also explained by Rajagopal Reddy et al. [1, 7]

and Siva Pratap Reddy et al. [10]. They indicated that the rms roughness of the as-deposited films is smaller than that after annealing. The presence of interfacial reactions at the metal–semiconductor junction plays a vital role in evaluating the device properties. Thus, the barrier height of Schottky contact after annealing always increased, as compared to that of the as-deposited one.

Different ideality factors with $n$ of 2.74–3.12 (by Eq. 3 via $I$–$V$ curve) and 2.82–3.19 (Eq. 5 of Cheung's method) in Table 1 have been obtained from our different Schottky diodes. However, the lower ideality factor $n$ after annealing at 500 °C can be correlated to the increase in SBH. There is also a clear trend of increasing the $R_s$ value of MOS Schottky diode compared to that of MS Schottky diode. This result can be admitted that there is an insulator layer of $SiO_2$ in MOS device, which builds up an dielectric layer with the induced dipole during forward bias and affects the values of $Rs$ and $n$ [3, 4, 12].

## 5 Conclusions

All sputtering-made Pt contacts to $n$-GaN MS and MOS diodes have been successfully made and characterized by the current–voltage test followed by analyzing the electrical parameters through the Cheung's and Norde methods. It is shown that the SBHs of Pt/$n$-GaN and Pt/$SiO_2$/$n$-GaN Schottky diodes were found to be 0.76 and 0.79 eV, respectively, by the Cheung's method and 0.85 and 0.91 eV by the Norde method. After annealing at 500 °C, there is a slight change in the SBHs due to larger surface roughness and interfacial disorder and reactions. The annealed MS and MOS Schottky diodes with a higher SBH and a denser microstructure also showed the improved leakage currents of $1.02 \times 10^{-8}$ and $1.86 \times 10^{-9}$ A, respectively. The diode is toward the ideal one after the ideality factor $n$ becomes smaller for the annealed diode. The MOS diode showed a high series resistance of 84.4 KΩ, as compared to 27.9 KΩ for the MS diode. The major effort of this work demonstrates the possibility of using the cost-effective RF sputtering for III-nitride electronic devices.

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